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Single Transistor RC-Only Second-Order Allpass Filters

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Abstract

In this letter, all possible single transistor RC-only second-order allpass filters obtainable from a four impedance common-source topology are reported. It is shown that there are only seven such filters with only one of them being a minimum component canonical 2R-2C filter. Two of the found filters are designed and simulated in a 65-nm CMOS process.

Keywords: allpass filters, CMOS analog circuits, filter theory, NMOS RC-only filters, two-port network

1 Introduction

Allpass filters are becoming increasingly important in building modern Ultra Wide Band (UWB) wireless communication systems where they are mainly used as True Time Delay (TTD) elements [1]. TTD elements are essential in beam forming and impulse radio receivers for synchronizing the received radio frequency (RF) signal with the locally generated pulse signal [2,3]. However, allpass filters reported in the literature are predominantly LC filters that are either purely passive [2] or require many transistors, such as the bipolar transistor-based design in Ulusoy et al. [1].

Since using allpass filters to replace digital delay stages significantly reduces the hardware complexity and cost [3,4], designing allpass filter cells in current- and voltage- modes using single transistors has been attempted in Ahmadi et al. [5,6] with excellent performance being achieved at RF frequencies. Fully differential allpass filter cells were also recently reported in Elamien et al. [7] and in Maundy et al. [8] among other types of filters. It is again noted that all of the thus far reported second-order single transistor filters have been LC-type filters with at least one inductor required [6,7]. This also includes the filters in [9–11]. Transistor-based first-order RC allpass filters have however been previously reported in Wijenayake et al. [12] as well as first-order sinh domain allpass filters [13]. In Tangsritrat and Pukkalanun [14] second-order allpass filters were constructed using current differencing transconductance amplifiers (CDTAs), but the number of transistors used is very large. Allpass filters based on such active building blocks are not suitable for high frequency operation.

In this letter we attempt to explore the possibility of obtaining RC second-order allpass filters using a single transistor surrounded by four impedances in a common-source topology. The automated search procedure is based on the two-port network modeling as explained in detail in Maundy et al. [15]. This procedure has proven its success in facilitating the search for circuits that satisfy a certain design criteria based on predefined circuit structure using the strength of symbolic mathematics tools [8].

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2 Proposed Second-Order Allpass Filters

Consider the proposed circuit shown in Fig. 1(a) where NMOS transistor M_1 , assumed to be operating in saturation mode, is surrounded by impedances Z_i ($i = s, 1, 2, 3$). The LC allpass filter reported in Ahmadi et al. [6] also belongs to this topology. However, here we are interested in RC filters only and hence we limit the impedance settings to the following types: individual R_i, C_i , series $R_i + C_i$, or parallel $R_i // C_i$. Current sources $I_{a,b}$ are present to ensure the correct DC biasing of the transistor. To model the transistor, we make use of the general two-port network transmission matrix defined as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} = [T] \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (1)$$

where V_1, I_1 are the voltage and current at the input ports, while V_2, I_2 are those at the output port as shown in Fig. 1(b). This two-port network representation assumes the device is linearized around its DC operating point. Different transmission matrices can be used depending on the sophistication of the transistor model required in the analysis.

$$[T_1] = \begin{bmatrix} 0 & -\frac{1}{g_m} \\ 0 & 0 \end{bmatrix} \quad (2a)$$

$$[T_2] = \begin{bmatrix} \frac{(1/r_o + sC_{gd})}{sC_{gd} - g_m} & \frac{1}{sC_{gd} - g_m} \\ \frac{(C_{gd}C_{gs}r_o s + C_{gd}g_m r_o + C_{gs} + C_{gd})s}{sC_{gd} - g_m} & \frac{(C_{gs} + C_{gd})s}{sC_{gd} - g_m} \end{bmatrix} \quad (2b)$$

The simplest model of (2a), considers only an ideal MOS transistor with a small-signal transconductance g_m . If the transistor's output resistance r_o in addition to the parasitic gate-to-source capacitance C_{gs} and gate-to-drain capacitance C_{gd} are included, then the matrix of (2b) can be used. More complex matrices can be developed depending on the level of complexity in the transistor model [16].

Figure 1: (a) General four-impedance single-transistor circuit biasing current sources $I_{a,b}$ and (b) corresponding equivalent circuit with M_1 replaced by its two port representation.

Straightforward analysis of the circuit in Fig. 1(b) indicates that it has a transfer function $H(s) = \frac{V_o(s)}{V_{in}(s)}$, input impedance $Z_{in}(s)$ and output impedance $Z_{out}(s)$ given respectively by

$$H(s) = \frac{Z_1 Z_2 (Z_3 + a_{12}) + Z_s \Delta Z}{Z_1 Z_2 (a_{11} Z_3 + a_{12}) + a_{12} Z_1 Z_3 + Z_s \Delta Z} \quad (3)$$

$$Z_{in}(s) = Z_s + \frac{Z_1 Z_2 (a_{11} Z_3 + a_{12}) + a_{12} Z_1 Z_3}{\Delta Z} \quad (4)$$

$$Z_{out}(s) = \frac{Z_1 Z_3 [Z_2 (a_{12} - Z_s (a_{11} + a_{22} + |a|))] + a_{12} Z_3 Z_s (Z_1 + Z_2)}{Z_1 Z_2 (a_{11} Z_3 + a_{12}) + a_{12} Z_1 Z_3 + Z_s \Delta Z} \quad (5)$$

where

$$\begin{aligned} \Delta Z &= Z_3 (a_{22} Z_1 + a_{11} Z_2 + a_{21}) + a_{12} (Z_1 + Z_2 + Z_3) \\ &\quad - Z_1 Z_2 (a_{11} + a_{22} + |a|) \end{aligned}$$

and $|a| = a_{11} a_{22} - a_{12} a_{21}$. In general the circuit in Fig. 1(a) can realize transfer functions of the form

$$H(s) = \frac{s^2 + \frac{\omega_z}{Q_z} s + \omega_z^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2}. \quad (6)$$

When $\omega_z = \omega_o$ and with the appropriate choice of g_m such that $Q_z = -Q$, second-order allpass transfer functions can be obtained. Note that Q for this filter type is always less than 1/2.

A systematic search was conducted using Maple [15] to discover all the possible RC allpass filters belonging to this topology. The result is seven possible filters given in Table 1 where the required impedances Z_i ($i = s, 1, 2, 3$), g_m condition that results in $Q_z = -Q$ as well as pole frequency values are given. As noted from Table 1 and since g_m must always remain positive implies that the conditions $C_s > 2C_3$ in 5 of the filters or $R_3 > 2R_s$ in the other two filters must be satisfied. Other observations from the Table include:

- The maximum theoretical Q of all filters is 1/2, ensuring that no peaking occurs in the delay response which has a maximally flat DC delay of $D(0) = \frac{2}{Q\omega_o}$ decreasing at ω_o to a delay $D(\omega_o) = \frac{4Q}{\omega_o}$.
- Resistor R_2 between drain and source is present in all the filters making it in effect parallel with the output resistance r_o of M_1 . That is $R_{2,eff} = R_2 / r_o$.
- Capacitances C_1 and C_3 are located in parallel with C_{gs} and C_{gd} , respectively and can be factored in the computation of C_1 and C_3 . That is $C_{1,eff} = C_1 + C_{gs}$ and $C_{3,eff} = C_3 + C_{gd}$.
- Filters #6 and #7 have a pole/zero frequency that is independent of g_m and dependent only on the passive components.
- Filter #6 is a canonical filter with the minimum number of components.
- Filters #1 through #5 are self biased by the presence of R_3 ensuring that M_1 is always in saturation. Filters #6 and #7 conversely must be DC biased for proper operation in saturation.
- Any error in satisfying the required condition on g_m results in a magnitude “bump” or “dip” given by $|H(\omega_o)| = \left| \frac{Q}{Q_z} \right|$.

Table 1: A list of all possible RC filters that satisfy (6) along with pole/zero frequency ω_o and the g_m required to satisfy $Q_z = -Q$.

#	Z_s, Z_1, Z_2, Z_3	$\omega_o = \omega_z$	$\frac{Q}{Q_z}$	$g_m (Q_z = -Q)$
1	$C_s, R_1, R_2, R_3 // C_3$	$\sqrt{\frac{g_m R_1 R_2 + R_1 + R_2 + R_3}{C_s C_3 R_1 R_2 R_3}}$	$\frac{C_s C_3 R_1 R_2 R_3 \sqrt{\frac{g_m R_1 R_2 + R_1 + R_2 + R_3}{C_s C_3 R_1 R_2 R_3}}}{C_3 R_2 R_3 + R_1 (C_s R_2 + R_3 (C_3 + C_s + g_m C_3 R_2))}$ $\frac{C_s C_3 R_1 R_2 R_3 \sqrt{\frac{g_m R_1 R_2 + R_1 + R_2 + R_3}{C_s C_3 R_1 R_2 R_3}}}{C_3 R_2 R_3 + R_1 (C_3 R_3 + R_2 (C_s + g_m R_3 (C_3 - C_s)))}$	$\frac{C_s \left(\frac{2}{R_3} + \frac{1}{R_2} \right) + 2C_3 \left(\frac{1}{R_2} + \frac{1}{R_1} \right)}{(C_s - 2C_3)}$
2	$C_s, C_1, R_2, R_3 // C_3$	$\sqrt{\frac{1+g_m R_2}{R_2 R_3 C_3 (C_1 + C_s)}}$	$\frac{R_2 R_3 C_3 (C_1 + C_s) \sqrt{\frac{1+g_m R_2}{R_2 R_3 C_3 (C_1 + C_s)}}}{R_2 (C_1 + C_s) + R_3 (C_1 + C_s + C_3 + g_m R_2 C_3)}$ $\frac{R_2 R_3 C_3 (C_1 + C_s) \sqrt{\frac{1+g_m R_2}{R_2 R_3 C_3 (C_1 + C_s)}}}{R_3 (C_1 + C_3) + R_2 (C_1 + C_s + g_m R_3 (C_3 - C_s))}$	$\frac{C_s \left(\frac{2}{R_3} + \frac{1}{R_2} \right) + 2C_1 \left(\frac{1}{R_2} + \frac{1}{R_3} \right) + \frac{2C_3}{R_2}}{(C_s - 2C_3)}$
3	$C_s, R_1 // C_1, R_2, R_3 // C_3$	$\sqrt{\frac{g_m R_1 R_2 + R_1 + R_2 + R_3}{(C_1 + C_s) C_3 R_1 R_2 R_3}}$	$\frac{(C_1 + C_s) C_3 R_1 R_2 R_3 \sqrt{\frac{g_m R_1 R_2 + R_1 + R_2 + R_3}{(C_1 + C_s) C_3 R_1 R_2 R_3}}}{C_3 R_2 R_3 + R_1 ((C_1 + C_s) R_2 + R_3 (C_3 + C_1 + C_s + g_m C_3 R_2))}$ $\frac{(C_1 + C_s) C_3 R_1 R_2 R_3 \sqrt{\frac{g_m R_1 R_2 + R_1 + R_2 + R_3}{(C_1 + C_s) C_3 R_1 R_2 R_3}}}{C_3 R_2 R_3 + R_1 (C_3 R_3 + R_2 (C_1 + C_s + g_m R_3 (C_3 - C_s)))}$	$\frac{C_s \left(\frac{2}{R_3} + \frac{1}{R_2} \right) + 2C_1 \left(\frac{1}{R_2} + \frac{1}{R_3} \right) + 2C_3 \left(\frac{1}{R_2} + \frac{1}{R_1} \right)}{(C_s - 2C_3)}$
4	$R_s + C_s, C_1, R_2, R_3$	$\sqrt{\frac{1+g_m R_2}{C_s C_1 R_s (R_2 + R_3)}}$	$\frac{R_s C_s C_1 (R_2 + R_3) \sqrt{\frac{1+g_m R_2}{C_s C_1 R_s (R_2 + R_3)}}}{C_1 (R_2 + R_3) + C_s (R_2 + R_3 + R_s + g_m R_2 R_s)}$ $\frac{R_s C_s C_1 (R_2 + R_3) \sqrt{\frac{1+g_m R_2}{C_s C_1 R_s (R_2 + R_3)}}}{C_1 (R_2 + R_3) + C_s (R_s + R_2 (1 + g_m (R_s - R_3)))}$	$\frac{2 \frac{C_1}{C_s} \left(1 + \frac{R_3}{R_2} \right) + 2 \left(1 + \frac{R_s}{R_2} \right) + \frac{R_3}{R_2}}{(R_3 - 2R_s)}$
5	$R_s + C_s, R_1 // C_1, R_2, R_3$	$\sqrt{\frac{g_m R_1 R_2 + R_1 + R_2 + R_3}{C_s C_1 R_1 R_s (R_2 + R_3)}}$	$\frac{\sqrt{\frac{g_m R_1 R_2 + R_1 + R_2 + R_3}{C_s C_1 R_1 R_s (R_2 + R_3)}}}{\frac{1}{R_s C_s} + \frac{1}{R_1 C_1} + \frac{(g_m R_s R_2 + R_s + R_2 + R_3)}{R_s (R_2 + R_3) C_1}}$ $\frac{\sqrt{\frac{g_m R_1 R_2 + R_1 + R_2 + R_3}{C_s C_1 R_1 R_s (R_2 + R_3)}}}{\frac{1}{R_s C_s} + \frac{1}{R_1 C_1} + \frac{(g_m R_2 (R_s - R_3) + R_s + R_2)}{R_s (R_2 + R_3) C_1}}$	$\frac{2 \frac{C_1}{C_s} \left(1 + \frac{R_3}{R_2} \right) + 2 \left(1 + \frac{R_s}{R_1} + \frac{R_3 R_s}{R_1 R_2} + \frac{R_s + R_3/2}{R_2} \right)}{(R_3 - 2R_s)}$
6	C_s, R_1, R_2, C_3	$\sqrt{\frac{1}{R_1 R_2 C_s C_3}}$	$\frac{\sqrt{R_1 R_2 C_3 C_s}}{R_1 C_s + C_3 (R_1 + R_2 + g_m R_1 R_2)}$ $\frac{\sqrt{R_1 R_2 C_3 C_s}}{R_2 C_3 + R_1 (C_3 + g_m R_2 (C_3 - C_s))}$	$\frac{2C_3 \left(\frac{1}{R_1} + \frac{1}{R_2} \right) + \frac{C_s}{R_2}}{(C_s - 2C_3)}$
7	$C_s, R_1 // C_1, R_2, C_3$	$\sqrt{\frac{1}{R_1 R_2 C_3 (C_1 + C_s)}}$	$\frac{\sqrt{R_1 R_2 C_3 (C_1 + C_s)}}{R_2 C_3 + R_1 (C_s + C_1 + C_3 + g_m R_2 C_3)}$ $\frac{\sqrt{R_1 R_2 C_3 (C_1 + C_s)}}{R_2 C_3 + R_1 (C_1 + C_3 + g_m R_2 (C_3 - C_s))}$	$\frac{2C_3 \left(\frac{1}{R_1} + \frac{1}{R_2} \right) + \frac{2C_1}{R_2} + \frac{C_s}{R_2}}{(C_s - 2C_3)}$

3 Simulation Results

To validate the operation of the found second-order allpass filters, topologies #1 and #4 were selected. The design in LTspice software is based on the PTM (Predictive Technology Model) 65 nm level-54 CMOS process BSIM4 parameters [17]. The filter setup and design parameters are listed in Table 2. In Figs. 2(a) and (b), the ideal and simulated gain and phase responses of the circuits #1 and #4 are depicted, respectively in wide frequency range by varying n in range $\{100 \rightarrow 0.01\}$ with decrement $10\times$. Hence, the simulated frequencies $f_{o_sim(n)} = f_{z_sim(n)}$ were varied as (10.56 kHz; 105.63 kHz; 1.06 MHz; 10.52 MHz; 101.67 MHz) and (10.02 kHz; 100.16 kHz; 1 MHz; 9.91 MHz; 90.21 MHz) for the two circuits respectively, via changing of the capacitor values while keeping other design parameters at their default values given in Table 2. Note that the ideal pole frequencies are (10 kHz; 100 kHz; 1 MHz; 10 MHz; 100 MHz). These simulation results confirm the excellent behavior of the circuits and the minimal discrepancies in phase responses. The quality factors of circuits #1 and #4 are respectively 0.341 and 0.233 while the power consumptions are respectively 79.06 μ W and 18.74 μ W from a 0.65 V supply and corresponding group delays are 93 and 136 nanoseconds. Note that in Figs. 2(a) and (b), zooms on the pole frequency region and group delay responses (at $n = 0.1$) are also depicted as insets.

The output and equivalent input noise variations against frequency at $n = 0.1$ have also been simulated and shown in Fig. 3. The equivalent output/input noise values at the simulated pole frequencies of circuits #1 and #4 are respectively 13.102 nV/ $\sqrt{\text{Hz}}$ / 13.073 nV/ $\sqrt{\text{Hz}}$ and 20.85 nV/ $\sqrt{\text{Hz}}$ / 20.79 nV/ $\sqrt{\text{Hz}}$. The effect of temperature on $f_{o_sim(n=0.1)}$ of both at $\varphi = -180^\circ$ was examined in the range $T \in \{-30; +70\}^\circ\text{C}$ with increment 1°C , i.e. 100 samples, and simulation results with corresponding statistical evaluation are depicted in Fig. 4.

Table 2: Design parameters of the selected filters

Circuit	#1					#4				
n (-)	100	10	1	0.1	0.01	100	10	1	0.1	0.01
CMOS technology	PTM 65 nm level-54 CMOS process BSIM4									
V_{dd} (V)	0.65									
M_1 W/L ($\mu\text{m}/\mu\text{m}$)	3.1 / 0.5					4.4 / 0.5				
$I_a = I_b$ (μA)	200					85				
g_m ($\mu\text{A}/\text{V}$) calcul. / sim.	513 / 563					490 / 534				
R_s ($\text{k}\Omega$)	-					1.62				
R_1 ($\text{k}\Omega$)	21					-				
R_2 ($\text{k}\Omega$)	10.5					11.5				
R_3 ($\text{k}\Omega$)	14					15				
C_s (pF)	$n \times 78.7$					$n \times 91$				
C_1 (pF)	-					$n \times 43$				
C_2 (pF)	-					-				
C_3 (pF)	$n \times 16.5$					-				
Q (-)	0.341					0.233				
$f_{o_ideal(n)} = f_{z_ideal(n)}$ (Hz)	10 k	100 k	1 M	10 M	100 M	10 k	100 k	1 M	10 M	100 M
$f_{o_sim(n)} = f_{z_sim(n)}$ (Hz)	10.56 k	105.63 k	1.06 M	10.52 M	101.67 M	10.02 k	100.16 k	1 M	9.9 M	90.21 M

Figure 2: Ideal and simulated gain and phase responses of the tested allpass filters for $n \in \{100 \rightarrow 0.01 : 10\}$. Corresponding zoom-in pole frequency region and group delay responses (see insets) at $n = 0.1$: (a) circuit #1, (b) circuit #4.

To illustrate the time-domain stability, transient analysis at $f_{o_sim(n=0.1)}$ are depicted in Fig. 5 along with the simulated total harmonic distortion (THD) variation versus the amplitude of the applied input voltage signal. THD values of 1.5% and 6.6%, respectively, are measured at 100 mV input. The input-referred third-order intercept point (IIP3) values of the circuits #1 and #4 at 10 MHz are 22.65 and 19.26 dBm, respectively. Moreover, the corresponding FFT spectrums of the output signals are shown in Fig. 6.

Finally, in order to evaluate the potential variation of the proposed filter parameters due to tolerances incurred from manufacturing processes, Monte Carlo statistical analysis is performed for resistors, capacitors, NMOS aspect ratio, and selected parameters of transistor model used (T_{oxe} , V_{th0} , K_1 , μ_0) with $\sigma=5\%$ tolerance for Gaussian distribution and 200 runs. Figures 7(a) and (b) show the simulated gain and phase responses with corresponding statistical evaluation for both tested filter circuits.

Figure 3: Simulated output and equivalent input noise variations versus frequency at $n = 0.1$.

Figure 4: Simulated temperature dependence of pole frequency and corresponding histograms for $n = 0.1$.

Figure 5: Transient simulations of input (100mV) and output signals and Total Harmonic Distortion (THD) of circuits #1 and #4 at $f_{o_sim}(n=0.1)$.

Figure 6: Simulated FFT spectrum of output of circuits #1 and #4 at $n = 0.1$.

Figure 7: Monte Carlo statistical analysis: Variations of the pole frequency at $\varphi = -180^\circ$ vs. variations of the gain and simulated gain and phase responses as insets (at $n = 0.1$): (a) circuit #1, (b) circuit #4.

4 Conclusion

In this letter, we reported the seven possible second-order RC allpass filters that can be obtained from a single transistor four impedance configuration. While only one filter is canonical with a pole frequency that depends on the passive component values only, most of the other filters have a pole frequency that can be electronically tunable through the transistor's g_m . LTspice simulation results using a 65nm technology file verify the correct operation of the circuits.

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