BRNO UNIVERSITY OF TECHNOLOGY
VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION
FAKULTA ELEKTROTECHNIKY
A KOMUNIKAČNÍCH TECHNOLOGIÍ

DEPARTMENT OF MICROELECTRONICS
ÚSTAV MIKROELEKTRONIKY

CONTROL UNIT FOR CUBESAT
ŘÍDICÍ JEDNOTKA PRO CUBESAT

MASTER'S THESIS
DIPLOMOVÁ PRÁCE

AUTHOR — **Bc. Jan Horký**
AUTOR PRÁCE

SUPERVISOR — **Ing. Michal Kubíček, Ph.D.**
VEDOUCÍ PRÁCE

BRNO 2017

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ
FAKULTA ELEKTROTECHNIKY A KOMUNIKAČNÍCH TECHNOLOGIÍ

Diplomová práce

magisterský navazující studijní obor **Mikroelektronika**
Ústav mikroelektroniky

Student: Bc. Jan Horký ***ID:*** 146830
Ročník: 2 ***Akademický rok:*** 2016/17

NÁZEV TÉMATU:

Řídicí jednotka pro CubeSat

POKYNY PRO VYPRACOVÁNÍ:

Ve spolupráci s firmou CSRC, s.r.o. navrhněte koncepci řídicí jednotky pro CubeSat s obvodem FPGA a vhodnými pamětmi. Jednotka bude umožňovat řídit CubeSat a zároveň zpracovávat uživatelská data. Jednotku vybavte základní sadou senzorů pro monitorování jejího stavu.
Ověřte funkčnost jednotky a vytvořte digitální design pro FPGA, který využije všechny její funkce.

DOPORUČENÁ LITERATURA:

[1] FUKÁTKO, Tomáš. Detekce a měření různých druhů záření. Praha: BEN - technická literatura, 2007. Senzory neelektrických veličin. ISBN 978-80-7300-193-3.

[2] ŠŤASTNÝ, Jakub. FPGA prakticky: realizace číslicových systémů pro programovatelná hradlová pole. Praha: BEN - technická literatura, 2010. ISBN 978-80-7300-261-9.

Termín zadání: 6.2.2017 ***Termín odevzdání:*** 25.5.2017

Vedoucí práce: Ing. Michal Kubíček, Ph.D.
Konzultant:

doc. Ing. Lukáš Fujcik, Ph.D.
předseda oborové rady

BRNO UNIVERSITY OF TECHNOLOGY
FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

Master's Thesis

Master's study field **Microelectronics**
Department of Microelectronics

Student: Bc. Jan Horký ***ID:*** 146830

Year of study: 2 ***Academic year:*** 2016/17

TITLE OF THESIS:

Control unit for CubeSat

INSTRUCTION:

Design an FPGA-based CubeSat control unit in cooperation with CSRC Company. The control unit will be equipped with a suitable set of memories and will enable both CubeSat control and user data processing. Equip the control unit with a set of basic sensors for monitoring of its status.
Verify the design functionality and prepare an FPGA configuration that will test all the functions of the unit.

The project will be done in cooperation with CSRC, spol. s r.o.

RECOMMENDED LITERATURE:

[1] FUKÁTKO, Tomáš. Detekce a měření různých druhů záření. Praha: BEN - technická literatura, 2007. Senzory neelektrických veličin. ISBN 978-80-7300-193-3.

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Date of project specification: 6.2.2017 ***Deadline for submission:*** 25.5.2017

Leader: Ing. Michal Kubíček, Ph.D.
Consultant:

doc. Ing. Lukáš Fujcik, Ph.D.
Subject Council chairman

ABSTRAKT

Cílem práce je návrh univerzální řídicí jednotky pro CubeSat založené na obvodu FPGA Taková jednotka doposud nebyla komerčně dostupná a navržená jednotka má tak dobrý potenciál zaplnit příslušné místo na trhu komponent pro CubeSat. Celá jednotka je navržena z komerčně dostupných komponent. Návrh jednotky je proveden tak, aby umožnil její funkci ve vesmírném prostředí. Stav konfigurace FPGA je pravidelně kontrolován a v případě zjištěné chyby dochází automaticky k rekonfiguraci FPGA a návratu jednotky do výchozího stavu. Jednotka obsahuje sadu senzorů, které monitorují její stav a v případě potřeby je možné na základě jejich výstupů provést opatření z hlediska ochrany funkce jednotky. Dvě paměti MRAM umožňují uložení tovární a uživatelské konfigurace FPGA, mezi kterými dochází k automatickému přepnutí na základě korektnosti uživatelské konfigurace.

KLÍČOVÁ SLOVA

Vesmír, CubeSat, Řídicí jednotka, Radiace, FPGA

ABSTRACT

The aim of the thesis is a design of a CubeSat control unit. Similar unit could not be found on the market and proposed unit has a potential to fill the gap. The board is composed of commercial parts yet reliable in the space environment. Because of its benefits, an FPGA was selected as the core of the board. The FPGA is periodically checked for errors and reset to default state if an error is found. The unit has various sensors to monitor its condition and can do necessary measures. Two MRAMs allow store golden bitstream and upload new bitstream in flight which are switched based on proper operation.

KEYWORDS

Space, CubeSat, Control Unit, Radiation, FPGA

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Experimentální část této diplomové práce byla podpořena výzkumnou infrastrukturou vybudovanou v rámci projektu CZ.1.05/2.1.00/03.0072
Centrum senzorických, informačních a komunikačních systémů (SIX)
operačního programu Výzkum a vývoj pro inovace.

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EVROPSKÁ UNIE
EVROPSKÝ FOND PRO REGIONÁLNÍ ROZVOJ
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2007-13
OP Výzkum a vývoj pro inovace

PROHLÁŠENÍ

Prohlašuji, že svou diplomovou práci na téma Řídicí jednotka pro CubeSat jsem vypracoval samostatně pod vedením vedoucího diplomové práce a s použitím odborné literatury a dalších informačních zdrojů, které jsou všechny citovány v práci a uvedeny v seznamu literatury na konci práce.

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V Brně dne ....

(podpis autora)

PODĚKOVÁNÍ

Děkuji vedoucímu diplomové práce Ing. Michalu Kubíčkovi, Ph.D. za účinnou metodickou, pedagogickou a odbornou pomoc a další cenné rady nejen při zpracování mé diplomové práce.

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Contents

Introduction

Since the beginning of the space exploration, space satellites had been objects of large volume and weight to be able to do all experiments and measurements. That made the cost of a satellite and its launch so expensive that only governmental space agencies could afford it.

Ongoing researches and new inventions in fields like electronics, mechatronics, and mechanics have been making devices smaller, cheaper and smarter. The computing power of processors, new types of algorithms and programming languages allowed to reduce the number of discrete parts and implement them as software. Due to the progress, satellites can be smaller, lighter and perform more tasks and experiments.

The idea of CubeSat was developed at the California Polytechnic State University together with Stanford University to teach students how to develop, design and manufacture space satellites. CubeSat were defined as U-class spacecraft with dimensions of 10x10x10 cm and weight up to 1.33 kg per unit. Since then, tens of universities have joined the international collaboration, and many private companies have been designing and manufacturing CubeSat or its parts. Specialized internet shops, selling parts for CubeSat were also founded.

Because of its small volume and weight, a CubeSat is significantly specialized, mostly for only one experiment. In most of the cases, there is not a need for high computing power. Therefore most of the control units use microcontrollers as CPU. If there is a need for faster signal processing, parallel processes or high computing power, a customer has to develop suitable board on his own as such types are not available on the market. That significantly increases overall cost and development time.

The aim of this thesis is to design and test control unit which can fill this gap on the market. The board is designed to be reliable in the harsh space environment and is designed according to European Space Agency's (ESA) and National Aeronautics and Space Administration's (NASA) standards. The board is compatible with boards of other manufacturers and CubeSat specification.

1. Space environment

As the complexity of space systems is continuously growing, an understanding of space environment is necessary to reduce failure possibility. The neutral atmosphere is responsible for drag, glow and oxygen erosion. Magnetic and electric fields are responsible for magnetic torques and electric fields. The UV/EUV radiation creates long-term changes in material surface properties. The IR environment is the main cause of thermal effects. Also, four charged-particle environments are discussed in the chapter: the interplanetary environment, the plasmasphere/ionosphere, the plasmasheet and the radiation belts. Synthetic space debris, meteoroids, and surface dust are also in this chapter [1].

1.1. Neutral Atmosphere

This environment is present at low altitudes around most of the planets. The atmosphere creates atmospheric drag, which influences a spacecraft's trajectory. A spacecraft has to periodically adjust its orbit, otherwise, it eventually crashes or burns in the atmosphere [1].

Orbital velocities and interactions with neutral particles can induce chemical interactions such as oxygen erosion (a serious problem for Kapton, silver, osmium and other materials) [1].

1.2. Electric and Magnetic Fields

Electric and magnetic fields exist around most bodies in space. Magnetic fields range from tenths of gauss near the Earth, about 4-8 gauss at Jupiter and few nanotesla in the solar wind. Electric fields range from 0.3 V/m close to the Earth to 60 V/m near Jupiter. Spacecraft surface charging potentials can reach 20 kV at the Earth. Arcing can occur between charged surfaces with potential differences as low as 200 V [1].

1.3. Ultraviolet Radiation

Ultraviolet radiation is important for spacecraft as it can change the surface chemistry of materials and causes photoelectron emission. The ultraviolet radiation is the continuum and line spectrum between 10-4000 Å. The solar energy in this range is between 10^7 and 10^{10} photons/cm^{2}s below 1000 Å and rises exponentially to 10^{16} protons/cm^{2}s between 1000 and 10000 Å [1].

1.4. Infrared

The infrared spectrum has wavelengths from 0.7 to 7 μm and is produced by the Sun. Other sources can be atmospheric glow, radiation from other planets and reflected sunlight. This environment has major thermal effects on spacecraft [1].

1.5. Solar Wind Plasma

The solar wind is a plasma, consisting of electrons, protons, and alpha particles, produced by the Sun. Densities and energies range from 50 particles/cm^{-3} (40 eV for ions, 65 eV for electrons) near Mercury to 0.2 particles/cm^{-3} (1 eV for ions, 10 eV for electrons) at Jupiter. The solar wind must be considered for missions near the Sun and for plasma sensors. This plasma can also induce surface potentials of 10 V, but potentials up to 100 V were also measured [1].

1.6. Ionospheric Plasma

The ionosphere is a component of a planetary atmosphere. For the Earth, the composition varies from O^+ dominated (density of about 10^6 cm^{-3}) environment at altitudes from 200 to 500 km, to H^+ dominated (density from 10^5 to 10^3 cm^{-3}) for higher altitudes. The concentration is illustrated in Figure 1. A spacecraft's velocity relative to the plasma can create a charged wake structure around the spacecraft altering the currents and electromagnetic fields around it. Ionospheres affect mainly radio wave propagation and spacecraft communications [1].

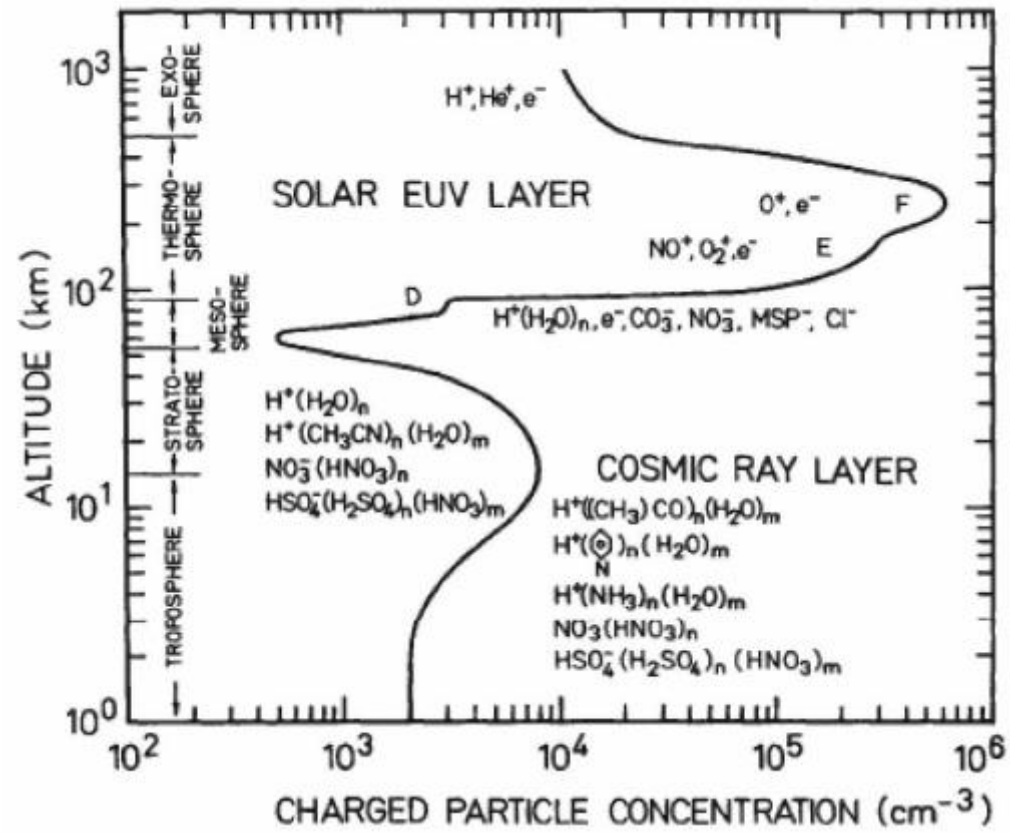


Figure 1: Concentration of charged particles in the ionosphere [2]

1.7. Aurora Plasma

Above the ionosphere, there is a plasma of lower density than in the ionosphere, but also of much higher energy. Charged particles can generate structures called auroras. Near the Earth's geostationary orbit, densities are on the order of about 1 cm^{-3} and their energies are in order of tens keV. The plasma can rise surface potentials to 20 kV or more [1].

1.8. Trapped Radiation

One of the effects of the Earth's magnetic field is to provide protection against charged particles. These particles are trapped in a barrier called Van Allen belts, discovered by first American satellite Explorer 1 [3]. The inner belt is formed in altitude from 1000 km to 6000 km, the outer belt in altitude from 13 000 km to 60 000 km. The altitudes and intensities of the belts vary based on which position on Earth they are measured from. The belts are most intense over the equator and almost absent above the poles [4].

The particles are mostly electrons and protons. Due to the high density of these particles, satellites and other man-made objects need a greater protection against radiation. On the other side, objects are less influenced by radiation below the inner belt.

In inclination, lower than 28 degrees and altitude lower than 500km, space satellites suffer from radiation dose 100-1000 rad(Si)/year. For higher inclinations and altitudes, the radiation dose increases to 1000-10000 rad(Si)/year [5].

1.9. Galactic Cosmic Rays

The galactic cosmic ray environment consists of protons and heavy nuclei with energies from 1 MeV/nucleon to 100 GeV/nucleon. Electrons are also in cosmic rays, but their amount is significantly smaller [1].

1.10.Solar Proton Events

The solar proton event generates hydrogen and heavy nuclei within energy range from 0.1 to 100 MeV/nucleon. Their intensities are usually several orders of magnitude large than of the galactic cosmic rays at these low energies. The galactic cosmic rays dominate the spectrum at energies above 100 MeV/nucleon. Solar proton events are one of the major radiation concern to spacecraft designers [1].

1.11.Meteoroids and space debris

Every spacecraft is exposed to the risk of collision with micrometeoroids and space debris. The damage depends on the size, impacted structure, and speed and direction of the impacting particle. An impact can cause serious damage and lead to malfunctions or destruction of the spacecraft. Impact velocities range from 11 to 70km/s [1].

In 2008 only 7% of objects in Earth's orbit were operational spacecraft, 41% were spent upper stages and mission-related objects. About 52% were parts from collisions and explosions. These objects can be divided into trackable and non-trackable particles. More than 500,000 particles are tracked. These particles are of the size of marble or bigger. The danger of hitting tracked particle can be minimized by choosing suitable orbit or small track adjustments [6]. The danger increases for CubeSat as they mostly do not have an engine which could be used to change its position.

The bigger danger is from non-trackable particles as they are nearly impossible to detect and there are many millions of them in orbit [7].

1.12.Dust

Dust can behave as a collection of charged particles. Comet dust environment can affect operations during flybys and/or landings. Significant dust environments are presented at the Moon, Mars, and comets [1].

1.13.Space Launchers - vibrations and acceleration

A satellite suffers from vibrations and acceleration from the lift-off of a rocket until cut off of the last engine (some satellites have their own engine to change their orbit), shown in Figure 2.

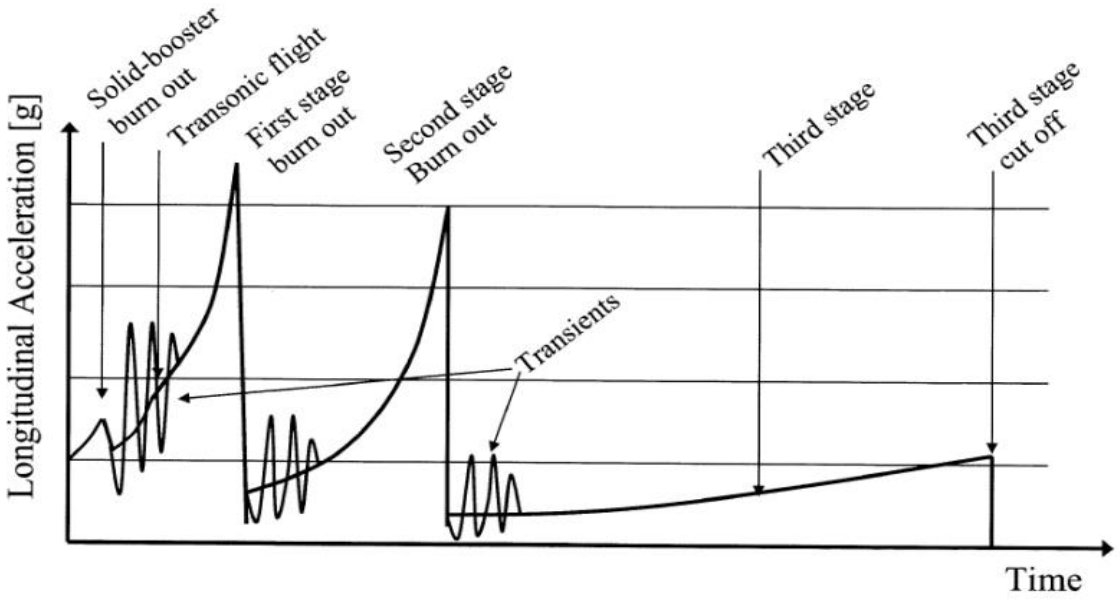


Figure 2: Steady-state and low-frequency accelerations during flight [8]

They are mostly caused by quasi-static loads, random vibrations, and shocks. They occur in different frequencies and amplitudes [8]. Figure 3 illustrates their distribution.

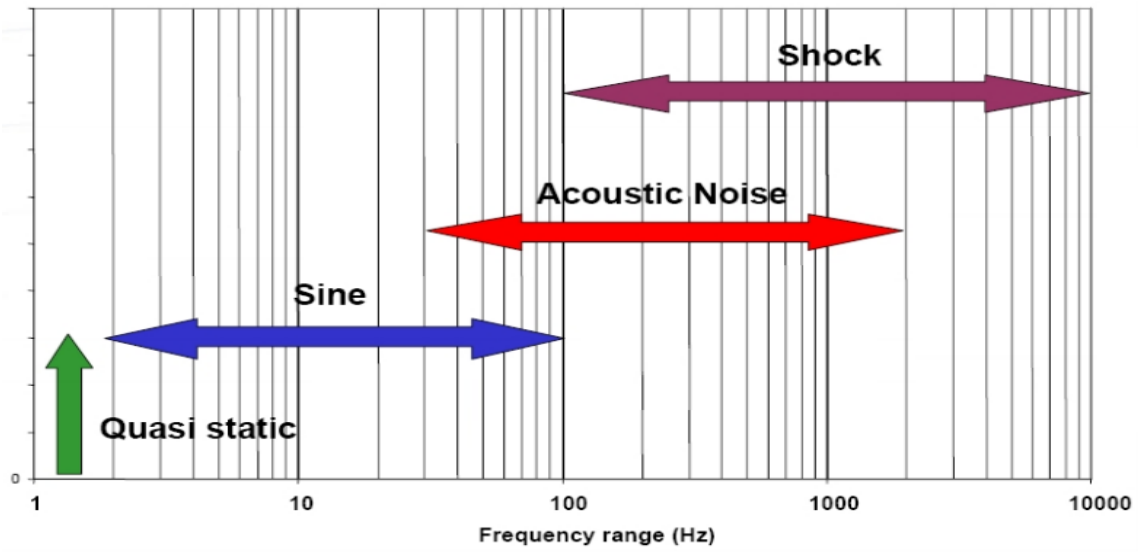


Figure 3: Typical frequencies of vibrations and shocks [8]

Quasi-static loads can be considered as static acceleration. They are a combination of acceleration of a rocket carrying the payload and low-frequency vibrations. They are mostly axial, with the highest value at stage burnout [9]. Random vibrations are mostly caused by engines of the rocket, structural responses to acoustic loads and aerodynamic

turbulences. The random means that all frequencies occur at the same time, but different amplitude. They are usually most stressing, as some frequencies can produce effective loads of tens g's [10]. Shocks are made by firing pyrotechnic mechanisms like stage separations, solar arrays deployment, and others.

1.14.Orbits

Spacecraft can orbit the Earth, Moon, and other objects (usually planets and moons). Most spacecraft have prograde orbits (they move from west to east), as it is the usual direction of rotation of objects [11].

Low Earth Orbit

Low Earth Orbit (LEO) is the lowest orbit which a spacecraft from Earth can reach. Most of spacecraft and satellites are deployed there as cost-to-orbit is the lowest. It lies in altitudes from 160 km to 2000 km [11]. Molecules in the atmosphere create a drag, which causes a decrease of spacecraft's orbit, therefore spacecraft need to periodically adjust their orbits. LEO is also the place where most of the space debris is located [12].

Geostationary and geosynchronous orbits

A geostationary or geosynchronous orbit is located at an altitude of 36,000 km. It takes the satellite 24 hours to orbit the Earth at this altitude, the satellite moves at the same speed as the Earth rotates. Geostationary satellites are orbiting above the equator in a circular orbit. Geosynchronous satellites are not positioned over the equator or have an elliptical orbit and so they appear to move across the sky. These types of satellites are typically communications or weather satellites [11].

Polar orbit

A polar orbit is any orbit in which the spacecraft passes over the rotation poles of the planet. In a polar orbit, the spacecraft can be made to follow any line of longitude. As the Earth rotates below the satellite, the satellite passes over a different region of the planet with each orbit. Polar orbits are used to map a planet or to observe specific effects relating to polar regions [11].

Sun-synchronous orbit

An orbit that passes over the same part of Earth at the same local time each day is called Sun-synchronous [11].

2. Radiation effects on electronics

The ionizing particles may generate failures in integrated circuits and semiconductor devices, as they can change a transistor state. These failures can be transient or permanent, depending on charge and location of the interaction.

The most frequent are Single Event Effects (SEE). They are considered as Soft Errors, as their effect is only temporary. The SEE can be divided to Single Event Upset (SEU) and Single Event Transient (SET). The SEU causes a change of state of a memory cell. Information, saved in the memory, is corrupted but the logic cell works normally. When new information is written, the logic cell will contain the new information unless another SEU occurs. The SET happens when radiation causes a voltage spike on an output of a circuit. The effect is only temporary, but the output can be latched during the spike and lead to serious failures. The particle can also have enough energy to interact with multiple transistors, which can lead to Multiple Cell Upset (MCU). If the corrupted bits are in the same memory, the error is named as Multiple-Bit Upset (MBU) [13]. The SEE are shown in Figure 4.

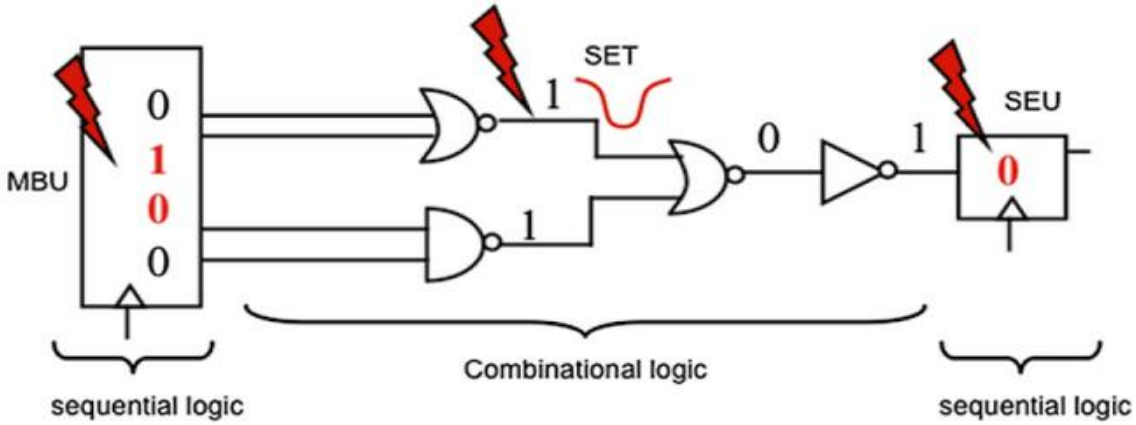


Figure 4: SEU, MBU and SET in the sequential and combinational logic [13]

Faults can also be permanent. Single Event Latchup (SEL) is caused by the opening parasitic bipolar transistors. The SEL can produce a large current between V_{CC} and ground. The power dissipation significantly increases as well as the temperature of the chip. The current can also damage nets and/or semiconductors and other parts. That can lead to permanent destruction of the IC. After the SEL occurs, the damage of the IC can be prevented by turning off the power supply [14]. Parasitic bipolar transistors are illustrated in Figure 5.

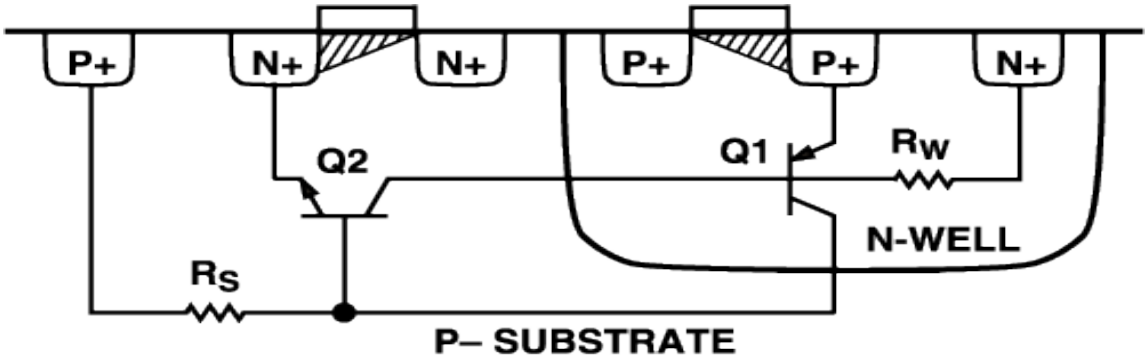


Figure 5: Cross-section of PMOS and NMOS devices, showing parasitic transistors Q1 and Q2 [15]

Single Event Gate Rupture (SEGR) is an event when radiation damages gate oxide of MOSFET transistor. It can also create conducting path through the gate. The SEGR affects mostly power MOSFETs [16]. Power MOSFETs can also suffer from Single Event Burnout (SEB). Radiation can induce current flow which opens parasitic bipolar transistor below the source. The bipolar transistor conducts short-circuit current through the MOSFET which leads to its destruction.

The sum of particle interactions is called Total Ionizing Dose (TID). In the long term, it can change part's threshold voltages, current leakage, timing parameters and other characteristics [17]. For space applications, the TID is expressed in krad(Si).

As a charged particle interacts with a material (semiconductor), it passes its energy to the material. This energy is expressed as Linear Energy Transfer (LET). The LET is described as the amount of energy the particle passes per one unit of distance and density (mostly MeV-cm2/mg). For example, the [14] shows the number of SEU events based on the amount of LET.

Electronics can be divided, based on the radiation hardness, into three groups: Commercial, Rad Tolerant, and Rad Hard. Their comparison is shown in Table 1. The commercial electronics is mostly made without any protection against radiation. The design of Rad Tolerant electronics is made in a way to provide protection against radiation, but only up to few tens of krads(Si). Rad Hard electronics is designed and manufactured for particular hardness level. The radiation protection often affects the design of the chip and also the design of its package. The electronics is tested in the radiation chamber.

Table 1: Categories of components and their characteristics [18]

Commercial	Rad Tolerant	Rad Hard
Process and Design limit the radiation hardness	Design assures rad hardness up to a certain level	Designed and processed for particular hardness level
No lot radiation controls	No lot radiation controls	Wafer lot radiation tested
Hardness levels: Total Dose: 2 to 10 krad (typical) SEU Threshold LET: 5 Mev/mg/cm2 SEU Error Rate: 10^{-5} errors/bit-day (typical)	Hardness levels: Total Dose: 20 to 50 krad (typical) SEU Threshold LET: 20 MeV/mg/cm2 SEU Error Rate: 10^{-7} - 10^{-8} errors/bit-day	Hardness levels: Total Dose: > 200 krad to >1 Mrad SEU Threshold LET: 80-150 MeV/mg/cm2 SEU Error Rate: 10^{-10} to 10^{-12} errors/bit-day
Customer performs rad testing and assumes all risk	Usually tested for functional fail only, risky	
Customer evaluation and risk	Customer evaluation and risk	

The radiation hardness also depends on the technology of the chip. Bipolar devices have significantly better hardness than unipolar (shown in Table 2). The hardness also differs for digital and analog circuits. Radiation degrades bipolar transistor's beta, which affects collector current and the operation of a circuit. It also affects transistor's input impedance, offset and gain [18].

Table 2: Radiation Hardness Comparison [18]

Technology		Total Dose Hardness [rad]
Bipolar	TTL/STTL	$1 \cdot 10^6$
	ECL	$1 \cdot 10^7$
	IIL	$1 \cdot 10^6$
	LINEAR	$1 \cdot 10^4$
MOS	NMOS	$7 \cdot 10^2$
	CMOS (BULK)	$3 \cdot 10^3$
	CMOS/RH	$1 \cdot 10^7$
	CMOS-SOS	$1 \cdot 10^6$

3. CubeSat

CubeSat are defined as U-class spacecraft with dimensions of 10x10x10 cm and weight up to 1.33 kg per unit. That is considered as one unit (U). Final CubeSat can consist of several units, mostly 1U, 3U, and 6U. An example of 1U CubeSat is shown in Figure 6. They are mostly composed of several boards; CubeSat COMPAS-1 is shown in Figure 7 as an example. Once in orbit, they are deployed from Poly-Picosatellite Orbital Deployer (PPOD) [19].

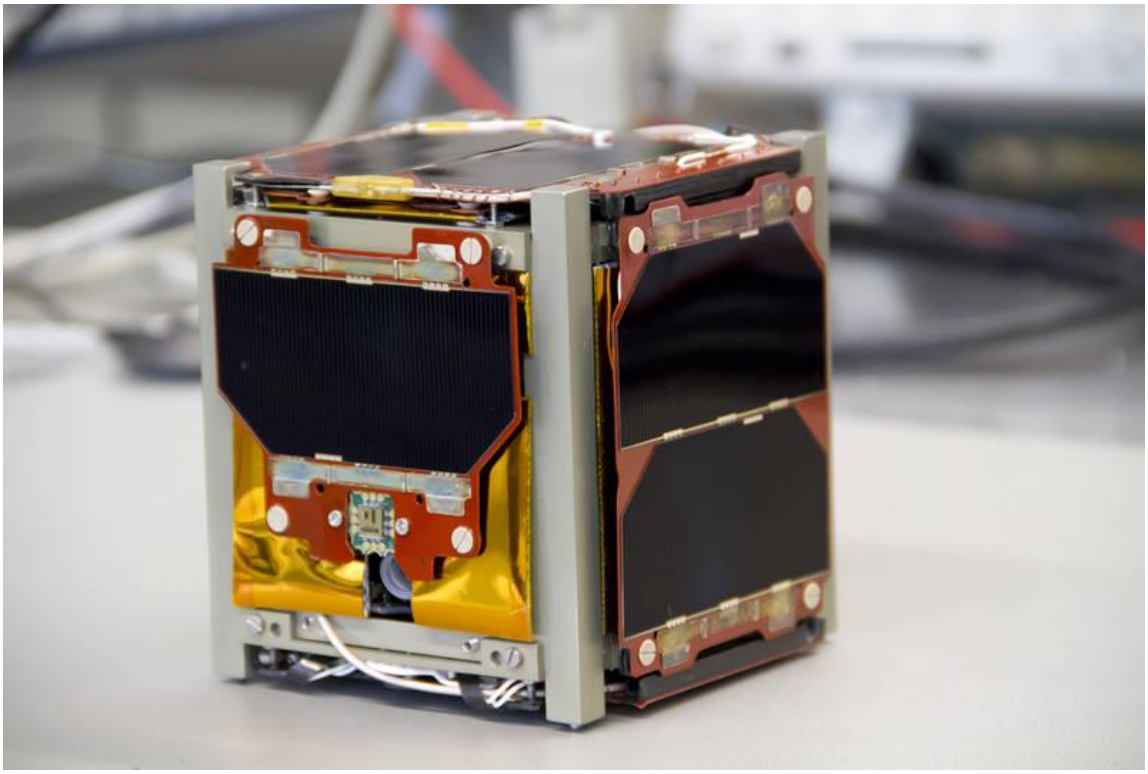


Figure 6: The First-MOVE CubeSat [20]

To reduce overall cost, CubeSat are mostly made by commercial parts. Also, they are often used to test new technologies before they are used in bigger satellites. As a disadvantage, they are usually not tested for radiation, and they are not suitable for space application outside of the Low Earth Orbit. To be suitable, every part has to go through series of tests, and their design has to be prepared for the space environment [21]. Most of CubeSat can survive only protected by Van Allen belts and even then, their lifetime is in order of moths.

CubeSat mostly use solar cells as a power source. As the surface area is small and limited, the power consumption has to be as low as possible. Some designs use bigger solar arrays which are deployed by spring or similar mechanism [22]. Solar cells are used to power electronics and often charge batteries. CubeSat use rechargeable Li-ion batteries to provide necessary power during the eclipse as well as during peak load times. Heaters are sometimes used to protect batteries against low temperatures [23].

For data handling and computing, CubeSat mostly use microcontrollers [22]. They provide sufficient computing power with low power requirements. On the other hand, they are not able to perform several tasks at the same time (sequential processing) therefore multiple of them have to be used. They also can react only to signals slower than few milliseconds [24]. As they are commercial parts, they are vulnerable to space radiation. Therefore they have to be protected by error detection and correction technique or/and redundancy.

To control an orientation of a CubeSat, different kinds of systems can be used. It can include reaction wheels, thrusters, Sun sensors, GPS receivers and others. They can be used to turn a CubeSat to face the Sun as much as possible, which increases the power generated by solar cells. Some CubeSat use a propulsion to change their position. That also helps to avoid collision with space debris. Tanks with cold gas are mostly used, but some experiments with electric propulsion and solar sails also have been made [23].

CubeSat use radio-communication systems in VHF, UHF, L-, S-, C- and X-band. Due to limited power supply, their power is usually limited up to 2W [25]. Every design has to comply radio standards and parameters of the country, where they are designed in.

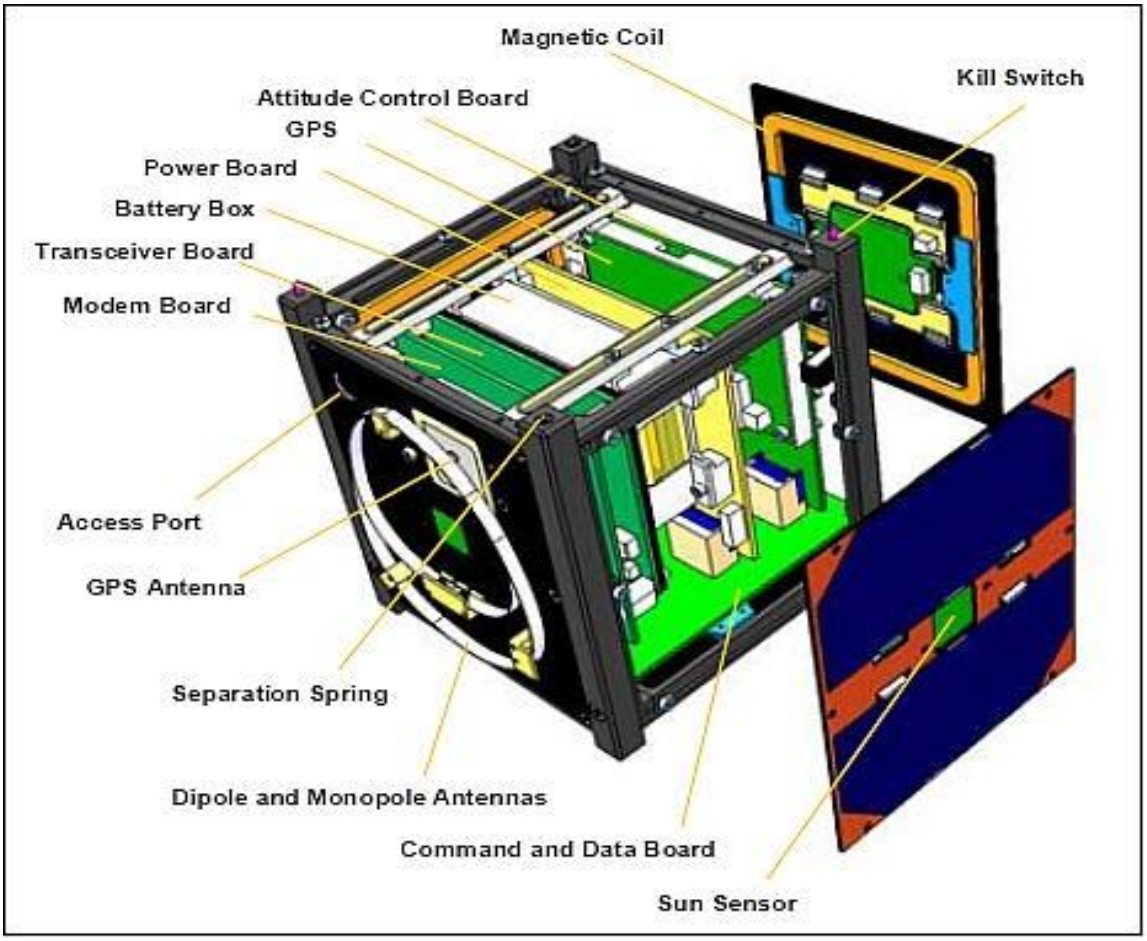
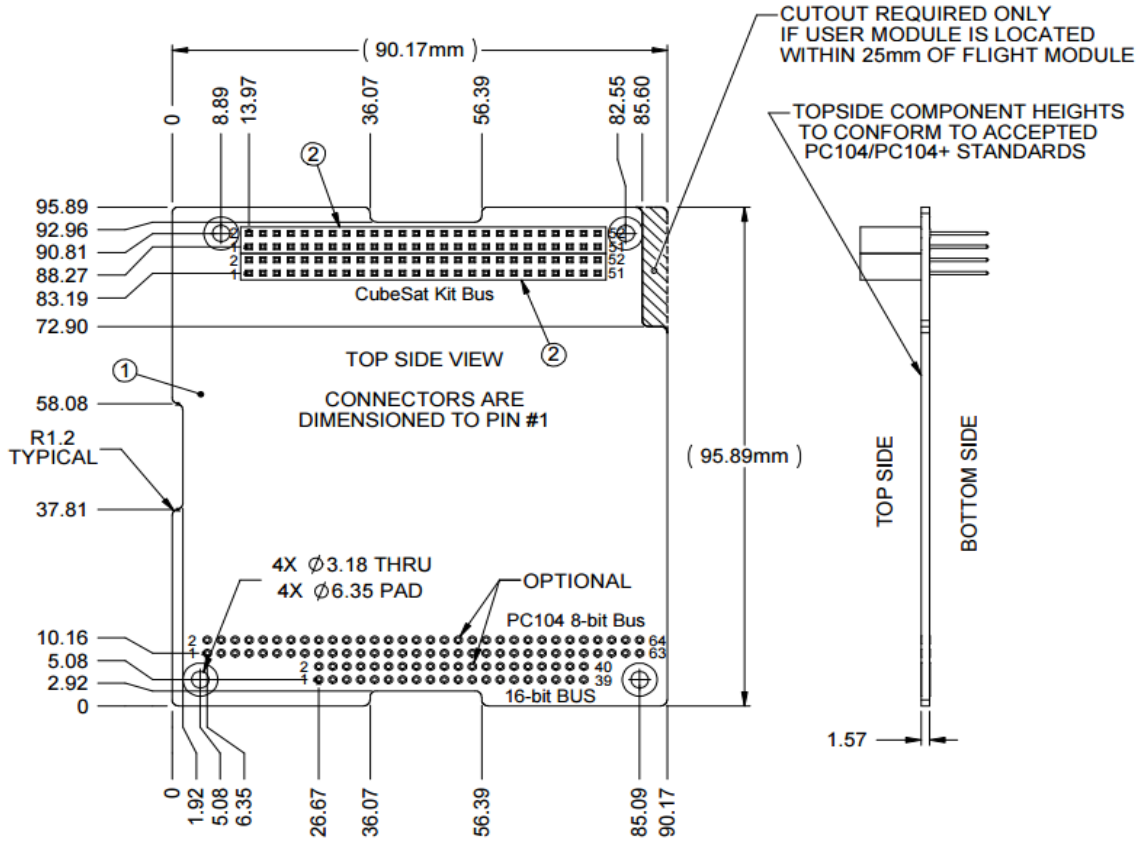


Figure 7: Configuration of the COMPASS-1 CubeSat [26]

3.1. Requirements

The CubeSat power system must be turned off while placed in PPOD. The power system consists of all batteries and solar cells. That prevents unwanted activation of any system. To achieve reliable off state, a mechanical deployment switch must be used. The switch is turned when the CubeSat is released from PPOD. If the switch is turned on and back, all circuits and timers must be reset.

As the final board for this thesis is designed to fit into one unit, it must fulfill dimensional requirements, shown in Figure 8.



ITEM	QTY	PART NUMBER	DESCRIPTION	MANUFACTURER
1	1	PC104 Spec PCB	User	User
2	2	ESQ-126-39-G-D	2x26 Stack-Through	Samtec.com

Figure 8: Required board dimensions [27]

Every board must be equipped with Samtec 2x26 Stack-Through connector to connect to other boards.

4. Design of the control unit

4.1. Design options and requirements

There are several ways to decrease the influence of the space environment. Examples range from shielding and blankets to careful component selection [1].

4.1.1. Expected environmental conditions

For each mission, expected environmental conditions must be evaluated, and the design has to fulfill all requirements. As the final application is not known, the most common is used for the design. CubeSat are usually deployed in the Low Earth Orbit, often from the International Space Station (ISS). The orbit parameters of the ISS can be used to specify the environment. The ESA provides simulation tools which can simulate all characteristics [28], discussed in the first chapter.

The CubeSat's orbit has Apogee 410 km, Perigee 402 km, orbit time 93 minutes and Inclination 52°. The simulation is shown in Figure 9. The mission duration is set to one year. The atmospheric drag slowly decreases the altitude.

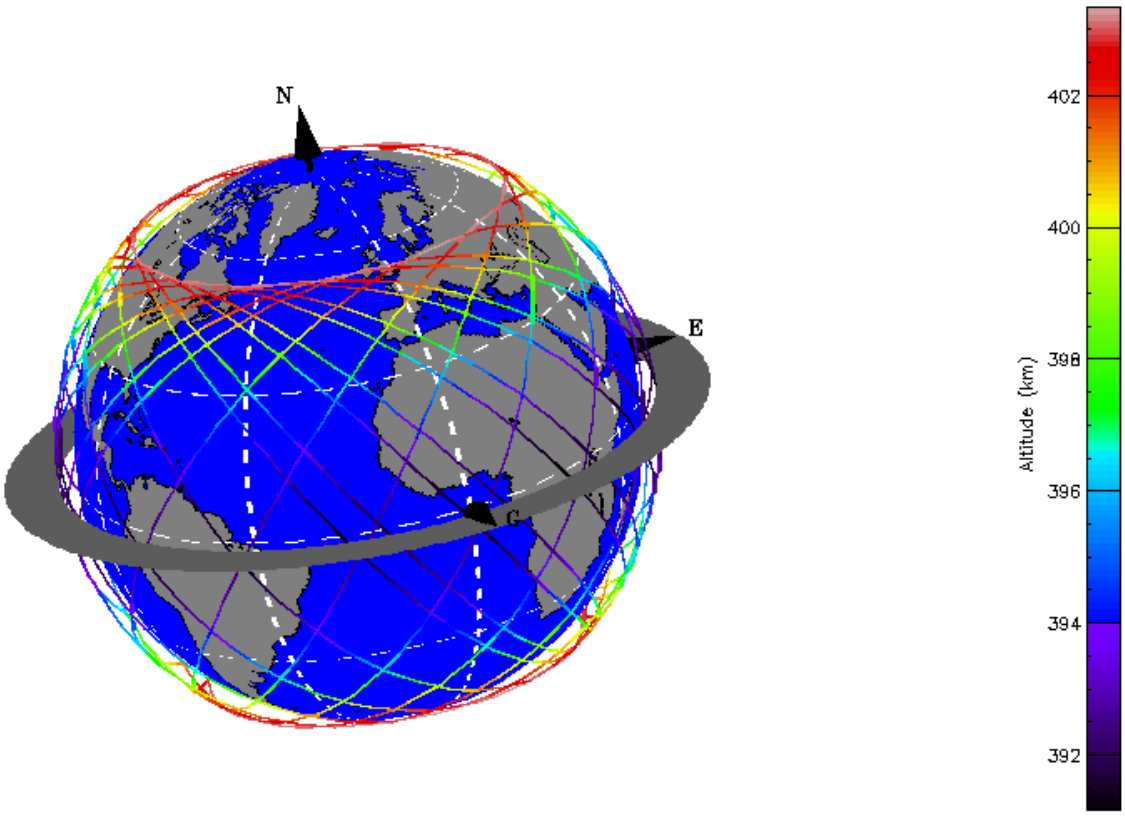


Figure 9: Simulated orbit [28]

After the orbit is set, it is possible to simulate long-term radiation dose. Figure 10 shows simulated dose based on shielding thickness. For example, measurement for XC6SLX150 (Spartan 6) shows that an SEU error is produced for dose ~13 Rad [29].

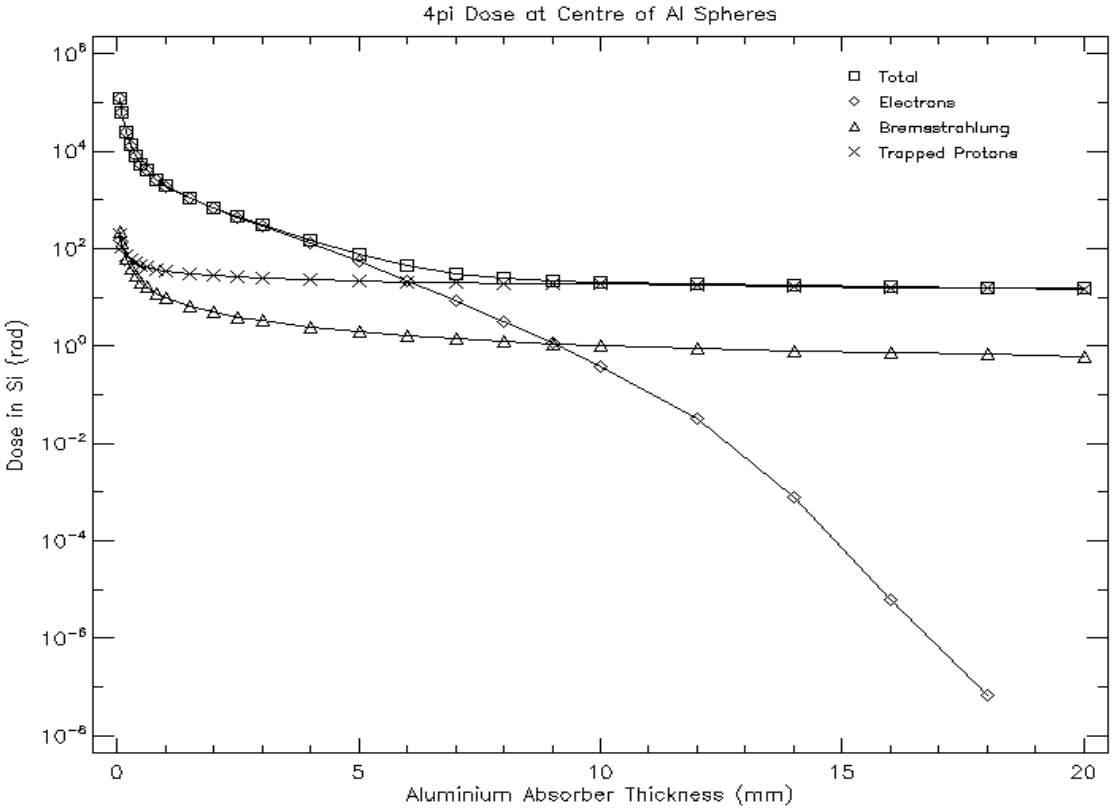


Figure 10: Expected dose rate as a function of shielding thickness [28]

Table 3 shows expected number of SEU, experienced by MOS transistor 2164, for the whole mission duration. Even thin shielding can significantly decrease the number of SEUs. Also, the device is protected by radiation belts. In geostationary orbit, the total number of bits for whole mission is about 10^6 times higher [28].

Table 3: Simulated SEU rate [28]

Effect	**Shielding thickness 0.0 mm**			**Shielding thickness 0.5 mm**		
	Bit	Bit/s	Bit/Day	Bit	Bit/s	Bit/Day
Direct ionization	$4.8 \cdot 10^{1}$	$1.5 \cdot 10^{-6}$	$1.3 \cdot 10^{-1}$	$1.4 \cdot 10^{-3}$	$4.4 \cdot 10^{-11}$	$3.8 \cdot 10^{-6}$
Proton induced ionization	$1.5 \cdot 10^{-3}$	$4.8 \cdot 10^{-11}$	$4.1 \cdot 10^{-6}$	$1.4 \cdot 10^{-3}$	$4.3 \cdot 10^{-11}$	$3.7 \cdot 10^{-6}$
Total	$4.8 \cdot 10^{1}$	$1.5 \cdot 10^{-6}$	$1.3 \cdot 10^{-1}$	$2.8 \cdot 10^{-3}$	$8.7 \cdot 10^{-11}$	$7.5 \cdot 10^{-6}$

Figure 11 shows simulated magnetic field. The CubeSat can experience magnetic field up to 0.6 Gauss.

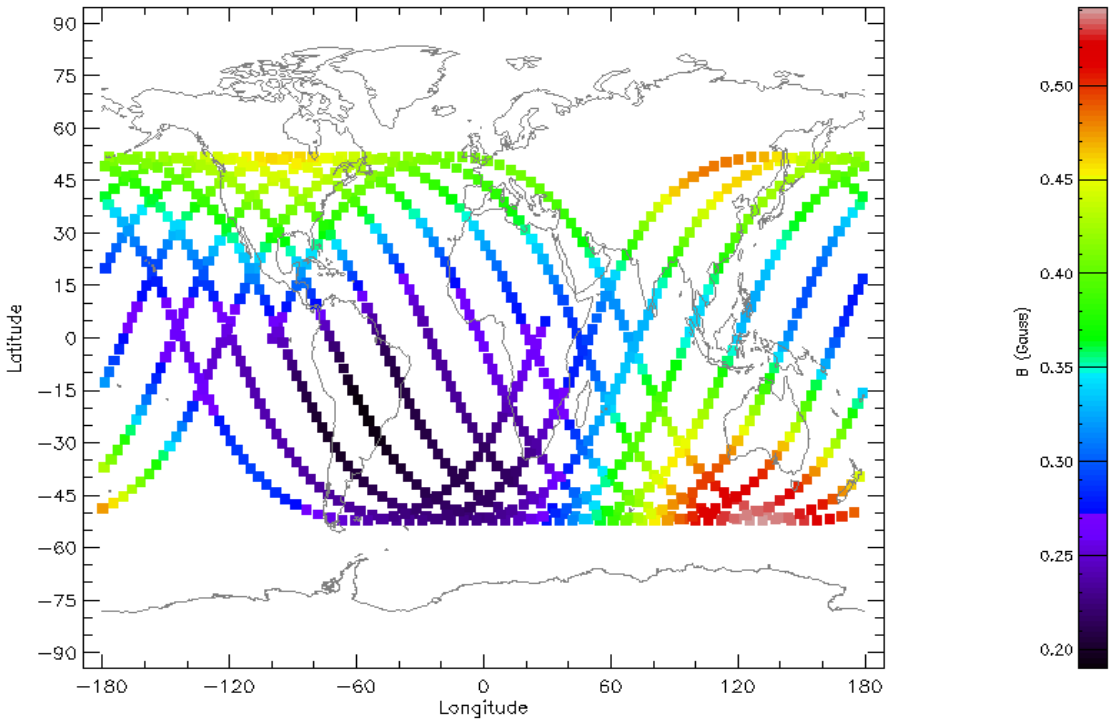


Figure 11: Simulated magnetic field [28]

Figure 12 shows a number of particles going through one square meter per year. As the number is lower than $2 \cdot 10^{-3}$ 1/m^2/year, the probability hitting the CubeSat is low and therefore an engine and/or special shielding should not be needed.

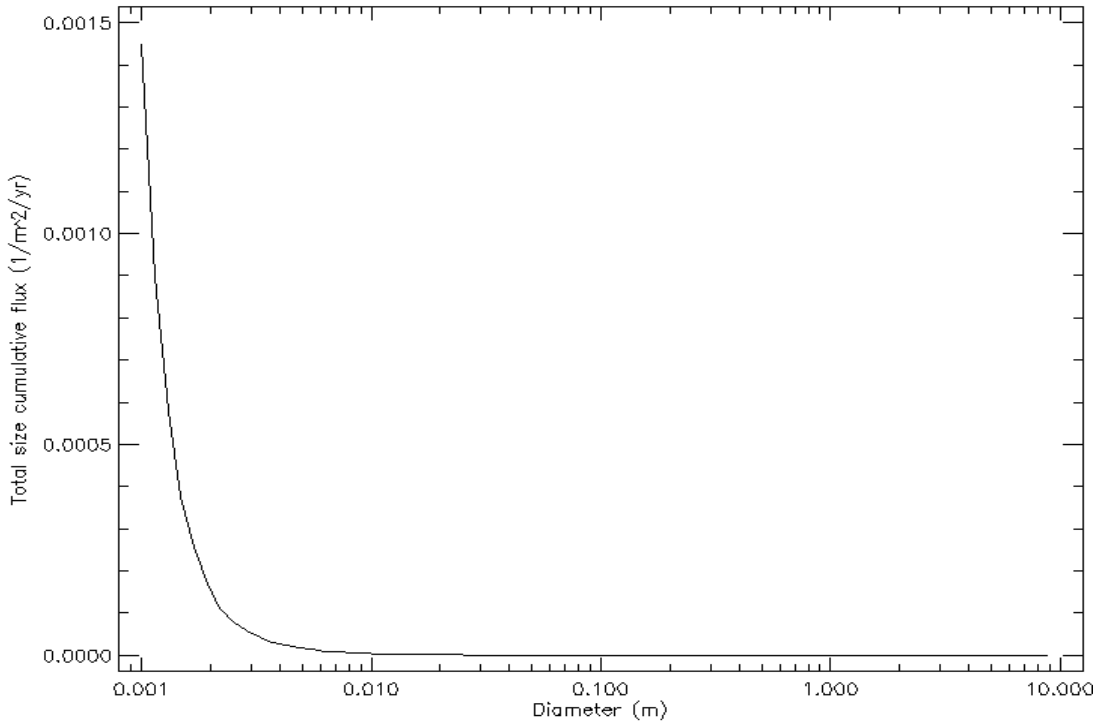


Figure 12: Simulated debris and meteoroid flux [28]

4.1.2. Shielding

One of the best methods for environmental mitigation, especially for radiation[1] and hypervelocity impacts. The first step is usually to account for the intrinsic spacecraft body shielding. If necessary, radiation-sensitive parts can be protected by bulk shielding, for example placing them into a box of high-Z materials. A spot-shield can be used when mass is a concern. Also, shielding plates can be placed between assemblies. In the case of EMC and EMI, an electrically conductive Faraday cage can be used [1].

4.1.3. Positioning and trajectory

Environmental effects are influenced by trajectory. It changes the amount of radiation, charging exposure and others. The placement or orientation of components or surfaces can minimize the effects of the environment. For example, the orientation of a surface to the velocity vector to minimize meteoroid fluence. Positioning can bring a reduction in specific fields yet has usually no impact on a system design [1].

4.1.4. Materials

Proper material selection can significantly improve the lifetime and reliability. There can be complex trade-offs between conductivity, thermal paints, and radiation sensitivity. Steps for selecting proper material are listed in [1].

4.1.5. Electronic parts selection

Electronic parts selection is a critical part of a spacecraft design. An engineer must trade cost and availability versus the class of part (commercial, military, space) and its survivability [1]. The process is discussed in chapters 2, 4.2, 4.3 and 4.4.

4.1.6. Circuit design

Circuit designs can limit radiation and thermal effects. It includes error detection and correction software, redundancy, proper layout and others. All spacecraft circuits should be tested for EMI and EMC [1].

4.1.7. PCB layout

Space environment creates surface charging potentials, as discussed in chapter 1. These effects can be mitigated by the proper layout and especially grounding [30].

[1] Figure 15 shows how the shielding affects the amount of radiation dose

4.2. Control unit selection

CubeSat mostly use microcontrollers, as well as boards only with microcontrollers are available on the market [22]. They have their advantages, but they can be unsuitable for some applications, where parallel computing or/and faster response is necessary. FPGAs can accomplish these requirements. Some aspects are shown in Table 4.

Table 4: Properties of CPUs and FPGAs [24]

	CPU	FPGA
Computation	Fixed arithmetic engines	User-configurable logic, DSP blocks, and data flow
Appropriate tasks	Decision making Complex analysis Lower data rate computation Block-oriented tasks	Compute-intensive algorithms Massively parallel operations Higher data rate computation Streaming tasks
I/O	Fixed, dedicated I/O ports	User-configurable I/O ports
Programmability	Program execution	Registers determine modes and define operating parameters
Ease of programming	C programming simplifies development tasks	HDL programming mandates hardware awareness
Maintenance/Upgrades	Less difficult	More difficult

FPGAs can react to signals in the order of nanoseconds, and they can do multiple operations at the same time. Also, their design can be uniquely made for every application. Their disadvantages are high power consumption (tens of milliamps in standby), higher price and bigger area on the board. One of the main cons is a need for separate memory for bitstream, which increases overall price and area.

Several manufacturers offer FPGAs suitable for space applications (Microsemi, Xilinx, Atmel). They are Rad-Hard, able to survive radiation up to 300 kRad(Si) without errors. On the other hand, their price can be higher than the price of the whole CubeSat, and as space grade devices, it is problematic to buy them due to ITAR regulations. Therefore, the different type has to be chosen. Commercial type offers the lowest price, but the smallest temperature range (usually 0°C to 85°C). The military type has a better temperature range (usually -55°C to 125°C) and its design is made to be as reliable as possible (sometimes as Rad-Tolerant). Its price is higher than commercial and automotive, but lower than space grade. ITAR regulation also applies.

Automotive type can be the best option. It has the same temperature range as military (-40°C to 125°C) and its design is focused on reliability. The price is only slightly higher than commercial. All parts in this design were chosen to be automotive or better.

To choose an FPGA, it is necessary to decide between antifuse and SRAM-based FPGAs. Antifuses are used to create a conductive path between logic cells and other parts. Before programming, the paths have a high resistance. After a voltage is applied, antifuses create a permanent conductive path and the FPGA is then non-volatile. On the other hand, as the programming is permanent, they cannot be reprogrammed. That brings an issue if a new design must be uploaded. Antifuse FPGAs are often used for space application, as radiation cannot change the digital circuit inside. Radiation-tolerant antifuse FPGAs are immune to SEUs and TID does not change their characteristics over time [31].

SRAM FPGAs are volatile; therefore, they have to be reprogrammed every time after its power is turned on. It brings a benefit of possibility to reconfigure them at any time. The FPGA can also be reprogrammed in orbit, therefore its bitstream can be updated or completely changed to perform different tasks. For this reason, SRAM-based FPGA is used for the board design.

SRAM FPGAs are vulnerable to radiation as it can change the FPGA's bitstream. Then the FPGA's function can change and it can lead to catastrophic failure. To prevent any faults, bitstream must be periodically checked for errors. SRAM FPGAs are also more vulnerable to SEUs than Antifuse FPGAs [31]. Table 5 shows the detailed comparison.

Table 5: Susceptibility to radiation of SRAM and antifuse PLD [32]

Susceptibility to particle radiation effects		
Resource	Antifuse/flash	SRAM
I/O	None	Low
Register	Moderate	Low
Block RAM	Very high (Very low with EDAC)	Very high
Logic cells	None	High
Routing matrix	None	High

Additional memory has to be placed with the FPGA to store the bitstream. After the FPGA is powered on, it copies the bitstream from memory and programs itself. The memory increases required area and overall price. Protection against radiation is necessary to prevent undesirable code change.

Atmel offers Rad-Hard and industrial FPGAs. Industrial FPGAs have insufficient temperature range (-40°C to 85°C) and a smaller number of logic cells (2304 cells for the biggest FPGA-AT40K40AL) [33]. As industrial, their design can be less reliable than automotive. The advantage is the use of 3V or 5V power supply, which eliminates the need for DC/DC converter.

Atmel's Rad-Hard FPGAs have a larger number of logic cells (14400 cells for ATF280F), desired temperature range (-55°C to 125°C), and they are protected against radiation. On the other hand, they need separate voltage for its core (1.8 V), use low-speed clock (50 MHz) and as previously said, their price is high.

Microsemi offers product lines for commercial, automotive, military and space applications. Its FPGAs are designed to be used in different types of applications. Some FPGAs are made for high computing power (IGLOO2, RTG4), for low power (IGLOO), with ARM cores (ProASIC3) and for mixed signal applications (Fusion). Microsemi is also the biggest manufacturer of antifuse FPGAs (RTAX, RTSX-SU, and others).

Xilinx offers product lines for commercial, automotive, military and space applications. Its main products are Spartan 6, Virtex, Kintex and Artix product lines. Its FPGAs have high computing power (thousands of configurable logic blocks), block RAM blocks, memory controllers and others features. Its FPGAs mostly have larger current consumption than Microsemi's FPGAs.

It was decided to use Xilinx's FPGA for this design. The program for digital design (ISE) is considered as more reliable and debugged. Another benefit is that its FPGAs have bigger user group than Microsemi, with more examples, sources, and advice for designs.

4.3. Xilinx FPGA selection

Xilinx offers Spartan 6 line (made in 45 nm), Artix (made in 28 nm), Virtex and Kintex (made in 28 nm, 20 nm, and 16 nm). Technologies with smaller size can suffer more from SEU but they are more resistant to radiation [34]. Main aspects of the decision were power consumption and bitstream size.

4.3.1. Power consumption

Products with a similar number of slices and logic cells from all product lines were chosen to compare power consumption; they are shown in Table 6. The main parameter was supply current for the FPGA's core (I_{CCINTQ}) as it is the biggest of all quiescent currents. As a CubeSat's power is limited, an FPGA's power consumption has to be as small as possible.

Table 6: Comparison of Xilinx's FPGAs [35]

	Part number	Slices	Logic cells
Spartan 6	XC6SLX150	23 038	147 443
Virtex	XC7VX330T	51 000	326 400
Kintex	XC7K160T	25 350	162 240
Artix	XC7A100T	15 850	101 440

The XC7VX330T from Virtex line has more than twice larger number of slices and cells, but a smaller one is not available.

Table 7 shows the current consumption for selected FPGAs. Values are specified for nominal voltage and temperature of 25°C. The Spartan 6 has the lowest consumption even for the part with the largest number of logic. Parts with less logic have smaller power consumption.

Table 7: Comparison of Xilinx's FPGAs based on power consumption [35]

	Part number	I_{CCINTQ}
Spartan 6	XC6SLX150	51 mA
Virtex	XC7VX330T	1012 mA
Kintex	XC7K160T	474 mA
Artix	XC7A100T	155 mA

As the power is one of the most important issues in the CubeSat design, the Spartan 6 product line was selected for the final design.

4.3.2. Memory

One of the biggest challenges in the design is to safely store the bitstream for the FPGA. Memory must have sufficient capacity and temperature range, but the most important is the ability to preserve data without an unwanted change. Therefore, the memory must be immune to radiation and interference. For bigger satellites and vehicles (where the price is not important), Rad-Hard memories are used. They are tolerant to radiation (up to hundreds of kRad(Si)), thoroughly tested and they have been successfully used on tens of space missions. Like Rad-Hard FPGAs, their price is too high to be used in CubeSat. The main manufacturer is 3D Plus.

Another option is One-Time Programmable (OTP) memory. The OPT memory can be programmed only once as it changes the internal circuit. Then the data are permanently saved and cannot be changed. Therefore, radiation or any interference does not have an effect on the data. Their advantage also makes an issue. As the data are permanent, the memory cannot be reprogrammed. It eliminates the possibility of uploading new bitstream. For this reason, OPT memory is not used for the design of the final board.

The best option is Magnetoresistive random-access memory (MRAM). Unlike other types of memories, MRAM uses magnetic fields to store data. It is a high-speed non-volatile memory, with low power consumption [36]. The main advantage of the design is that radiation does not affect the magnetic field. Therefore it does not change the data inside the memory. MRAM can also survive harsh environments and temperatures [37].

Table 8: Comparison of various types of memories [38]

	MRAM	**SRAM**	**DRAM**	**FLAH**	**FERAM**
Read Speed	Fast	Fastest	Medium	Fast	Fast
Write Speed	Fast	Fastest	Medium	Low	Medium
Array Efficiency	Med/High	High	High	Med/Low	Medium
Future Scalability	Good	Good	Limited	Limited	Limited
Cell Density	Med/High	Low	High	Medium	Medium
Non-Volatility	Yes	No	No	Yes	Yes
Endurance	Infinite	Infinite	Infinite	Limited	Limited
Cell Leakage	Low	Low/High	High	Low	Low
Low Voltage	Yes	Yes	Limited	Limited	Limited
Complexity	Medium	Low	Medium	Medium	Medium

The highest density MRAMs are made by Everspin Technologies. They offer MRAMs with a capacity of 128 kb, 256 kb, 1 Mb, 4 Mb and 16 Mb. 64 Mb memory is in development. Memories are available in Commercial, Industrial and Automotive grade.

Other types of memories are vulnerable to radiation and therefore cannot be used for storing the bitstream. Table 8 shows that MRAM also excels in other parameters. They are useful when large capacity is needed and some data loss can be tolerated. MRAM memory was found as the best option and is used to store the bitstream for the FPGA. Flash memory is used to store data from sensors as it has a larger capacity and is also non-volatile.

4.3.3. FPGA selection

As the final board can have various types of application, it is desired to have as many sources available as possible. It means to choose an FPGA with the largest number of logic cells. The XC6SLX150 would be a suitable choice, but the device's bitstream is too large to be stored in the MRAM (33.8 Mb). As the largest available MRAM is 16 Mb, then the XC6SLX45 with bitstream size of 11.9 Mb is the best choice. The XA6SLX45 (an automotive version of XC6SLX45) has 43,661 logic cells and 6,822 slices. The device is made only in BGA package. BGA packages are not recommended for space applications, as there is a high risk of badly soldered pins, shortcuts between pads and other issues [39]. To minimize the risk of failure, it is recommended to choose a package with the biggest pads and pitch. The FGG484 package with size 23x23 mm and 1.0 mm pitch was selected for the board. This package provides 316 user I/Os.

4.4. Enhanced products

For other electronic parts, another option is available. Texas Instruments offer Enhanced Products (EP) line. Products in this line are suitable for use in military, medical and space applications. Unlike commercial parts, they are designed for long lifetime applications (15+ years), they use a rugged lead frame, improved die attach and Au bond wires. Copper bond wires can break during high stress and they are not tested for harsh environments. Au wires have proven long term success without a failure in harsh environments.

EP are also built in one FAB, tested on the same site and have one material set for product build. It reduces the difference between parts. They also must comply more tests, which are also more challenging. For example, commercial parts are tested by Highly Accelerated Stress Test (HAST) for 96 hours while EP are tested for 250 hours [40].

EP provides lots of benefits while the price is only a few percent higher than commercial parts, but it has smaller product range. It can make a design more challenging as some required parts may not be available.

4.5. Circuit design

One of the main tasks of the board is to provide reliable FPGA reset if an error is found. An error detection has to be implemented by software. The software should decide if the FPGA can be reset, as an error in unimportant function should not reset the FPGA while critical tasks have to be done. Spartan 6 also checks the configuration memory. If the CRC is wrong, the FPGA must be reset.

The design uses two MRAM memories for storing the bitstream. The first memory is used to store proven, tested and errorless golden bitstream. The memory has a Write enable pin. The voltage on the pin can be set to zero (active mode) only by plugging a jumper in.

The bitstream is uploaded to “golden” memory before launch. Then the jumper is unplugged and as the Write enable pin is permanently connected to V_{CC}, the bitstream cannot be changed. This solution provides reliable bitstream storage.

The second MRAM can be used to store a new version of the bitstream. It can be deleted, changed or uploaded during flight. Storing a user data is also possible.

Block diagram of the final board is shown in Figure 13.

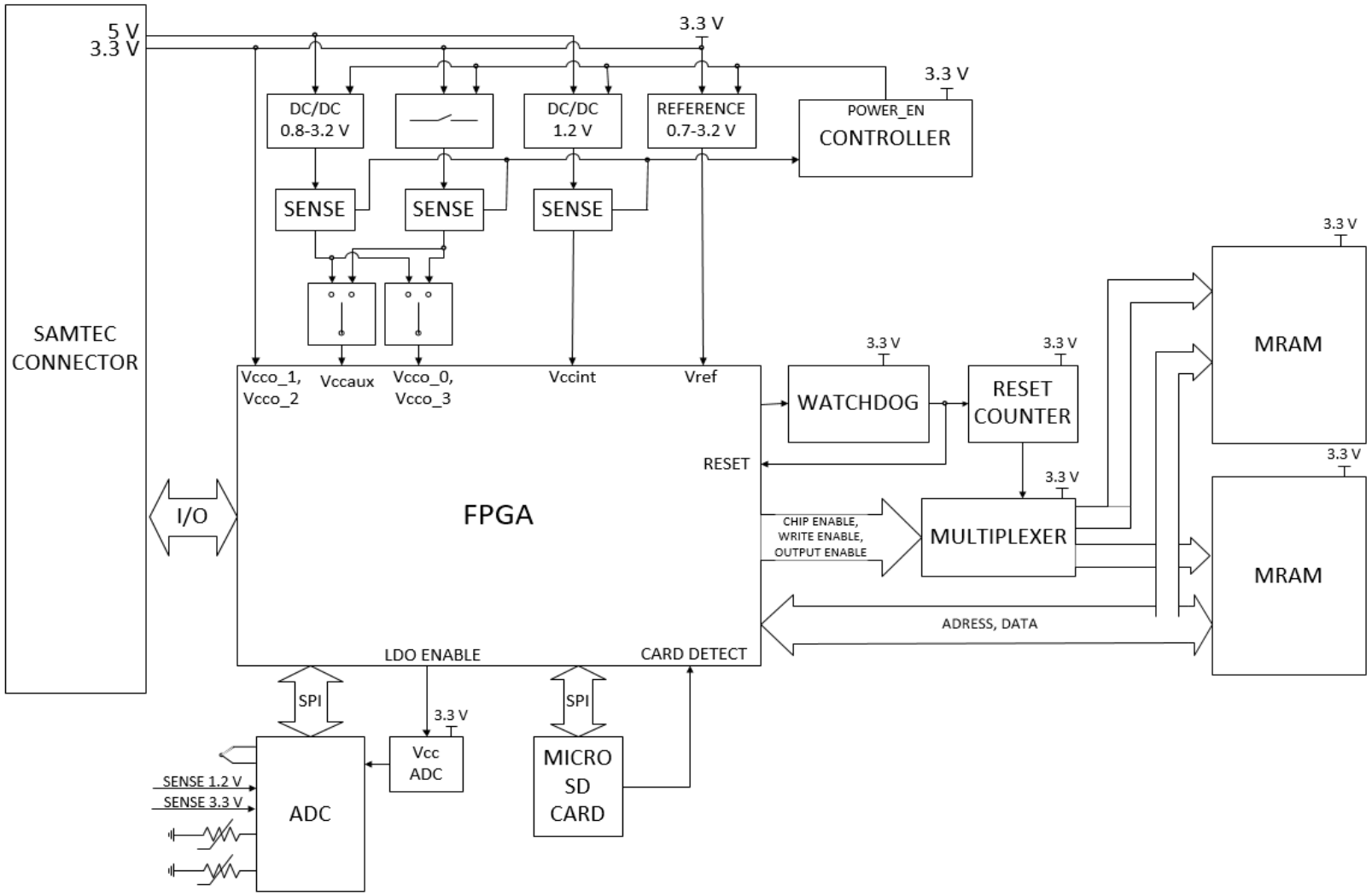


Figure 13: Block diagram of the control unit

4.5.1. FPGA configuration circuit

The FPGA must periodically produce a pulse on the WDI pin of the watchdog circuit (TPS3813K33MDBVREP). The pulse (longer than 3 us) must occur more often than 2 seconds but also less often than 25 ms. The signal goes through the buffer gate (SN74AHCT1G126). The buffer gate has Output Enable pin, which is controlled by INIT_B from the FPGA. After the FPGA is programmed, CRC is periodically carried out. If an error is found, the INIT_B is set to zero. That disables the buffer and the pulse cannot get to the watchdog.

If the FPGA stops producing the pulse (by error or command) or the CRC sets INIT_B to zero, then the watchdog timer resets the FPGA. Afterward, the FPGA is configured from the second MRAM. There can be an event when the configuration from the second MRAM fails. The reset can take place while uploading the bitstream, new code can incorporate an error and other faults. The FPGA can be stuck in reconfiguration loop and the whole CubeSat is unusable. To prevent this outcome, the board uses a shift register (SN74HC595) to count the number of configuration cycles. If the FPGA is reset three times in a row (the shift register needs two input pulses to shift the value), the shift register switches the multiplexer (SN74LV4053) to select the first MRAM with the golden bitstream. The whole process is illustrated in Figure 14. The multiplexer has a jumper on the Select input. Before the launch, when the golden bitstream has to be uploaded, the jumper ties the Select input to 3.3V. Only then the first MRAM can be accessed. Afterward, the jumper must be put into the other position to connect the Select input of the multiplexer to the output of the shift register.

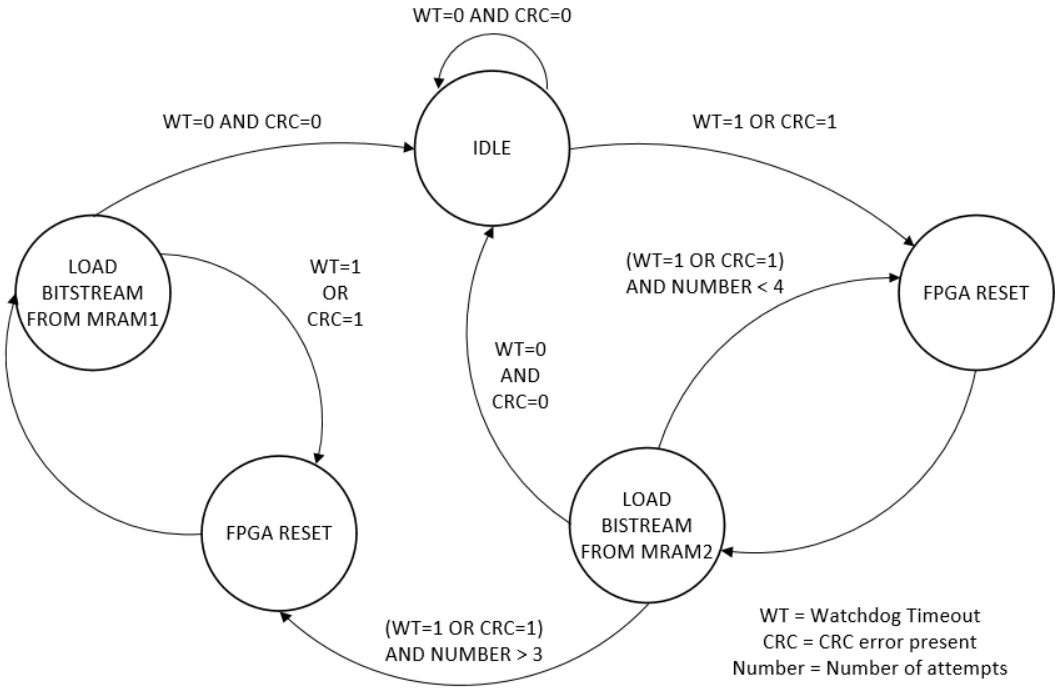


Figure 14: Configuration diagram

All Data and Address signal are connected together; the multiplexer controls the MRAMs by signal Chip Enable, Output Enable, and Write Enable. A smaller multiplexer is needed than if all signals are switched. The MRAMs are switched in order of few hundreds of nanoseconds after the reset, while the FPGA needs at least 10us to start configuration [41]. The time window is sufficient to safely switch the signals. On the other hand, the default configuration clock is set to 2 MHz. Time needed for configuration is:

$$t_{CONFIG} = \frac{1}{clk_{CONFIG}} \cdot \frac{BITSTREAM}{8\ bits} + t_{STARTUP} \tag{4.1}$$

$$t_{CONFIG} = \frac{1}{2 \cdot 10^6} \cdot \frac{11.9 \cdot 10^6}{8} + 10^{-3} \cong \underline{0.76\ s}$$

where clk_{CONFIG} is configuration clock, BITSTREAM is the size of bitstream divided by 8 (MRAM has 8 data bits in parallel), and $t_{STARTUP}$ is the time, until the FPGA starts configuration (defined primarily by ramp time of power sources).

As the watchdog timeout is 2 seconds, the configuration is fast enough to prevent the timeout. The frequency can be set up to 40 MHz if needed [41].

The pulse from the FPGA moreover resets the shift register. Such a solution increases the reliability of the circuit, as a chance of a change of the output by radiation is minimized.

When the board is powered for the first time, both memories are empty and the FPGA cannot load the bitstream. Therefore, programming the memories is not possible. Fortunately, the Spartan 6 provides the possibility to be programmed by JTAG. JTAG has to be used to program the FPGA and then the bitstream can be uploaded to the MRAMs. For this case, the watchdog must be disconnected by removing 0 Ω resistor on its output. Otherwise, the FPGA cannot be programmed as it is periodically reset before the bitstream's upload is finished. There is no need to use JTAG after the memories are programmed.

Proposed circuit is shown in Figure 15.

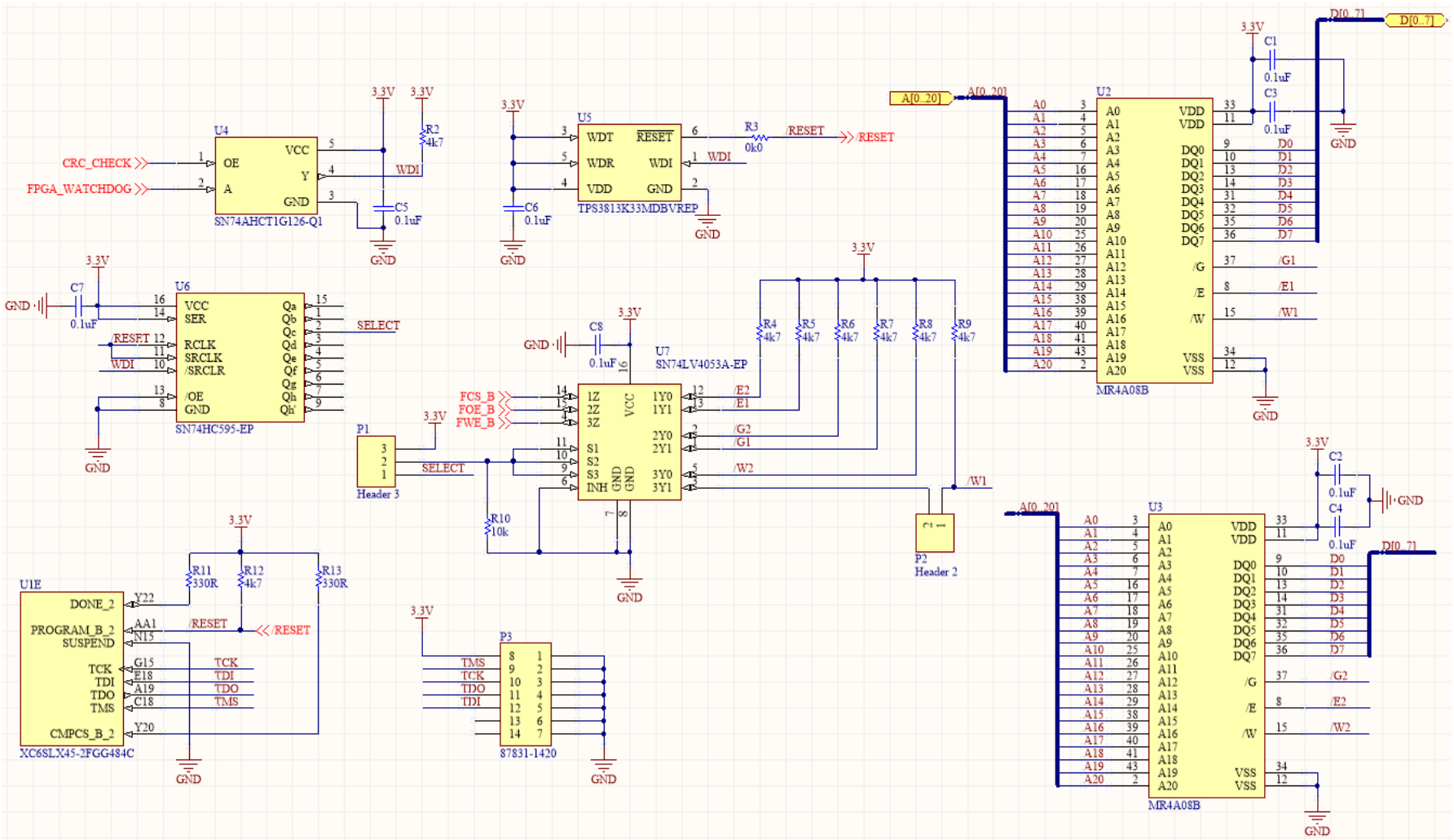


Figure 15: Schematic of the configuration circuit

4.5.2. Power supply

The CubeSat specification requires that all boards must have standard interface connector. The connector's layout gives information that 5 V and 3.3 V are available as a power supply [42]. These voltages are active immediately after a CubeSat is switched on. A CubeSat should also provide additional 5V and 3.3V rails, which can be turned on by a command from the control unit. As only the FPGA can control them, they cannot be used for powering it.

The connector has a current rating of 3 Amps per pin. Each of main voltage rails uses two pins, but the design cannot ensure that the current does not go just through one pin. Therefore, the peak current value must be lower than 3 Amps.

4.5.2.1.Power for the FPGA's core

The Spartan 6 needs a different power supply for its core and I/O banks. The power consumption for its core depends mainly on logic usage. Xilinx offers a Power Estimator (XPE) which allows estimating all currents, temperature, and on-chip power. As the final application is not known, the XPE was used to assess the worst case. With the maximum logic used, 25,000 LUTs and 50,000 FFs with 50 MHz clock, the core needs a current of 2.4 Amps. Texas Instruments offers few EP DC/DC converters; however, their packages are too large to be used. Converter LMZ10504EXT was selected, as it passed EMI tests and military tests for vibration and drop. The converter has maximum output current 4 Amps, but can be changed to LMZ10505EXT with output current 5 Amps without any modifications.

To decrease the current through the connector, the converter uses 5 V as the input voltage. The converter has efficiency better than 80 %; input current can be calculated:

$$P_{OUT} = 0.8 \cdot P_{IN} \tag{4.2}$$

$$V_{OUT} \cdot I_{OUT} = 0.8 \cdot V_{IN} \cdot I_{IN} \tag{4.3}$$

$$1.2 \cdot 4 = 0.8 \cdot 5 \cdot \mathrm{x}$$

$$\underline{\mathrm{x} = 1.2\ Amps}$$

where P_{OUT} is output power, P_{IN} is input power, 0.8 is the converter's efficiency, V_{OUT} is the output voltage, I_{OUT} is the output current, V_{IN} is the input voltage and I_{IN} is the input current.

The input current is low enough not to damage the connector. The design was calculated using part's datasheet [43] for optimized ripple and transient response. The FPGA's core needs 1.2 V, the range of 1.14-1.26 V is allowed. Start-up time was set to 10 ms. The schematic of the converter is shown in Figure 16.

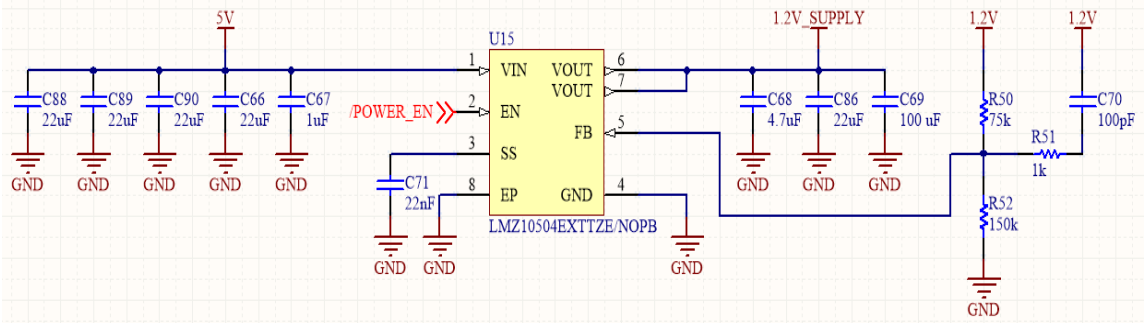


Figure 16: Schematic of the DC-DC converter

4.5.2.2.Power supply for the FPGA's I/O banks

The Spartan 6 needs a separate power supply for I/O banks. The voltage depends on an I/O standard; the voltage can vary from 1.2 V to 3.3 V. Therefore, an adjustable voltage source is a must.

From the power estimation, the power consumption of I/O banks should not be higher than 3 Amps. Same DC/DC converter as for FPGA's core was selected to simplify the design. Output voltage can be changed in range 0.8 V to 3.3 V by changing resistor R55.

As other components on the board use 3.3V logic, V_{CCO_1} and V_{CCO_2} banks are permanently connected to 3.3V power rail and cannot be changed. It secures proper logic levels for communication with memories, ADC and other parts on the board. V_{CCO_0} and V_{CCO_3} banks have a jumper, which allows a user to select either 3.3V power rail or adjustable output from the converter. Selecting 3.3V power rail ensures same voltage potential for all banks, simplifies the design and space on the board (the converter can be removed) and decreases overall power dissipation, generated by the converter.

If different logic levels are not needed, all banks can be connected to the 3.3V power rail, the converter can be connected to V_{CCAUX} and set to 2.5 V. It decreases V_{CCAUX} current by 40 %. Otherwise, the V_{CCAUX} must be connected to 3.3V power rail as it can work only with 2.5 V and 3.3 V.

Final circuit is shown in Figure 17.

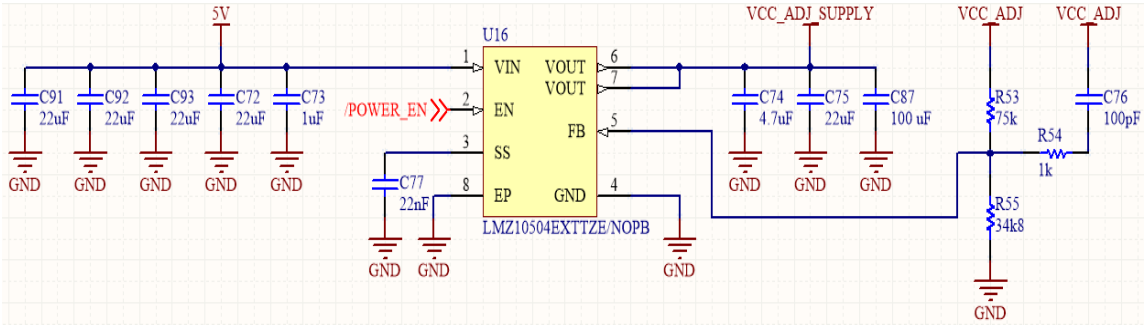


Figure 17: Schematic of the power supply for I/O banks

4.5.2.3.Reference voltage

As some protocols also need a voltage reference for proper operation, an adjustable LDO is necessary. The need for current from the reference is negligible and therefore a small IC with low driving capability can be used. The board accommodates TPS76201, which is an Ultra-LDO with current capability up to 100 mA. Its output voltage can be set in a range from 0.7 V to 5.5 V with dropout voltage about 100 mV.

Final circuit is shown in Figure 18.

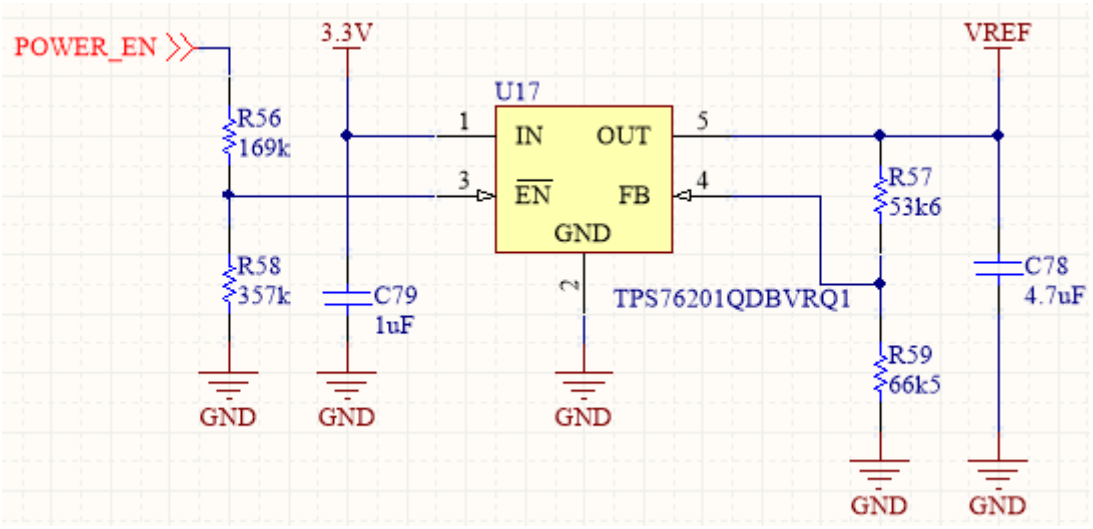


Figure 18: Reference voltage source

The power supplies are enabled by POWER_EN signal. It uses 5V logic, but the TPS76201 can survive only voltages up to V_{IN}. The input divider is used to decrease the Enable voltage.

The reference might be needed just on specific I/O banks; therefore, the voltage is connected through 0 Ω resistors. A user can disconnect the reference by removing these resistors.

4.5.3. Latch-up protection

As previously discussed, SEL can permanently destroy an IC. Some sort of protection is a must.

The task of the protection circuit is to protect the FPGA. Protecting other devices would require large circuit and would significantly increase necessary space and overall cost. Also, if the FPGA and power supply are not harmed, the board can still work and do most of its tasks even when all other parts are destroyed.

The circuit consists of sense resistors, amplifiers, comparators and supervisor circuit. The resistors are connected to 3.3V, 1.2V and ADJ supply rail for the FPGA. The resistors were selected to be 5 mΩ, as a bigger voltage dropout could cause malfunctions (supply voltage lower than needed). In 1.2V and ADJ supply rails, the resistors are placed before

voltage dividers to produce a stable output voltage, as the regulators compensate the voltage across the sense resistors.

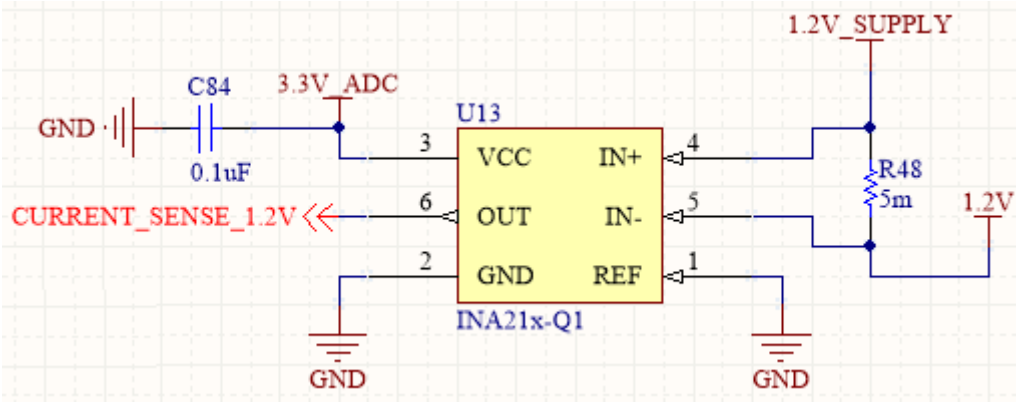


Figure 19: Sense circuit

The voltage across the sense resistors is amplified by op-amps INA214 (shown in Figure 19). Each op-amp has gain 100, and their output is connected to comparators LM2902-EP. If a comparator's input voltage is higher than the reference voltage, the comparator changes its output to log.0. If the voltage on any Sense input of the supervisor (TPS3307-18) is in log.0, the supervisor disables all power sources. Power sources are enabled when SEL is removed. The supervisor circuit is shown in Figure 20.

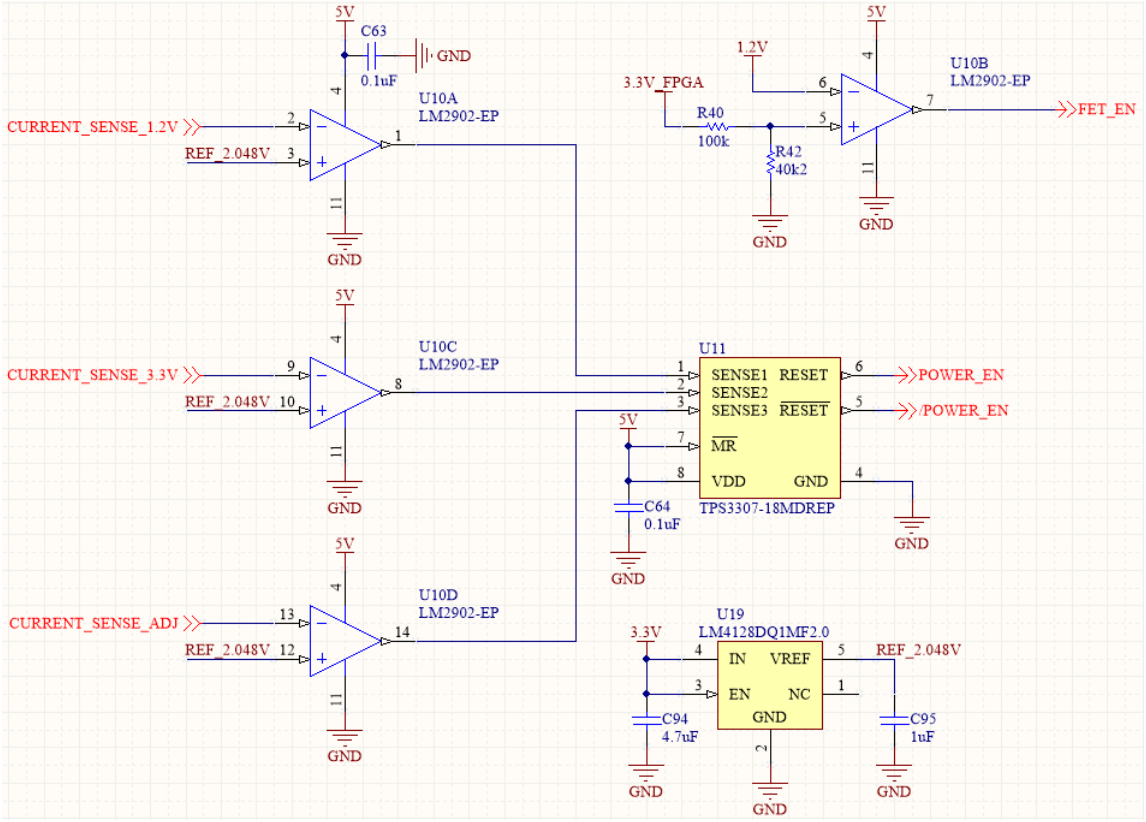


Figure 20: Schematic of the supervisor circuit

3.3V power rail is produced outside of the board, therefore a PMOS transistor is used to switch the rail on/off. The allowed voltage range is small, so power transistor with ultra-low R_{DS} is a must. Also, the transistor must be fully opened at V_{GS} of 3.3 V.

The requirement for voltage ramp brings an issue with switching the PMOS. Providing a voltage with a ramp on the gate of the transistor is not a suitable option. The transistor would be closed until the voltage reaches threshold voltage of the transistor. Then the output voltage rises almost immediately to the supply rail. The ramp time of the voltage cannot be guaranteed. To provide desired ramp time, some feedback is necessary.

The opamp LM2902-EP uses 1.2V power rail as input. When power is enabled, the 1.2V rail rises with stable ramp time. The op-amp compares the power rail with the output of the PMOS and changes its output to achieve same value. Connected resistors divide the PMOS's output by 2.5. The reason is to have output voltage 3.3V when the input voltage is 1.0V. It decreases the ramp time, but the output is immune to any interference on the input. Figure 21 and 22 show improved circuit and its simulation.

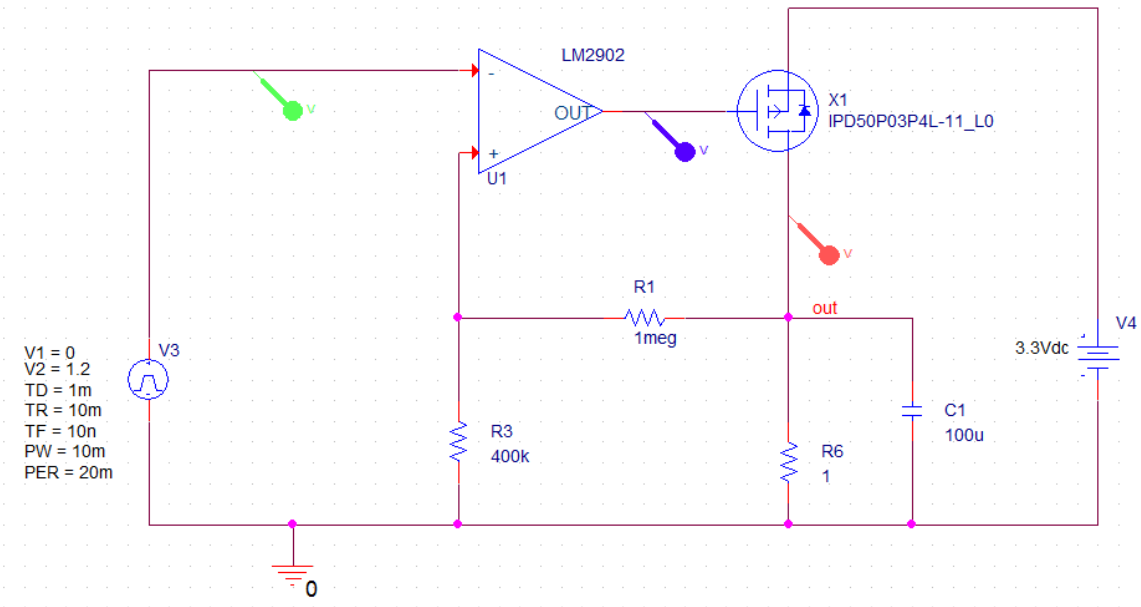


Figure 21: Improved circuit

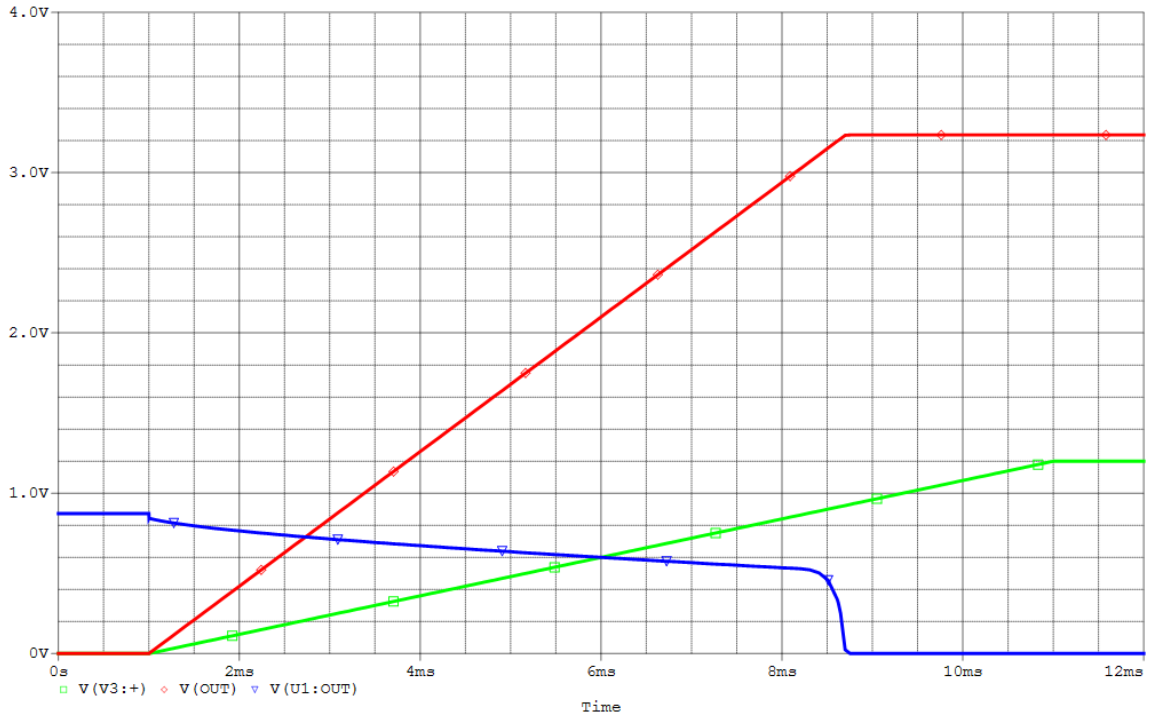


Figure 22: The input and output voltage

4.5.4. Capacitors for supply rails

The FPGA needs specific capacitors for all supply rails and each bank. These capacitors and recommended layout are specified in the FPGA's datasheet.

4.5.5. Clock generator

The FPGA needs an external clock for operation. A CMOS MEMS oscillator was selected, as this type is the only one with desired temperature range. Also, it usually has a smaller package.

The DSC1101 oscillator with 50MHz frequency was selected. It is qualified to MIL-STD-883, which means excellent shock and vibration immunity and reliability.

4.5.6. Data storage

The board uses microSD card as main data storage. Using card brings benefits of bigger storage for data and simpler communication over SPI. That also means the significantly lower number of signal lines than for parallel communication.

MicroSD cards have great shock, vibration, humidity and magnetic immunity. The connector has a detect signal, which checks if the card is plugged in. The FPGA can check if the card is connected correctly before sending data.

The main problem is the temperature range. As MicroSD cards are capable surviving a temperature range from -25°C to 85°C [44], it decreases overall board usability. Other parts are selected to work in the range up to 125°C.

If the temperature is a concern and if there is no need for storing a large amount of data, one of the MRAM memories can be used as storage. A user can store data to MRAM without changing the circuit, the principle works the same way as storing new bitstream. The main disadvantage is that the board loses the ability to have two bitstreams. Also, the reconfiguration takes more time, as the circuit first tries to load bitstream from MRAM with user data. After it fails, it loads the golden bitstream.

4.5.7. AD converter

The main way how parts dissipate their heat is through heat convection with air. This way is not present in space vacuum; therefore the power dissipation is a big concern. The most important parts' temperature should be periodically checked and some measures must be done if temperature achieves threshold value.

The parts with the highest dissipations on the board are the DC/DC converters and the FPGA. The converters have internal temperature sensors, which shut them down in a case of high temperature, yet another sensor can warn the FPGA early and some measures may be used. The ADC has two thermistors, which measure temperature on the board. As the main heat transfer in space is by conduction, a thermistor placed close to a part can sense the part's temperature. One of the thermistors should be placed near the FPGA as close as possible. The ADC also has a connection to thermocouples, which can be attached to any part on the board (or whole system). For example, it can be attached directly to the FPGA's package, measuring the temperature more accurately. A thermocouple measures only temperature difference, therefore one of the thermistors should be placed as close to thermocouple's terminals as possible to get the reference value. The circuit is shown in Figure 23.

The ADC also measures the voltage on the current sense circuits, so the current consumption on 1.2V and 3.3V power rails can be calculated:

$$V_{SENSE} = \frac{V_{CURRENT\_SENSE}}{GAIN_{INA214}} = \frac{V_{CURRENT\_SENSE}}{100} \tag{4.15}$$

$$I_{RAIL} = \frac{V_{SENSE}}{R_{SENSE}} = \frac{V_{SENSE}}{5 \cdot 10^{-3}} \tag{4.16}$$

where V_{SENSE} is the voltage on the sense resistor, $V_{CURRENT\_SENSE}$ is the output voltage of the INA214 op-amp, $GAIN_{INA214}$ is the gain of the INA214 op-amp, I_{RAIL} is the current through the sense resistor and R_{SENSE} is the resistance of the sense resistor.

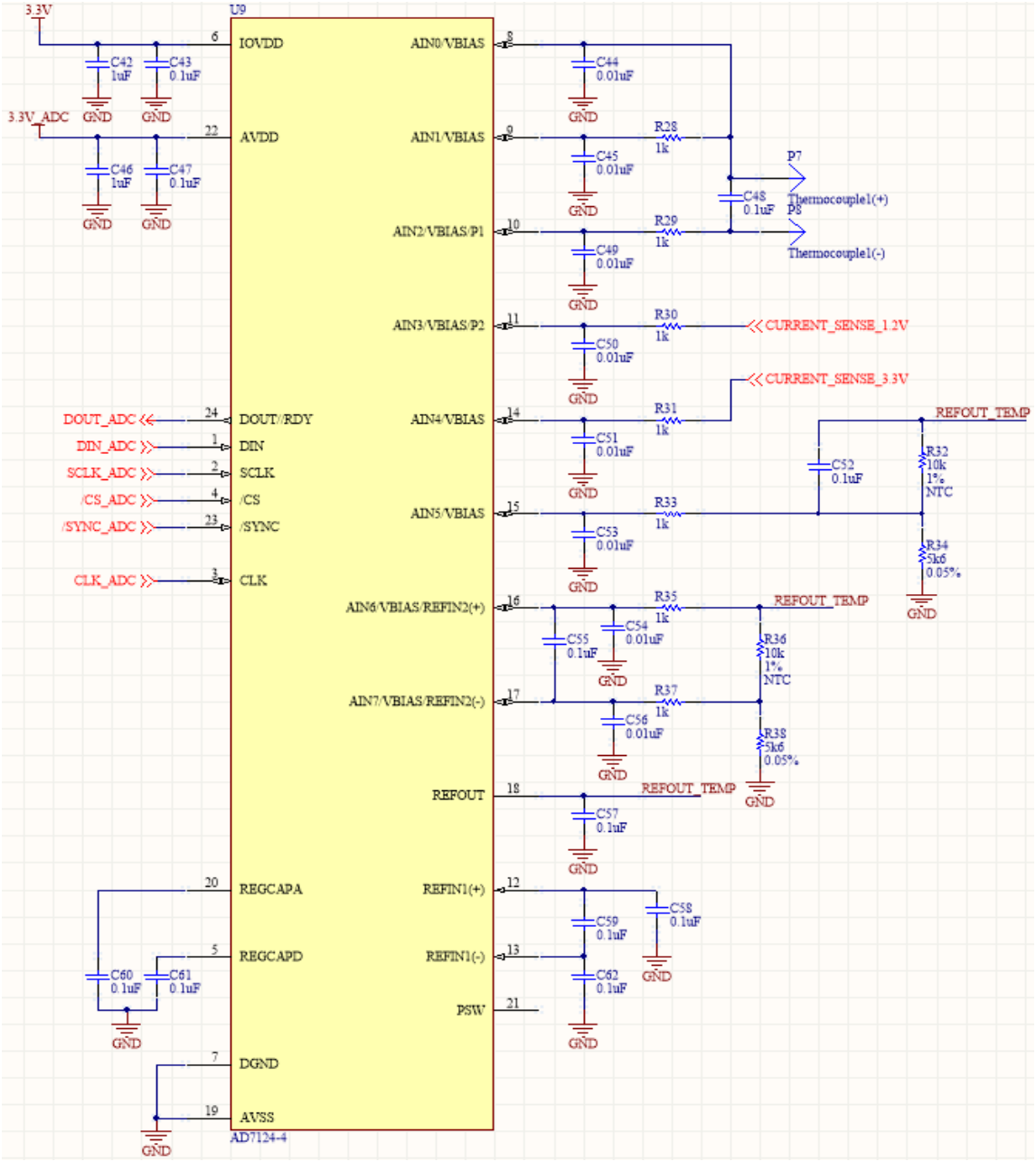


Figure 23: Schematics of the AD converter

5. PCB design

The PCB dimensions were designed according to CubeSat specification, described in chapter 3.1. The FPGA was placed as close to the I/O connector as possible to allow high-speed signals. The same reason was for placing oscillator and configuration circuit close to the FPGA.

Almost every part is placed on the top side of the board as it allows soldering by reflow. Only capacitors for the FPGA and the MRAMs are placed on the bottom side. It improves noise reduction and overall performance.

The PCB has copper pour in all layers, which improves shielding and heat conduction. The exception is the top layer under the FPGA. The copper plane can cause assembly issues, therefore is not used for this version. If the proper assembly can be ensured, the design can be easily changed. Top and bottom layer are connected to the GND and interconnected using via stitching. The board is shown in Figure 24.

Parts were assembled in vapor phase oven at Department of Microelectronics.

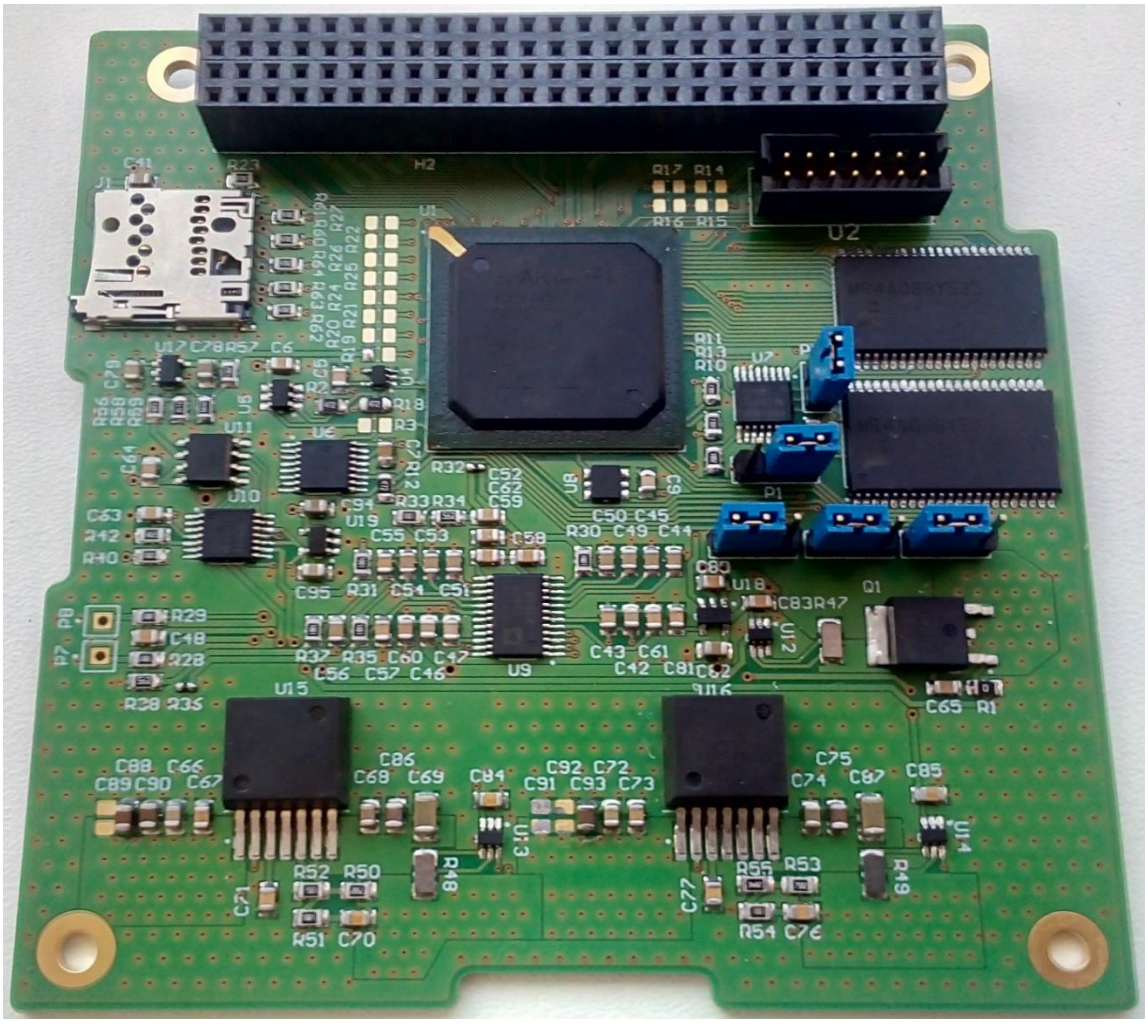


Figure 24: Final board

6. Price

The bill of materials is shown in Annex C. The overall price of the component is below 200 euro and price of the PCB is 67 euro [45]. Average control unit costs 4500 euro [22]. The unit proposed in this thesis brings significant cost reduction.

7. Digital design

As the aim of this thesis is hardware design, the main purpose of digital design is to demonstrate the unit's capabilities and test its functionality. Therefore, the Software-Implemented Error Recovery, Profile-Guided Code Transformation, and other techniques are not implemented. Using these techniques improves error mitigation and SEU protection [13].

The unit communicates with the user over UART, with one stop and start bit, no parity bit, and frequency 115200 bauds. The frequency can be easily changed in the code.

7.1. TOP Module

The TOP module is mainly responsible for communication with the user and between other modules. It accepts requests from UART and sends responses. It also checks correct temperatures and voltages and resets the FPGA in the case of limit values.

7.2. MRAM Controller

The MRAM controller is responsible for interaction with MRAM memories. It can erase the memories, write and read user data, and store bitstream for FPGA's configuration. The complete state machine is shown in Figure 25.

The write mode is selected by command 57_{16}. Then the user sends three bytes to select desired address. The controller sets the address on output and waits for a data byte. The writing process is carried out in several steps, each of them lasts for 5 µs. In the first step, the Chip Enable is pulled down to enable the MRAM. In the next step, the data byte is set to output and Write enable is pulled down. The controller waits another step to ensure the data are written properly. The „success" byte 53_{16} is sent to the user at the end of the write cycle.

The bitstream store mode works in a similar way. The mode is selected by command 42_{16}. The controller sets the address to zero and waits for two FF_{16} bytes which signalize the beginning of bitstream. Then the controller increments the address every time a new byte is written. The write cycle ends when the address gets to value $16A673_{16}$, which is

a fixed size of the bitstream, and the „success“ byte is sent. The bitstream must be binary, without swapped bits, and without compression.

To erase the memory, the user sends command 45_{16}, the controller sets the address to zero and writes 00_{16} byte. Then increments the address and repeats the cycle. The process is finished when the address reaches the end.

The read mode is selected by command 52_{16}. Then the user sends three bytes to select desired address. The controller sets the address on output and starts the read cycle. As the writing process, data reading is carried out in several steps, each of them lasts for 5 µs. In the first step, the Chip Enable is pulled down to enable the MRAM. In the next step, the Output enable is pulled down. The controller waits another step to ensure that the valid data are on the MRAM's output. Then the data are read and sent to the user.

The controller can also check if the MRAM is empty. It is recommended to do so before writing new bitstream. The cycle starts with command 57_{16}. The controller sets the address to zero, read the data and checks if data is zero. If not, the „fail“ byte 46_{16} is sent. If otherwise, the controller increments the address and checks the data. It sends „success“ byte 53_{16} if reaches the end of memory and all data are zero.

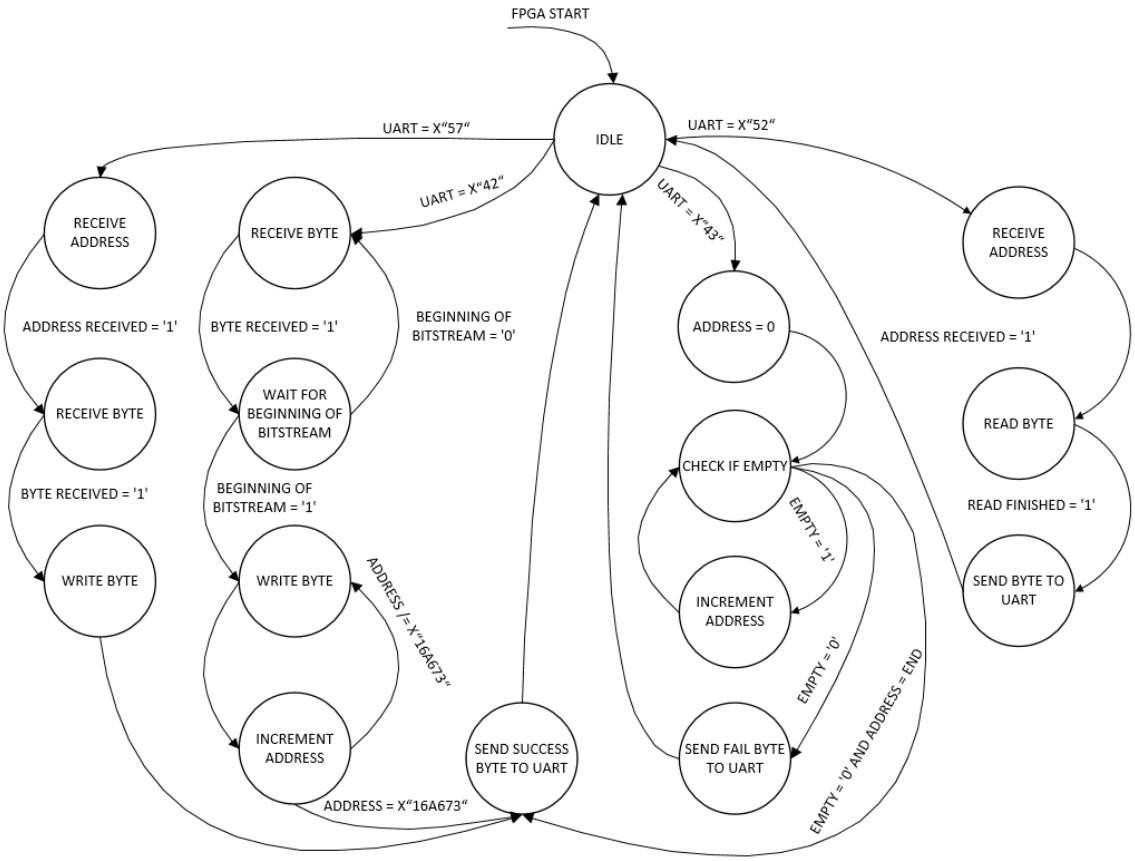


Figure 25: States of MRAM Controller

7.3. ADC Controller

The controller communicates with the ADC and reads measured data. The SPI protocol operates in SPI Mode 3 and can have a frequency up 100 MHz [46]. The ADC is configured to run in full power mode and SPI speed is set to 1 MHz and can be changed in the code if needed.

To write any data, the FPGA must write data to communication register. It selects if the next operation is read or write operation, and determines to which register operation occurs [46]. Then the FPGA must wait until the ADC processes the data. This time is determined by ADC's power mode and can be calculated from ADC's datasheet [46]. The FPGA can write data after this period. Data can be acquired by setting MOSI to '1' and pulsing SCLK. The complete state machine is shown in Figure 26.

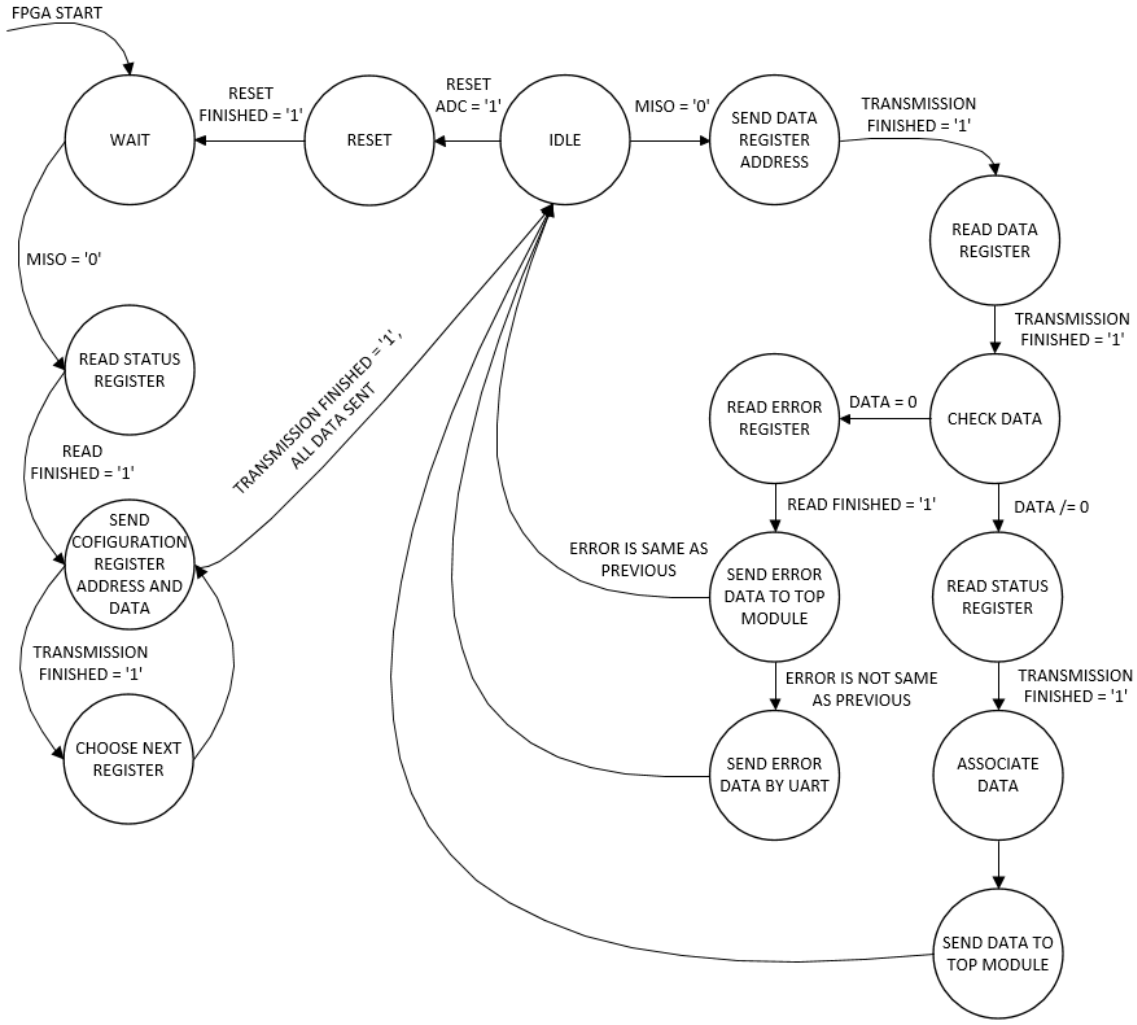


Figure 26: States of ADC Controller

After the start up, the FPGA must wait until the ADC is ready, which is signalized by ADC pulling MISO down. The FPGA reads the Status register to clear the Power-up reset flag. After that, the configuration can start. The configuration registers are described in Table 9.

Table 9: Configured registers, listed bits are enabled, the rest is disabled

Register	Enabled Bits
ADC Control Register	DATA_STATUS, REF_EN, POWER_MODE = FULL POWER
ADC Configuration Register	REF_BUFP, REF_BUFM, AIN_BUFP, AIN_BUFM, REF_SEL = INTERNAL REFERENCE
ADC Channel 0 Register	Enable, AINP = AIN6, AINM = AIN5
ADC Channel 1 Register	Enable, AINP = AIN6, AINM = AIN7
ADC Channel 2 Register	Enable, AINP = AIN3, AINM = AV_{SS}
ADC Channel 3 Register	Enable, AINP = AIN4, AINM = AV_{SS}

The controller goes to Idle state after all registers are configured. The ADC sets MISO high a measures the first channel (Channel 0). The MISO is pulled down after the measurement and the FPGA sends the Data register address to read the value. The Status register is transmitted immediately after reading the Data register. This is useful as the four LSBs of the Status register indicate the channel to which the conversion corresponds [46]. If the measured value is not a zero, the controller sends the data to the TOP module, where it can be stored and/or send to the user. Then the ADC starts measuring the next channel.

An error is present if the measured value is zero. In this case, the controller reads the error register and sends it to the TOP module. Then the error is sent to the user, but only if a new one is present. The controller would not stop transmitting the error if otherwise. The ADC can be reset by sending command 41_{16}.

7.3.1. Temperature calculation

Calculating temperature in °C from the measured value is complex and would be difficult to implement in the FPGA, therefore only the measured value is sent and the user should do the calculation. Temperature can be found using equations from [47]:

$$R_{NTC} = \frac{ADC_{CODE} \cdot R_{REF}}{FS_{CODE} - ADC_{CODE}} \tag{6.1}$$

$$T = \frac{1}{\frac{ln\left(\frac{R_{NTC}}{R_0}\right)}{\beta} + \frac{1}{T_0}} - 273.15 \tag{6.2}$$

where ADC_{CODE} is the code read from the ADC, R_{REF} = 5.6 kΩ, FS_{CODE} is the full-scale code from the ADC (2^{24}), R_0 = 10 kΩ, β = 3434 K and T_0 = 298.15 K.

7.3.2. Current calculation

Measured voltage can be calculated:

$$V_{CHANNEL} = \frac{V_{REF}}{FS_{CODE}} \cdot ADC_{CODE} \tag{6.3}$$

where V_{REF} is reference voltage 2.5 V. Then the current in the 1.2V and 3.3V power rails can be calculated by equations 4.15 and 4.16.

7.3.3. Further improvements

The ADC provides a number of error detections and protections. It can check correct operation, internal and external voltages, and others. The ADC can use CRC check of serial communication with the FPGA and also check internal registers. This improves SEU immunity.

7.4. SD Card Controller

The controller stores the measured values from the ADC to the micro SD card and can read any data as user requests. The operation is shown in Figure 27. The socket for the card has an internal switch, which detects if the card is inserted.

The SD card stores data as blocks with a size of 512 bytes. The controller uses two FIFO memories as temporary storage. When all 512 bytes are in the first FIFO, the controller sends its content to SD card. Reading from the SD cards works in a similar way. The controller sends a command for a read operation and block's address. The SD card sends all 512 bytes and they are stored in the second FIFO. Then the controller takes the right byte from the memory and sends it to the TOP module.

The controller continuously checks if the card is inserted after the FPGA's start up. If the card is plugged in, the controller resets the card and runs initialization process. Then it gets to the Idle state. The ADC signalizes every time the measurement cycle (all channels measured) finishes. The SD controller takes the data and stores them in a buffer, which is then sent to the first FIFO. It means that only whole set of data is saved. The design uses a simple counter to create a period, after which the data are sent to the first FIFO. The period is set to 5 ms but can be easily changed in the code.

To read any byte, the user has to send a command 53_{16}, which stops the processes for storing data and sets the controller to the read mode. Then the user must send five bytes to choose the right block address and three bytes to select the address of the byte in the second FIFO. The controller sends the byte via UART and erases the memory.

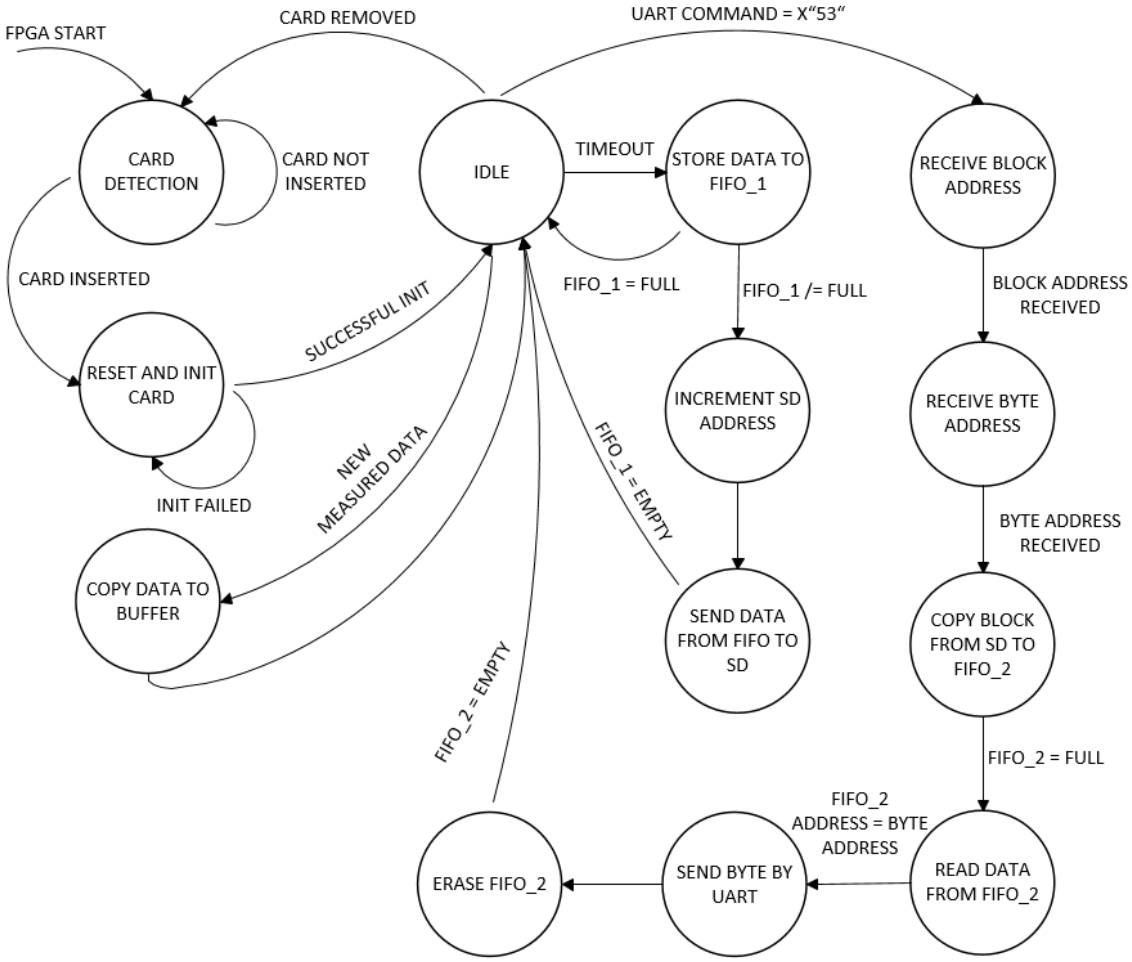


Figure 27: States of SD Controller

7.4.1. Interface Controller

The SD Controller uses standard SPI interface. As any specific protocol is not needed, the block responsible for SD card initialization and communication was downloaded from [48]. The operation is described in the same source.

7.5. UART Controller

The design uses two blocks, one as a transmitter and one as a receiver. Both use standard UART interface, therefore they were downloaded from [49]. Using verified design decreases the development time and helps with debugging.

UART has one stop and one start bit, no parity bit, and frequency 115200 bauds. The design uses parameter g_CLKS_PER_BIT, which can be calculated [49]:

$$g\_CLKS\_PER\_BIT = \frac{clk}{f_{UART}} \tag{6.4}$$

The user can change the baud rate or internal frequency by changing this parameter.

7.6. Design statistics

Statistics of the whole design is shown in Table 10. The table shows that the design uses less than 8 % of available resources. It leaves enough space for user application.

Table 10: Logic utilizaton

Logic	Used	Available	Utilization
Slice Registers	1141	54576	2%
Slice LUTs	1435	27288	5%
Slices	498	6822	7%

After implementation, XPower Analyzer can be run to estimate power consumption. Results are shown in Table 11.

Table 11: Power consumption for V_{CCAUX} = 3.3 V

Power Net	Voltage [V]	Current [mA]		
		Total	Dynamic	Quiescent
V_{CCINT}	1.2	28	12	16
V_{CCAUX}	3.3	6	0	6
$V_{CCO3.3V}$	3.3	7	5	2
Total Supply Power [mW]		76	32	44

7.7. High load design

The purpose of this digital design is to stress the power sources and the FPGA to the maximum. The design was used from [50] as its main advantage is to easily change the number of logic. Several iterations were made to find the setup which uses the biggest number of logic resources. The results are shown in Table 12. Higher utilization was not achieved due to various problems with implementation.

Table 12: Logic utilization of high load design

Logic	Used	Available	Utilization
Slice Registers	14450	54576	26%
Slice LUTs	15244	27288	55%
Slices	5657	6822	82%
RAM Blocks	42	116	36%
DSP48A1	48	58	82%

XPower Analyzer was used to estimate power consumption. Results are shown in Table 13.

Table 13: Power consumption for high load circuit

Power Net	Voltage [V]	Current [mA]		
		Total	Dynamic	Quiescent
V_{CCINT}	1.2	302	283	19
V_{CCAUX}	3.3	6	0	6
$V_{CCO3.3V}$	3.3	7	5	2
Total Supply Power [mW]		384	342	42

8. Measurement results

Proper operation and its parameters of the unit are shown in this chapter.

8.1. Power

8.1.1. Power consumption

To estimate unit's suitability for CubeSat missions, power consumption has to be measured. Input current for both power inputs was measured for different types of operation. Results are shown in Table 14.

Table 14: Input current

Mode	V_{CCAUX} = 3.3 V		V_{CCAUX} = 2.5 V	
	Current [mA]			
	5V power rail	3.3V power rail	5V power rail	3.3V power rail
Before configuration	27.58	45.80	30.07	39.60
Before configuration, JTAG programmer connected	27.59	54.20	30.19	48.80
Idle, after configuration	29.83	34.58	31.52	30.04
Idle, JTAG connected	29.78	44.40	31.51	40.40
Idle, SD card connected	29.85	110.00	31.68	108.40
Maximal	29.85	110.00	31.68	108.40

Results show that input current is highest when SD card is connected. Current is decreased to half if SD card is not needed. If V_{CCAUX} is connected to 2.5 V input current from 3.3V power rail is decreased by 13 % in Idle mode. Input current in 5V power rail is slightly increased as the adjustable DC/DC converter is powered from it.

8.1.2. Power consumption at high load

The purpose of the high load is to stress power sources to maximum. Input currents for this mode are shown in Table 15. Consumption was measured without SD card.

Table 15: Input current at high load

Mode	V_{CCAUX} = 3.3 V		V_{CCAUX} = 2.5 V	
	Current [mA]			
	5V power rail	3.3V power rail	5V power rail	3.3V power rail
Before configuration	28	46	30	40
After configuration	102	36	104	31

8.1.3. FPGA's power inputs

The FPGA's power sources can have a maximum ripple of 50 mV and ramp from 0.2 to 50 ms. Power ramp for the 1.2V power source is shown in Figure 28. Ramp time is approximately 10 ms. The adjustable DC/DC converter has same results as the same component is used. Every measurement was done for high load design.

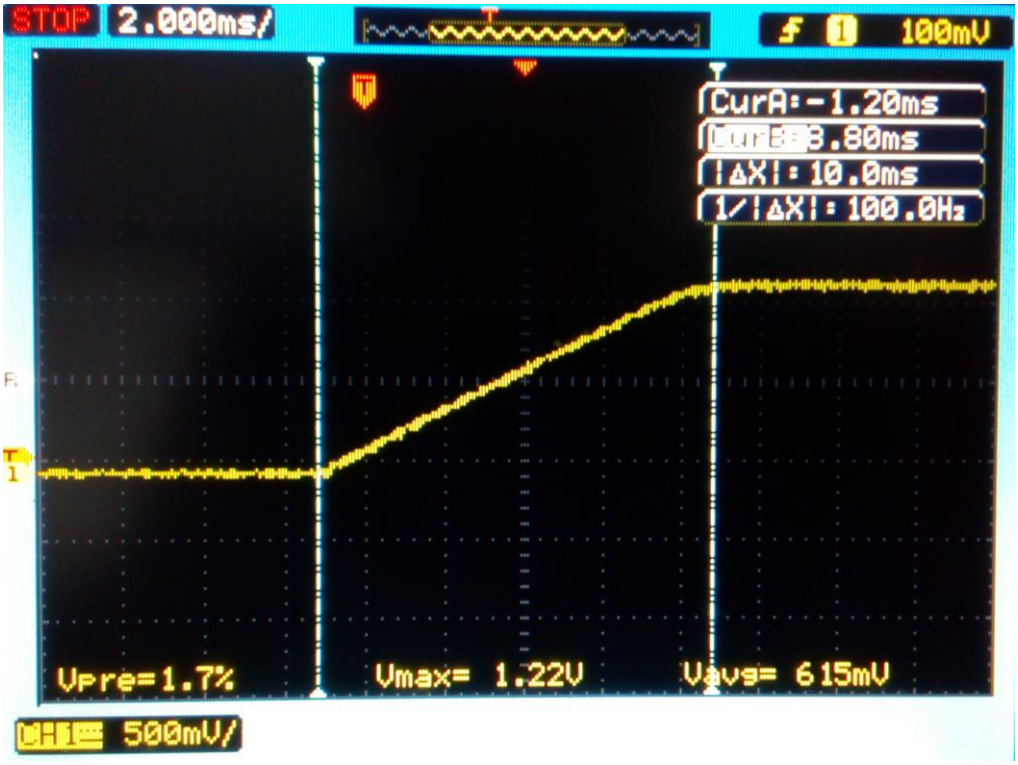


Figure 28: 1.2V power rail - ramp time

Ramp time for 3.3V power rail is shown in Figure 29. The measurement shows that voltage rises by small steps. It does not affect the FPGA's start up or its functionality. Steps can be mitigated by changing the value of feedback components R_1 and C_{65}. Ramp time is shorter as discussed in chapter 4.5.3., but still in required range.

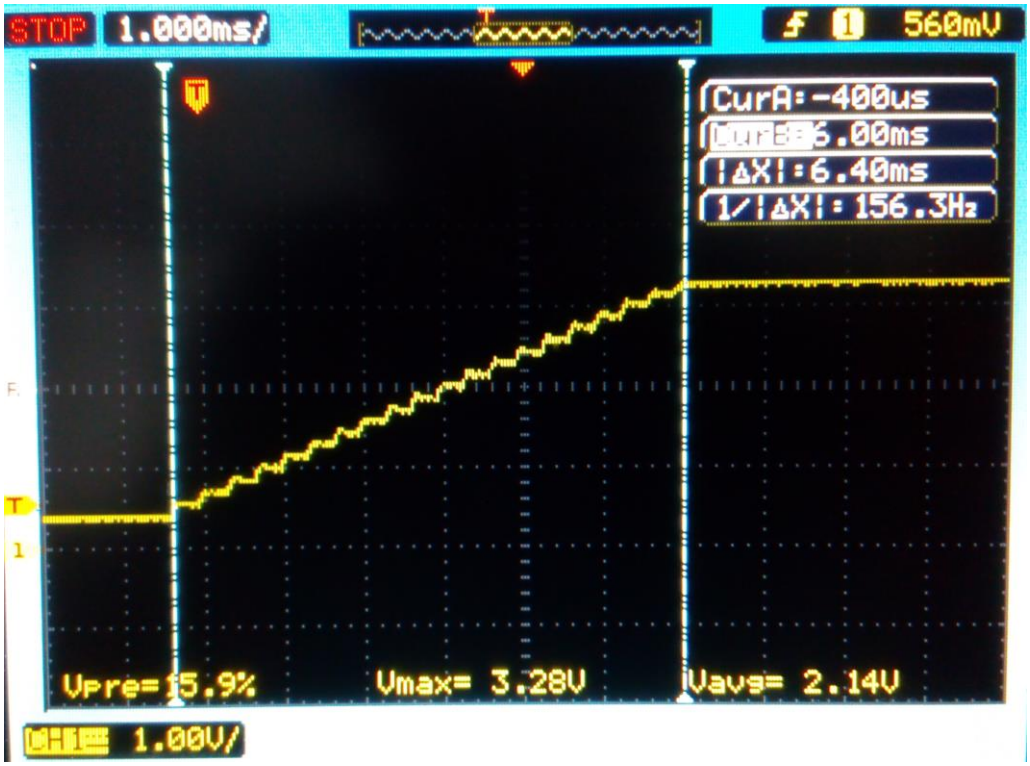


Figure 29: 3.3V power rail - ramp time

Figure 30 shows voltage ripple at the 1.2V power rail. The ripple has a period of 1 µs, which is switching frequency of the DC/DC converter. Figure 31 shows the detail of the ripple.

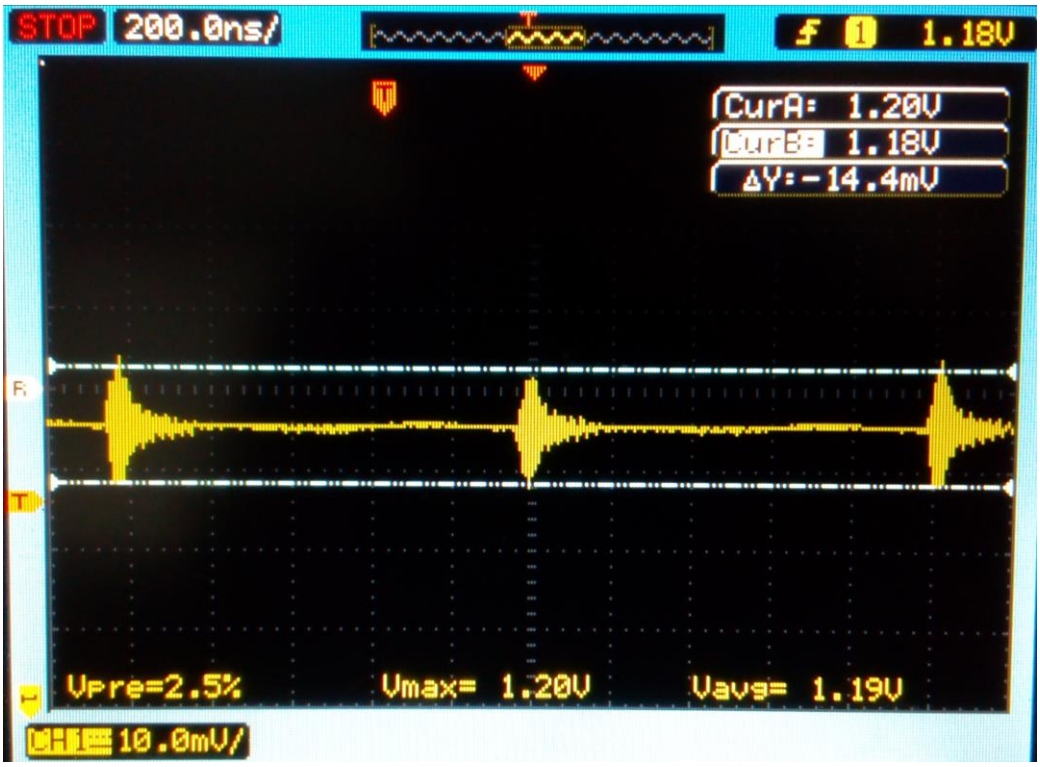


Figure 30: Voltage ripple at 1.2V power rail

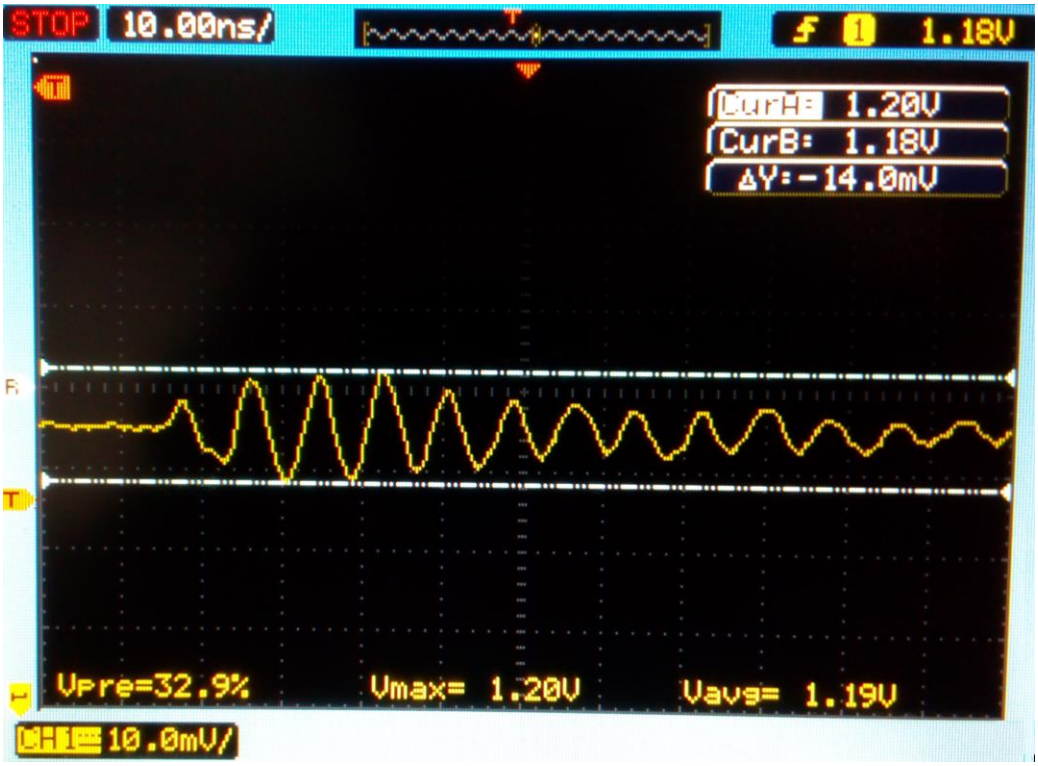


Figure 31: Voltage ripple at 1.2V power rail – detail

The voltage ripple has a maximal value 14 mV_{P-P}, which is low enough for proper operation. The 3.3V power rail has no ripple as there is now switching component in the path.

8.1.4. Conclusion

Power consumption is about 100 mA for both power inputs even for high utilization. It can be further reduced by enabling Power reduction in Synthesis and Implementation, using slower clock and other techniques.

The standard CubeSat solar array provides current 500 mA at 5 V at maximum power [22]. Therefore, more than 300 mA can be used for other circuits and/or for charging onboard batteries. The smallest CubeSat battery has a capacity of 3 Ah [22]. In the worst case, a satellite is exposed to the Sun for about half of orbit. As soon as the CubeSat stays in shadow for a shorter time than 15 hours, the unit is suitable to be used in all types of CubeSat.

8.2. Configuration circuit

Figure 32 shows measurement of configuration circuit by a logic analyzer. The first wave is the output from the FPGA. It generates pulses with period about 50 ms. When pulses are not produced anymore, the watchdog waits 2 seconds and produces reset pulse (the second wave). Every reset pulse sets logic 1 to another output of the shift register (the third-fourth wave).

Figure 32: Configuration circuit measurement

9. Stratospheric test flight

To test the survivability of the unit in harsh conditions and radioactive environment, the unit was used as one of the payloads of the stratospheric balloon. The test was carried out at 20th of May in Torun as a part of Near Space Conference.

The main goal of the test was to measure a number of SEU in the configuration memory. The bitstream was uploaded to the FPGA. After the landing, the bitstream should be downloaded from the FPGA and compared with pre-flight version. The number of different bits would give a number of SEUs.

9.1. Preparations

The unit was supposed to be connected to another board providing the necessary power. That board was developed by another student. Unfortunately, the board was not finished before the flight. As this outcome was known a day before launch, another solution had to be made.

The power was provided by six AAA batteries, each with nominal voltage 1.5 V and 1200mAh capacity [51]. The unit can work with voltage down to 2.2 V for 3.3V rail and voltage down to 4.2 V for 5V power rail. As the voltage drops quickly at the beginning of discharge curve, four batteries had to be used for 5V power rail instead of three. The batteries were connected to 56Ω resistor until the voltage dropped to 5.5 V, which is the maximum for DC/DC converters, before connecting to the unit. Then the batteries were placed into battery holder and attached to the board by tape, wires were soldered directly to the I/O connector. The prepared board is shown in Figure 33.

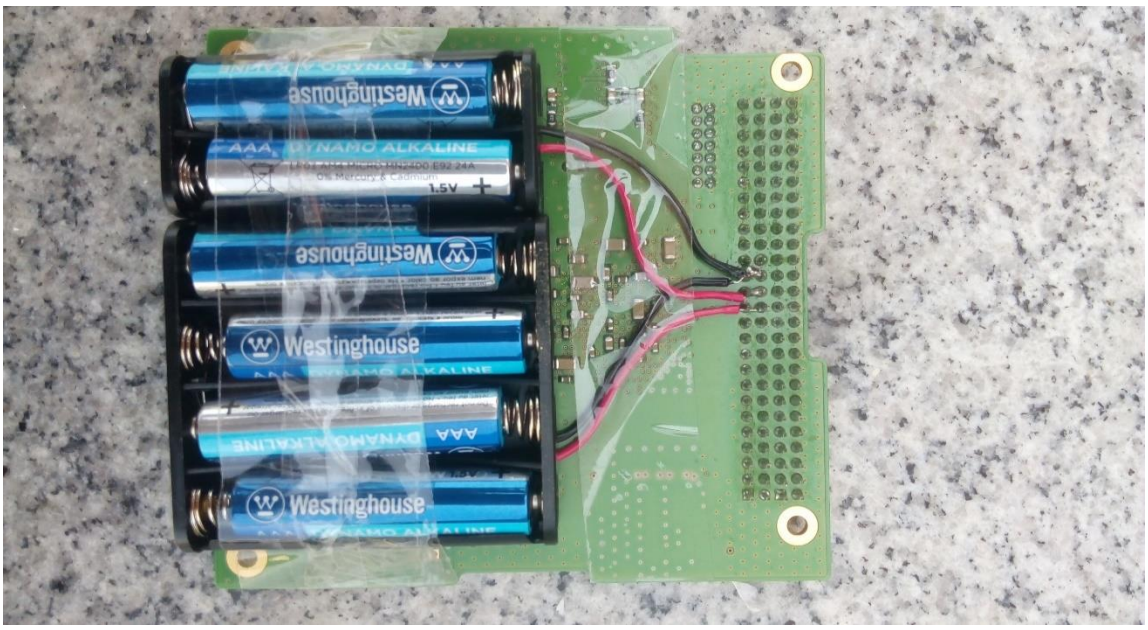


Figure 33: The board with batteries

9.2. Results

The flight took approximately five hours and the balloon got to the altitude of 33 km. Unfortunately, its parachute did not deploy completely, therefore the descent was faster than expected. After recovery of the payload, it was found that one of the batteries disconnected during impact. No data could be acquired as the configuration is volatile.

The survivability of the board could not be evaluated as the bitstreams could not be compared. Another test flight should take place in summer and will be carried out by Department of Dosimetry and Application of Ionizing Radiation. The unit will be additional payload of radiation dosimeter.

Photos from the flight are shown in Annex D.

10.Summary

The main goal of this thesis was to design a control unit with FPGA, which can be used in future CubeSat.

The first part explains characteristics of the space environment. Radiation, temperature, debris, plasmas and other elements, which have a significant impact on a mission, are described. Also, information about main Earth's orbits is provided.

The second part continues in describing space environment, focusing on radiation and its effects on electronics. It compares radiation hardness of bipolar and unipolar technology. The part mainly describes effects on digital logic and various types of errors which can radiation produce. The chapter also compares Commercial, Rad Tolerant and Rad Hard types of electronic parts.

The third part is focused on CubeSat; their characteristics, properties, and aspects. The most important requirements are listed, especially the dimensions of the board. The dimensions will be used for layout of the control unit.

At the beginning of the design, an exemplary orbit was chosen to simulate and predict an environment, which can a CubeSat experience. The orbit was selected to be the same as the orbit of the International Space Station. The simulation showed, that even a thin aluminum shielding can significantly decrease the radiation dose. Other ways to decrease the influence of the environment are also discussed.

The main part of the thesis is the selection of the FPGA. Considering pros and cons, the automotive version of the Spartan 6 was selected. The FPGA has the lowest power consumption and price of all products offered by Xilinx. As the FPGA is SRAM based, there is a need for separate bitstream storage. The MRAM was selected as it is immune to radiation. The proposed circuit offers two memories, first for golden bitstream and second for new bitstream or user data. The designed circuit provides autonomous reconfiguration in a case of an error and protects the FPGA against latchups.

The unit was designed according to CubeSat standard and fits 1U CubeSat. A digital design was made to test all its functions. Final tests confirmed proper operation of the unit and all its subsystems. The unit also brings significant cost reduction compared to other units on the market.

The unit can be used in space environment with sufficient reliability and significant cost reduction. Future development will include vibration stress test, temperature measurement in a vacuum chamber and another flight as the payload of the stratospheric balloon.

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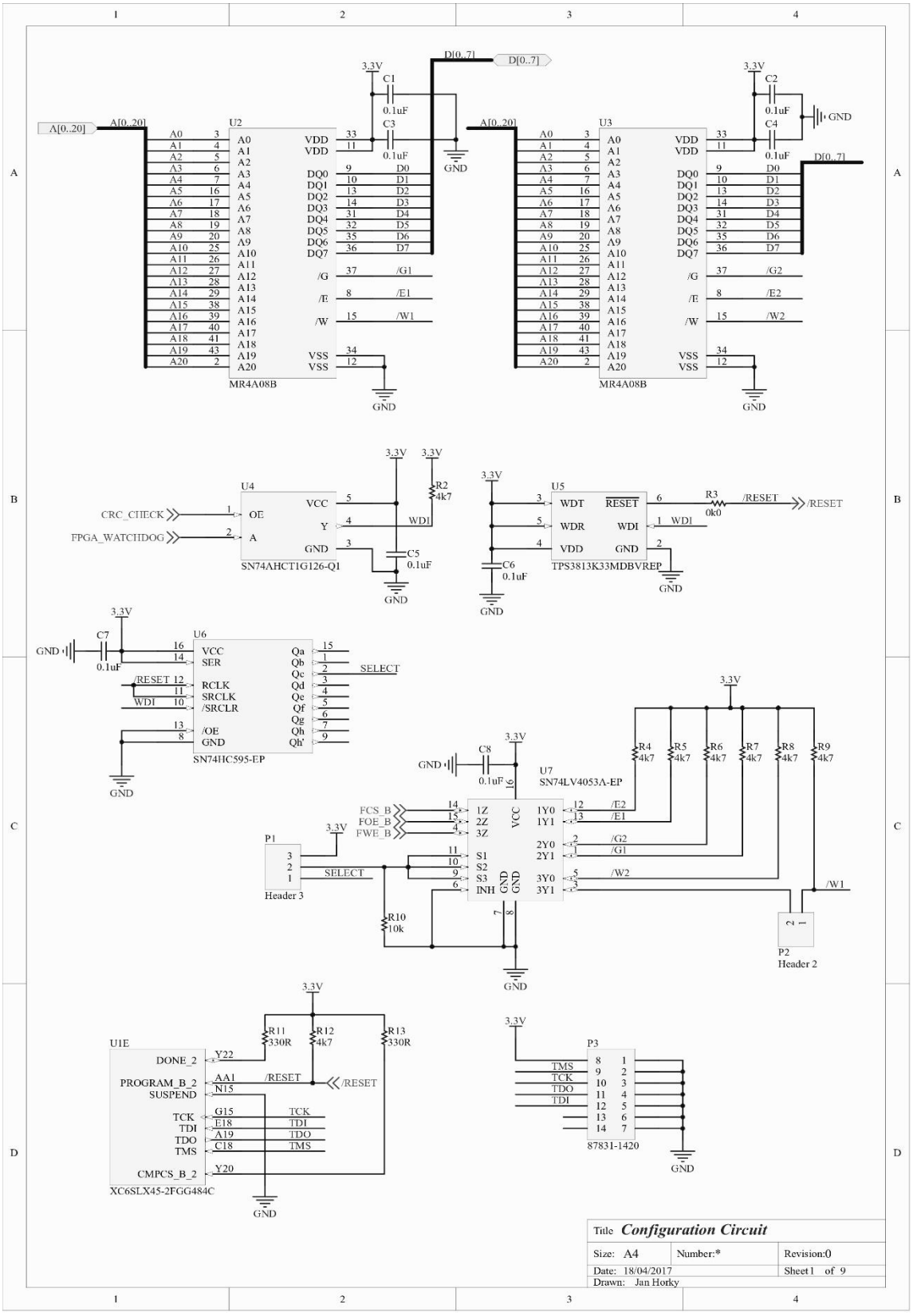
List of acronyms

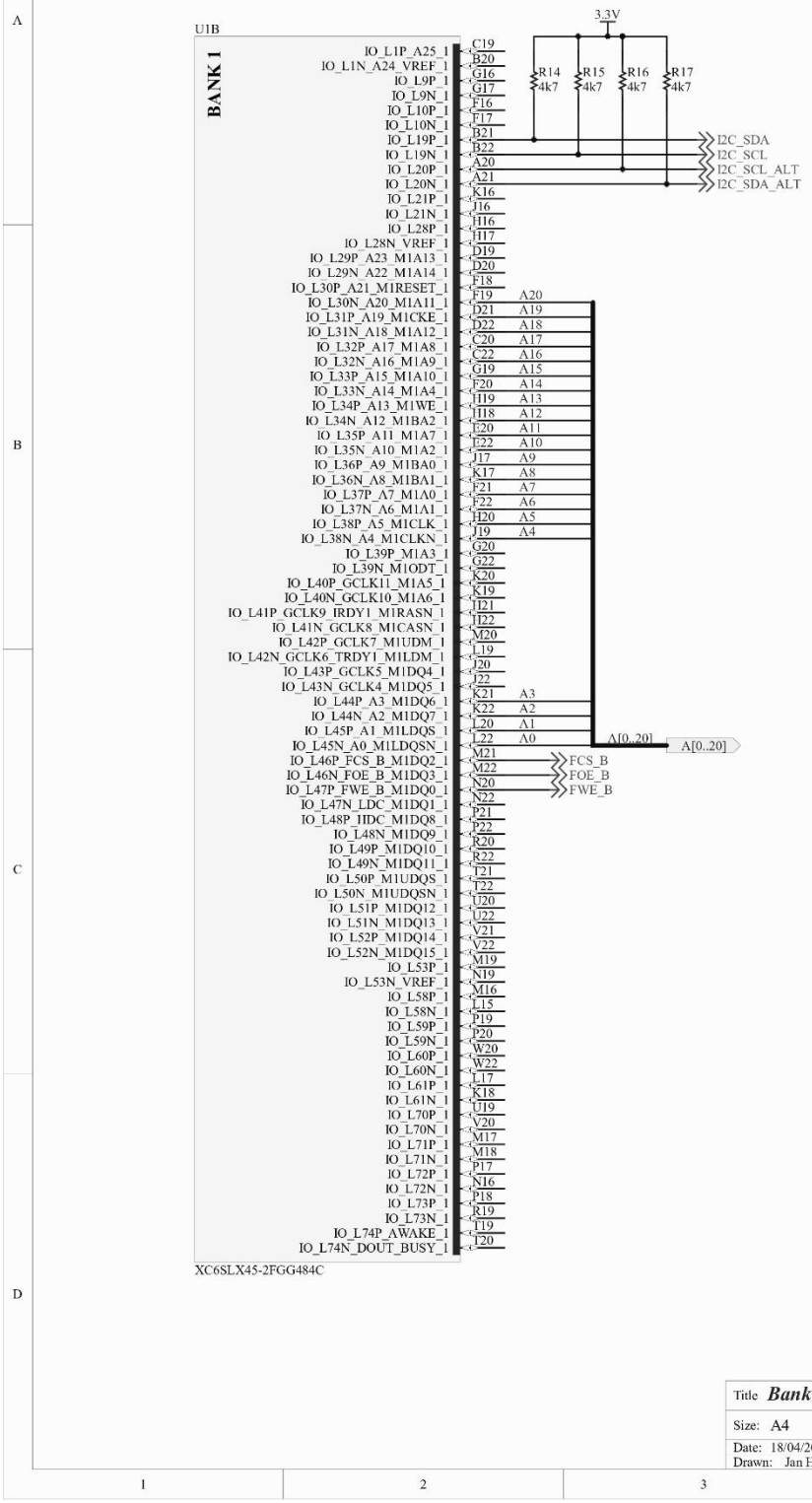
ESA	European Space Agency
NASA	National Aeronautics and Space Administration
UV	Ultraviolet
IR	Infrared
LEO	Low Earth Orbit
SEE	Single Event Effects
SEU	Single Event Upset
SET	Single Event Transient
MCU	Multiple Cell Upset
MBU	Multiple Bit Upset
SEL	Single Event Latchup
SEGR	Single Event Gate Rupture
TID	Total Ionizing Dose
LET	Linear Energy Transfer
PPOD	Poly-Picosatellite Orbital Deployer
ISS	International Space Station
FPGA	Field-programmable gate array
SRAM	Static random-access memory
MRAM	Magnetoresistive random-access memory
EP	Enhanced Products

List of figures

List of tables

Annex A. The control unit schematics

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IO_L36N_A8_M1BA1_1 K17 A8
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Revision:0
Date: 18/04/2017
Sheet 2 of 9
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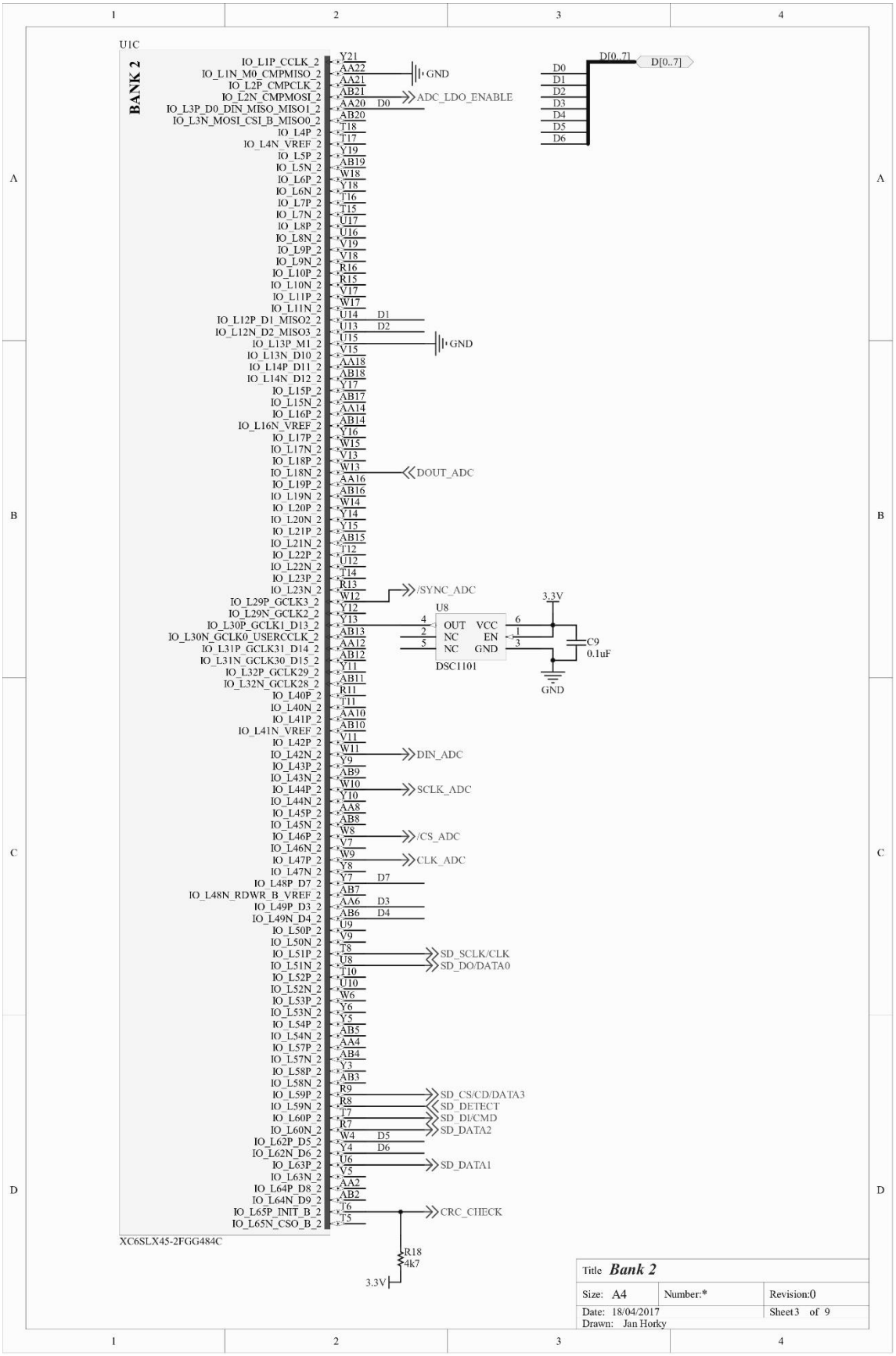
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IO_L4N_VREF_2
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IO_L5N_2
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IO_L6N_2
IO_L7P_2
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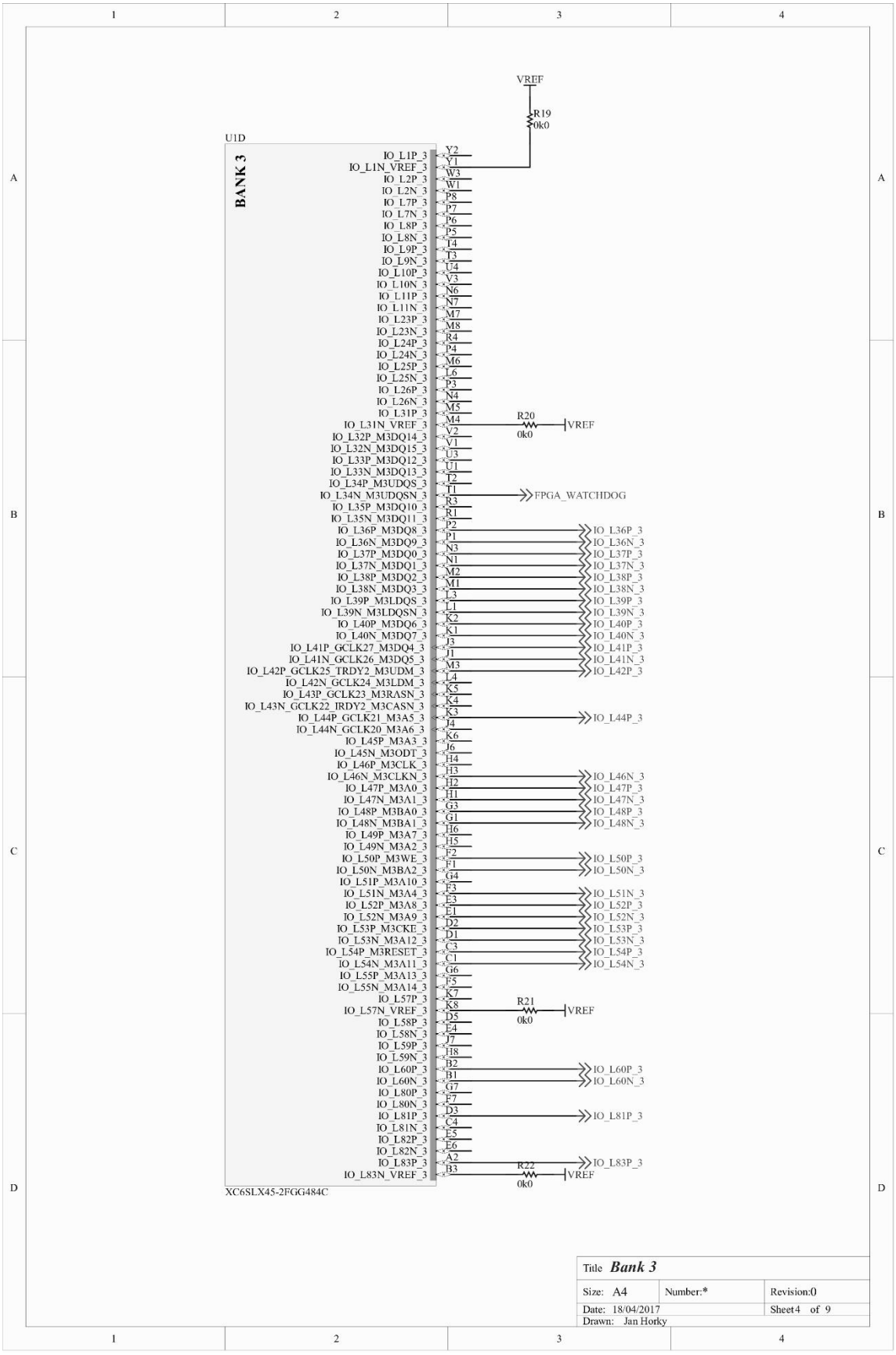
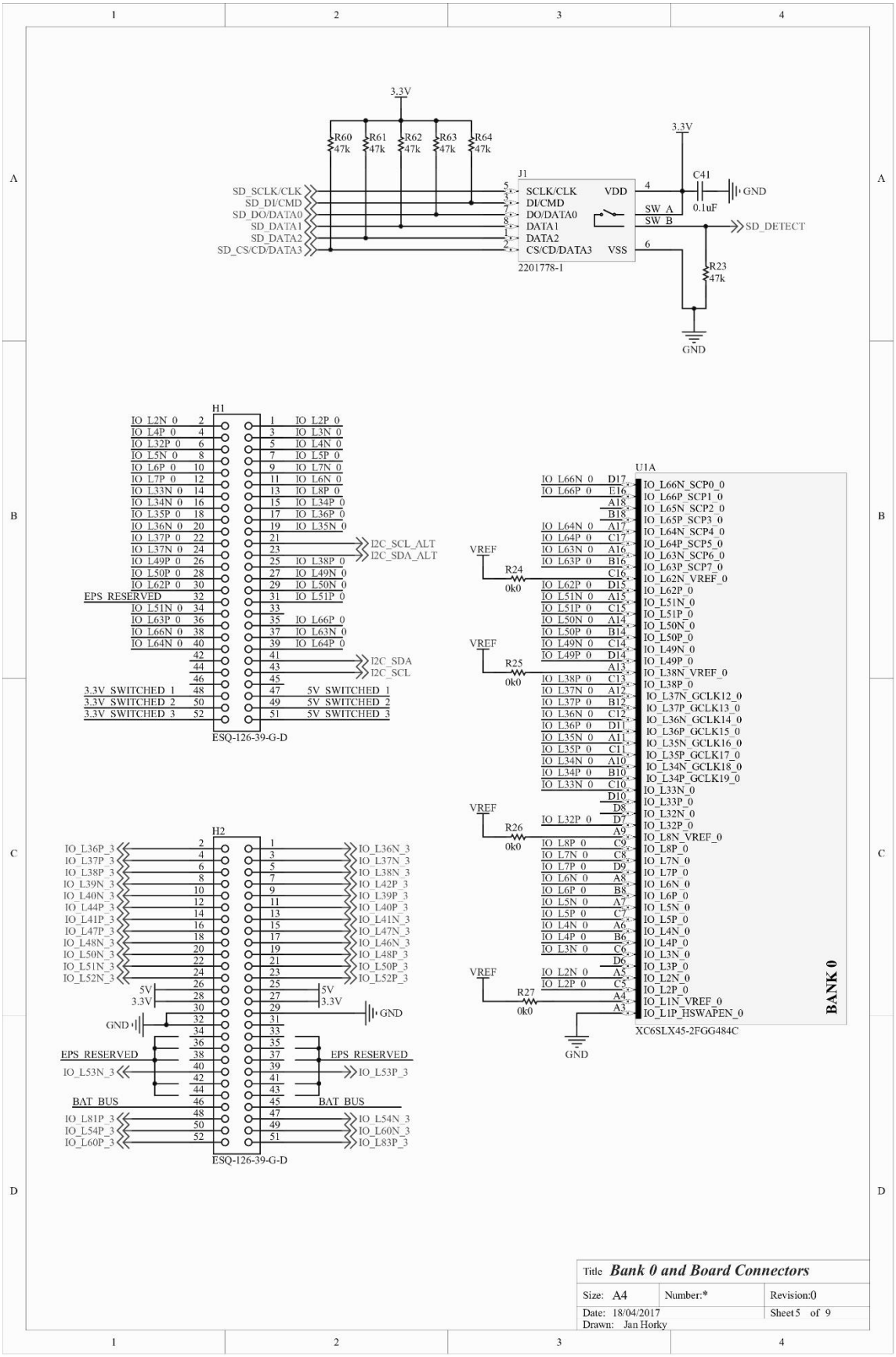
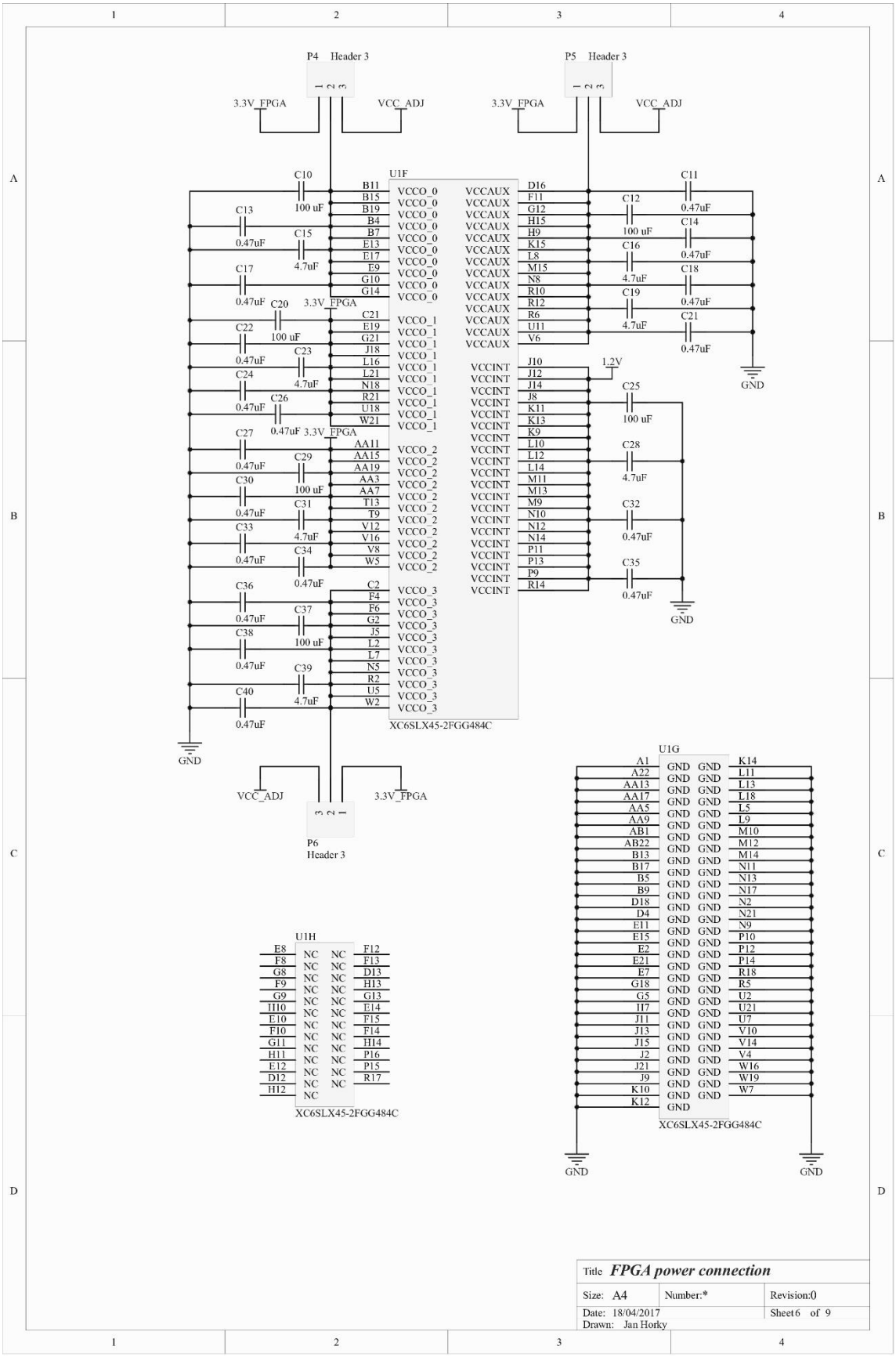
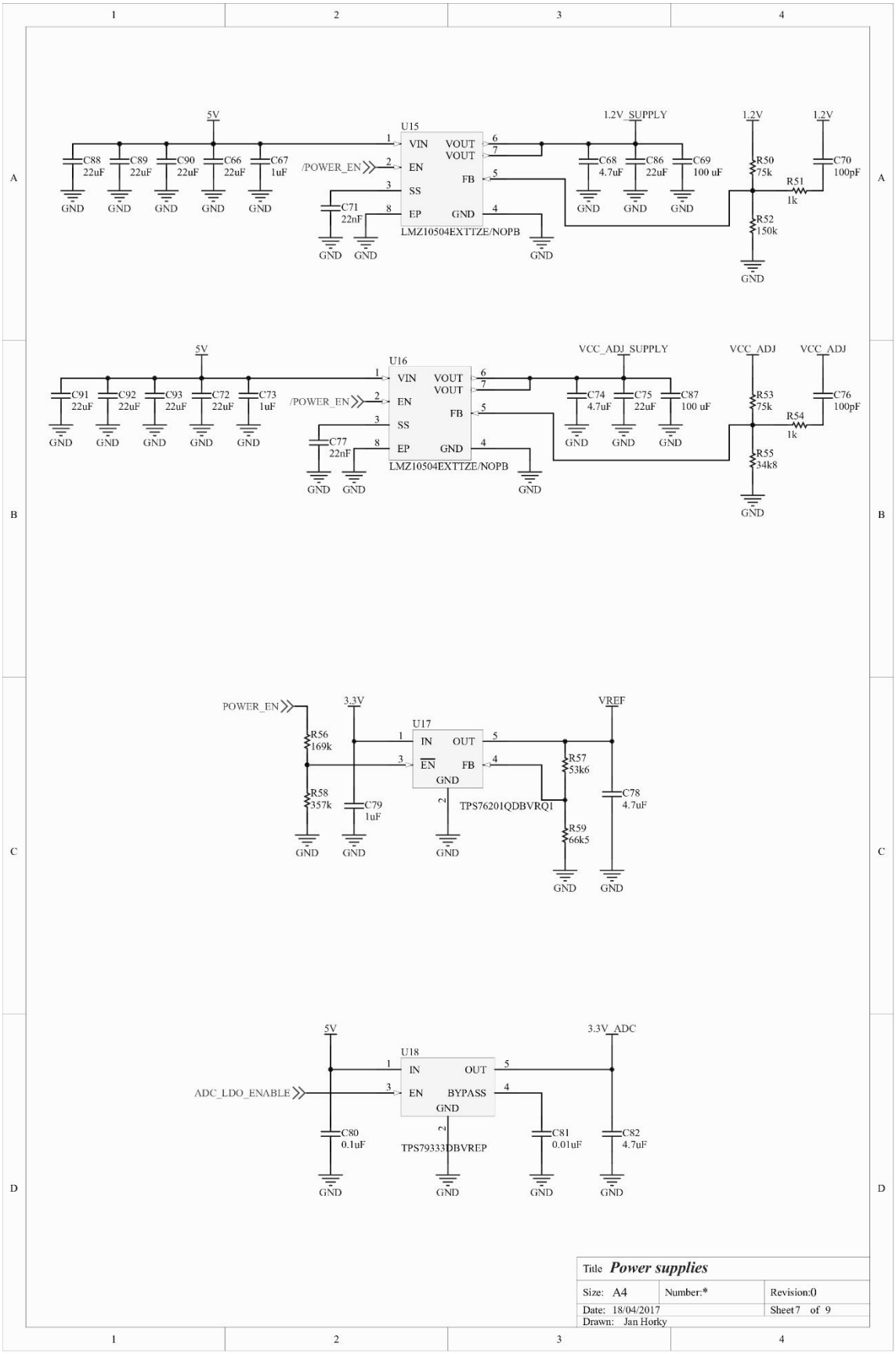
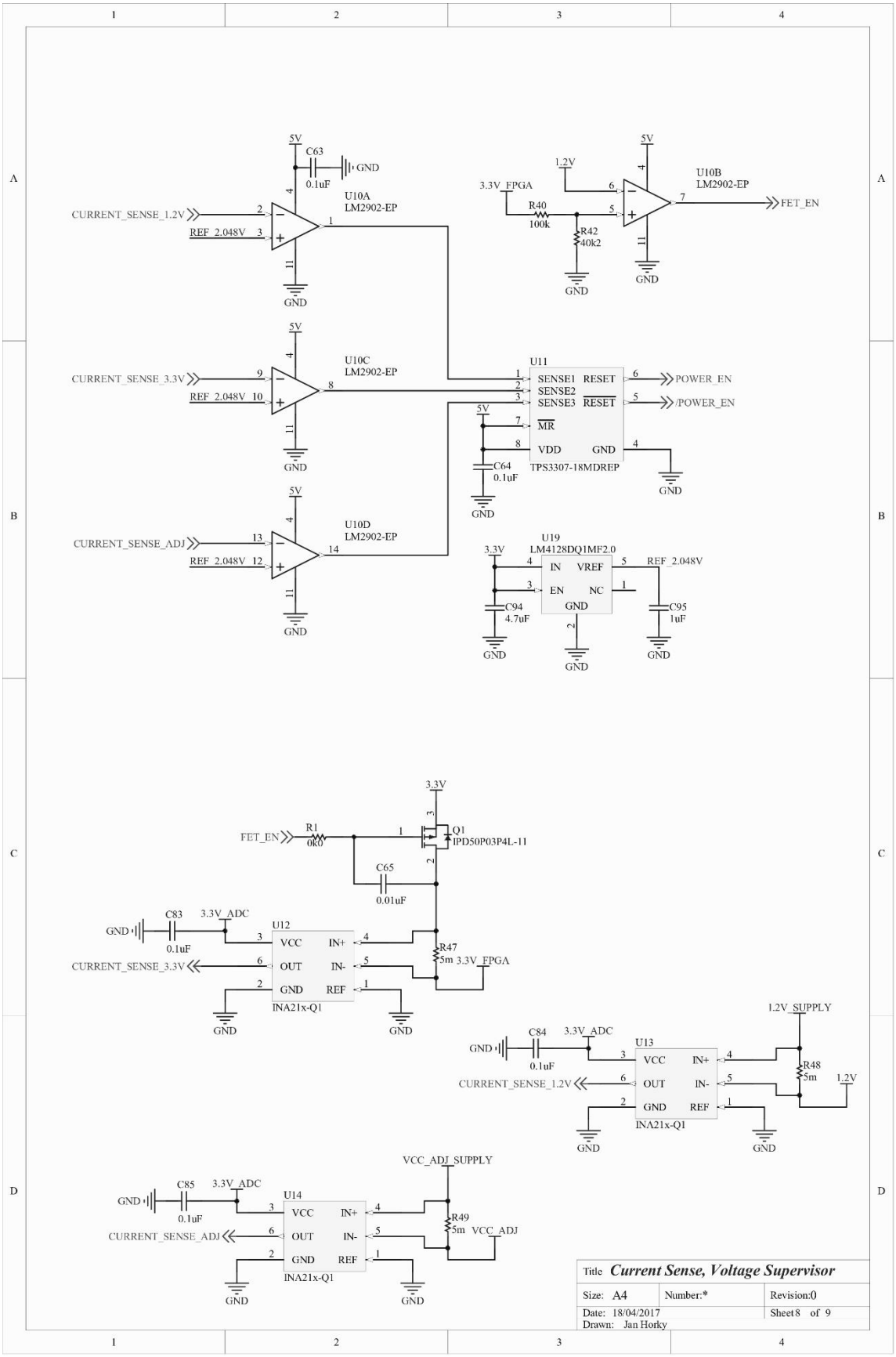
IO_L47N_2
IO_L48P_D7_2
IO_L48N_RDWR_B_VREF_2
IO_L49P_D3_2
IO_L49N_D4_2
IO_L50P_2
IO_L50N_2
IO_L51P_2
IO_L51N_2
IO_L52P_2
IO_L52N_2
IO_L53P_2
IO_L53N_2
IO_L54P_2
IO_L54N_2
IO_L57P_2
IO_L57N_2
IO_L58P_2
IO_L58N_2
IO_L59P_2
IO_L59N_2
IO_L60P_2
IO_L60N_2
IO_L62P_D5_2
IO_L62N_D6_2
IO_L63P_2
IO_L63N_2
IO_L64P_D8_2
IO_L64N_D9_2
IO_L65P_INIT_B_2
IO_L65N_CSO_B_2
XC6SLX45-2FGG484C
GND
ADC_LDO_ENABLE
D0
D1
D2
D3
D4
D5
D6
D7
D[0..7]
DOUT_ADC
/SYNC_ADC
DIN_ADC
SCLK_ADC
/CS_ADC
CLK_ADC
SD_SCLK/CLK
SD_DO/DATA0
SD_CS/CD/DATA3
SD_DETECT
SD_DI/CMD
SD_DATA2
SD_DATA1
CRC_CHECK
U8
OUT
VCC
NC
EN
NC
GND
DSC1101
3.3V
C9
0.1uF
R18
4k7
Title Bank 2
Size: A4
Number:*
Revision:0
Date: 18/04/2017
Sheet 3 of 9
Drawn: Jan Horky

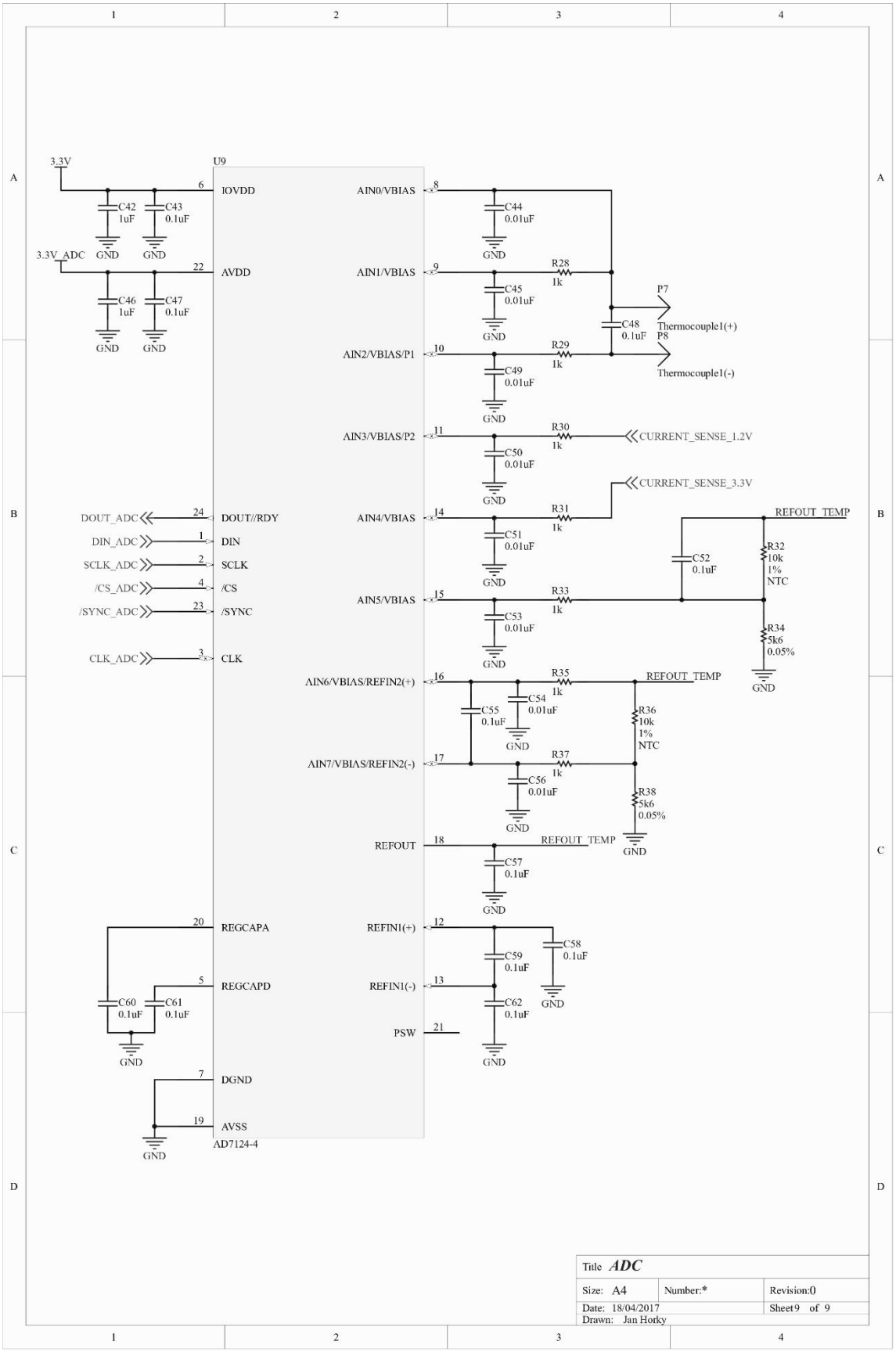

VREF
R19
0k0
U1D
BANK 3
IO_L1P_3 Y2
IO_L1N_VREF_3 Y1
IO_L2P_3 W3
IO_L2N_3 W1
IO_L7P_3 P8
IO_L7N_3 P7
IO_L8P_3 P6
IO_L8N_3 P5
IO_L9P_3 T4
IO_L9N_3 T3
IO_L10P_3 U4
IO_L10N_3 V3
IO_L11P_3 N6
IO_L11N_3 N7
IO_L23P_3 M7
IO_L23N_3 M8
IO_L24P_3 R4
IO_L24N_3 P4
IO_L25P_3 M6
IO_L25N_3 L6
IO_L26P_3 P3
IO_L26N_3 N4
IO_L31P_3 M5
IO_L31N_VREF_3 M4
R20
0k0
VREF
IO_L32P_M3DQ14_3 V2
IO_L32N_M3DQ15_3 V1
IO_L33P_M3DQ12_3 U3
IO_L33N_M3DQ13_3 U1
IO_L34P_M3UDQS_3 T2
IO_L34N_M3UDQSN_3 T1
FPGA_WATCHDOG
IO_L35P_M3DQ10_3 R3
IO_L35N_M3DQ11_3 R1
IO_L36P_M3DQ8_3 P2
IO_L36N_M3DQ9_3 P1
IO_L37P_M3DQ0_3 N3
IO_L37N_M3DQ1_3 N1
IO_L38P_M3DQ2_3 M2
IO_L38N_M3DQ3_3 M1
IO_L39P_M3LDQS_3 L3
IO_L39N_M3LDQSN_3 L1
IO_L40P_M3DQ6_3 K2
IO_L40N_M3DQ7_3 K1
IO_L41P_GCLK27_M3DQ4_3 J3
IO_L41N_GCLK26_M3DQ5_3 J1
IO_L42P_GCLK25_TRDY2_M3UDM_3 M3
IO_L42N_GCLK24_M3LDM_3 L4
IO_L43P_GCLK23_M3RASN_3 K5
IO_L43N_GCLK22_IRDY2_M3CASN_3 K4
IO_L44P_GCLK21_M3A5_3 K3
IO_L44N_GCLK20_M3A6_3 J4
IO_L45P_M3A3_3 K6
IO_L45N_M3ODT_3 J6
IO_L46P_M3CLK_3 H4
IO_L46N_M3CLKN_3 H3
IO_L47P_M3A0_3 H2
IO_L47N_M3A1_3 H1
IO_L48P_M3BA0_3 G3
IO_L48N_M3BA1_3 G1
IO_L49P_M3A7_3 H6
IO_L49N_M3A2_3 H5
IO_L50P_M3WE_3 F2
IO_L50N_M3BA2_3 F1
IO_L51P_M3A10_3 G4
IO_L51N_M3A4_3 F3
IO_L52P_M3A8_3 E3
IO_L52N_M3A9_3 E1
IO_L53P_M3CKE_3 D2
IO_L53N_M3A12_3 D1
IO_L54P_M3RESET_3 C3
IO_L54N_M3A11_3 C1
IO_L55P_M3A13_3 G6
IO_L55N_M3A14_3 F5
IO_L57P_3 K7
IO_L57N_VREF_3 K8
R21
0k0
VREF
IO_L58P_3 D5
IO_L58N_3 E4
IO_L59P_3 J7
IO_L59N_3 H8
IO_L60P_3 B2
IO_L60N_3 B1
IO_L80P_3 G7
IO_L80N_3 F7
IO_L81P_3 D3
IO_L81N_3 C4
IO_L82P_3 E5
IO_L82N_3 E6
IO_L83P_3 A2
IO_L83N_VREF_3 B3
R22
0k0
VREF
XC6SLX45-2FGG484C
IO_L36P_3
IO_L36N_3
IO_L37P_3
IO_L37N_3
IO_L38P_3
IO_L38N_3
IO_L39P_3
IO_L39N_3
IO_L40P_3
IO_L40N_3
IO_L41P_3
IO_L41N_3
IO_L42P_3
IO_L44P_3
IO_L46N_3
IO_L47P_3
IO_L47N_3
IO_L48P_3
IO_L48N_3
IO_L50P_3
IO_L50N_3
IO_L51N_3
IO_L52P_3
IO_L52N_3
IO_L53P_3
IO_L53N_3
IO_L54P_3
IO_L54N_3
IO_L60P_3
IO_L60N_3
IO_L81P_3
IO_L83P_3
Title Bank 3
Size: A4
Number:*
Revision:0
Date: 18/04/2017
Sheet 4 of 9
Drawn: Jan Horky


3.3V
R60 47k
R61 47k
R62 47k
R63 47k
R64 47k
SD_SCLK/CLK
SD_DI/CMD
SD_DO/DATA0
SD_DATA1
SD_DATA2
SD_CS/CD/DATA3
J1
SCLK/CLK
DI/CMD
DO/DATA0
DATA1
DATA2
CS/CD/DATA3
VDD
VSS
2201778-1
C41
0.1uF
GND
SW_A
SW_B
SD_DETECT
R23 47k
H1
I2C_SCL_ALT
I2C_SDA_ALT
I2C_SDA
I2C_SCL
EPS_RESERVED
3.3V_SWITCHED_1
3.3V_SWITCHED_2
3.3V_SWITCHED_3
5V_SWITCHED_1
5V_SWITCHED_2
5V_SWITCHED_3
ESQ-126-39-G-D
H2
5V
3.3V
BAT_BUS
U1A
VREF
R24 0k0
R25 0k0
R26 0k0
R27 0k0
BANK 0
XC6SLX45-2FGG484C
Title Bank 0 and Board Connectors
Size: A4
Number:*
Revision:0
Date: 18/04/2017
Sheet 5 of 9
Drawn: Jan Horky


P4 Header 3
P5 Header 3
3.3V_FPGA
VCC_ADJ
U1F
XC6SLX45-2FGG484C
1.2V
GND
P6
Header 3
U1H
U1G
Title FPGA power connection
Size: A4
Number:*
Revision:0
Date: 18/04/2017
Sheet 6 of 9
Drawn: Jan Horky


5V
U15
VIN
VOUT
VOUT
EN
FB
SS
EP
GND
LMZ10504EXTTZE/NOPB
/POWER_EN
C88 22uF
C89 22uF
C90 22uF
C66 22uF
C67 1uF
C71 22nF
1.2V_SUPPLY
C68 4.7uF
C86 22uF
C69 100 uF
1.2V
R50 75k
R51 1k
R52 150k
C70 100pF
GND
U16
VCC_ADJ_SUPPLY
C91 22uF
C92 22uF
C93 22uF
C72 22uF
C73 1uF
C77 22nF
C74 4.7uF
C75 22uF
C87 100 uF
VCC_ADJ
R53 75k
R54 1k
R55 34k8
C76 100pF
POWER_EN
3.3V
U17
IN
OUT
EN
FB
GND
TPS76201QDBVRQ1
R56 169k
R58 357k
C79 1uF
R57 53k6
R59 66k5
C78 4.7uF
VREF
ADC_LDO_ENABLE
U18
BYPASS
TPS79333DBVREP
C80 0.1uF
C81 0.01uF
C82 4.7uF
3.3V_ADC
Title Power supplies
Size: A4
Number:*
Revision:0
Date: 18/04/2017
Sheet 7 of 9
Drawn: Jan Horky

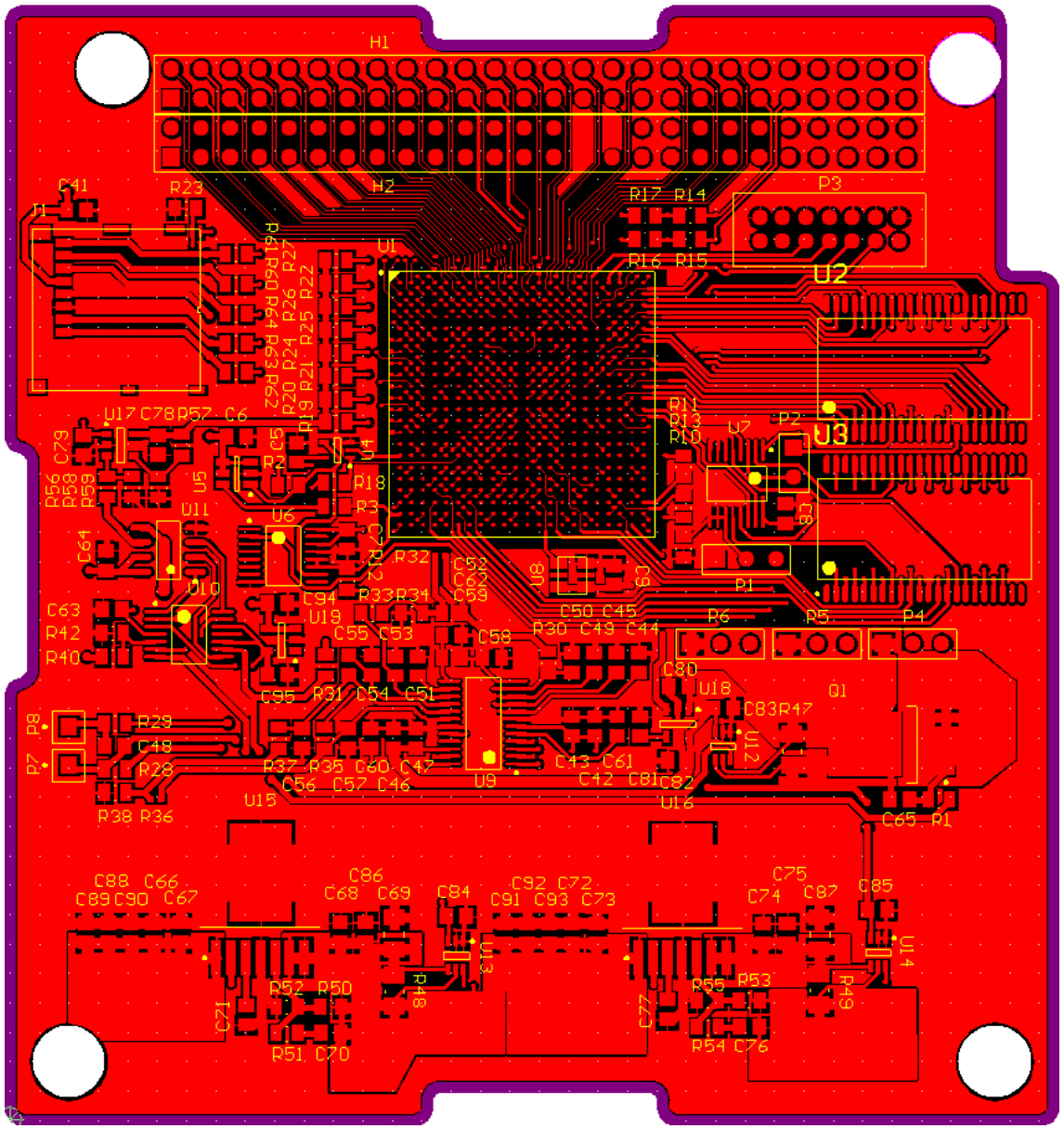

5V
C63
0.1uF
GND
U10A
LM2902-EP
CURRENT_SENSE_1.2V
REF_2.048V
1.2V
3.3V_FPGA
R40
100k
R42
40k2
U10B
LM2902-EP
FET_EN
U10C
LM2902-EP
CURRENT_SENSE_3.3V
REF_2.048V
U11
SENSE1
SENSE2
SENSE3
RESET
MR
VDD
GND
POWER_EN
/POWER_EN
C64
0.1uF
TPS3307-18MDREP
U10D
LM2902-EP
CURRENT_SENSE_ADJ
REF_2.048V
U19
LM4128DQ1MF2.0
IN
VREF
EN
NC
REF_2.048V
C94
4.7uF
C95
1uF
3.3V
FET_EN
R1
0k0
Q1
IPD50P03P4L-11
C65
0.01uF
C83
3.3V_ADC
0.1uF
U12
VCC
IN+
OUT
IN-
GND
REF
INA21x-Q1
CURRENT_SENSE_3.3V
R47
5m
3.3V_FPGA
1.2V_SUPPLY
C84
3.3V_ADC
0.1uF
U13
CURRENT_SENSE_1.2V
R48
5m
1.2V
INA21x-Q1
VCC_ADJ_SUPPLY
C85
3.3V_ADC
0.1uF
U14
CURRENT_SENSE_ADJ
R49
5m
VCC_ADJ
INA21x-Q1
Title Current Sense, Voltage Supervisor
Size: A4
Number:*
Revision:0
Date: 18/04/2017
Sheet 8 of 9
Drawn: Jan Horky


U9
3.3V
3.3V_ADC
IOVDD
AVDD
C42 1uF
C43 0.1uF
C46 1uF
C47 0.1uF
GND
AIN0/VBIAS
AIN1/VBIAS
AIN2/VBIAS/P1
AIN3/VBIAS/P2
AIN4/VBIAS
AIN5/VBIAS
AIN6/VBIAS/REFIN2(+)
AIN7/VBIAS/REFIN2(-)
REFOUT
REFIN1(+)
REFIN1(-)
PSW
C44 0.01uF
C45 0.01uF
C49 0.01uF
C50 0.01uF
C51 0.01uF
C53 0.01uF
C54 0.01uF
C55 0.1uF
C56 0.01uF
C57 0.1uF
C58 0.1uF
C59 0.1uF
C62 0.1uF
R28 1k
R29 1k
R30 1k
R31 1k
R33 1k
R35 1k
R37 1k
C48 0.1uF
P7
Thermocouple1(+)
P8
Thermocouple1(-)
CURRENT_SENSE_1.2V
CURRENT_SENSE_3.3V
REFOUT_TEMP
C52 0.1uF
R32 10k 1% NTC
R34 5k6 0.05%
R36 10k 1% NTC
R38 5k6 0.05%
DOUT_ADC
DIN_ADC
SCLK_ADC
/CS_ADC
/SYNC_ADC
CLK_ADC
DOUT//RDY
DIN
SCLK
/CS
/SYNC
CLK
REGCAPA
REGCAPD
C60 0.1uF
C61 0.1uF
DGND
AVSS
AD7124-4
Title ADC
Size: A4
Number:*
Revision:0
Date: 18/04/2017
Sheet 9 of 9
Drawn: Jan Horky

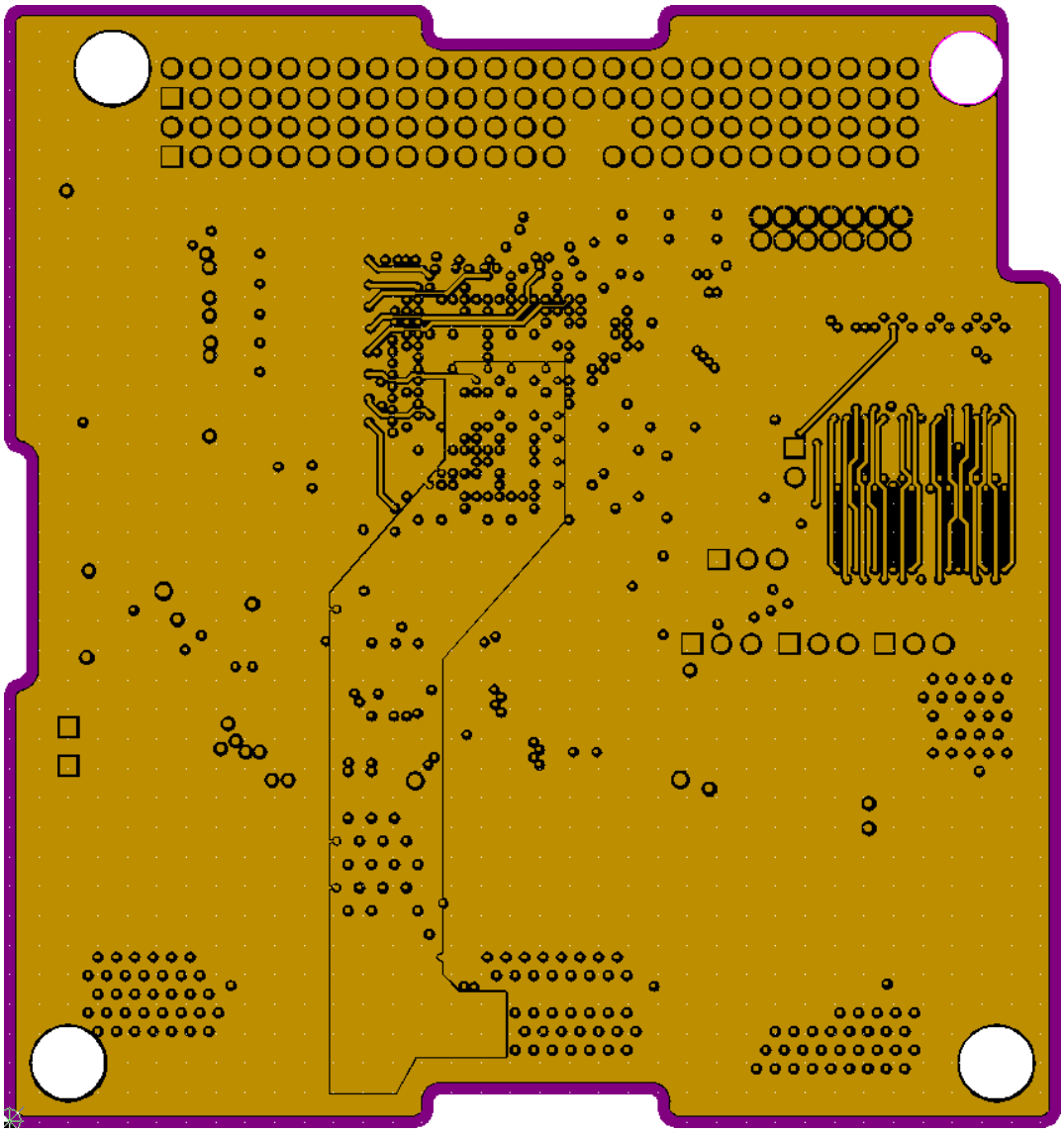
Annex B. PCB layout

Board’s dimensions 10x10 cm, scale 1.5:1. Only via which are unconnected in the current layer are shown.

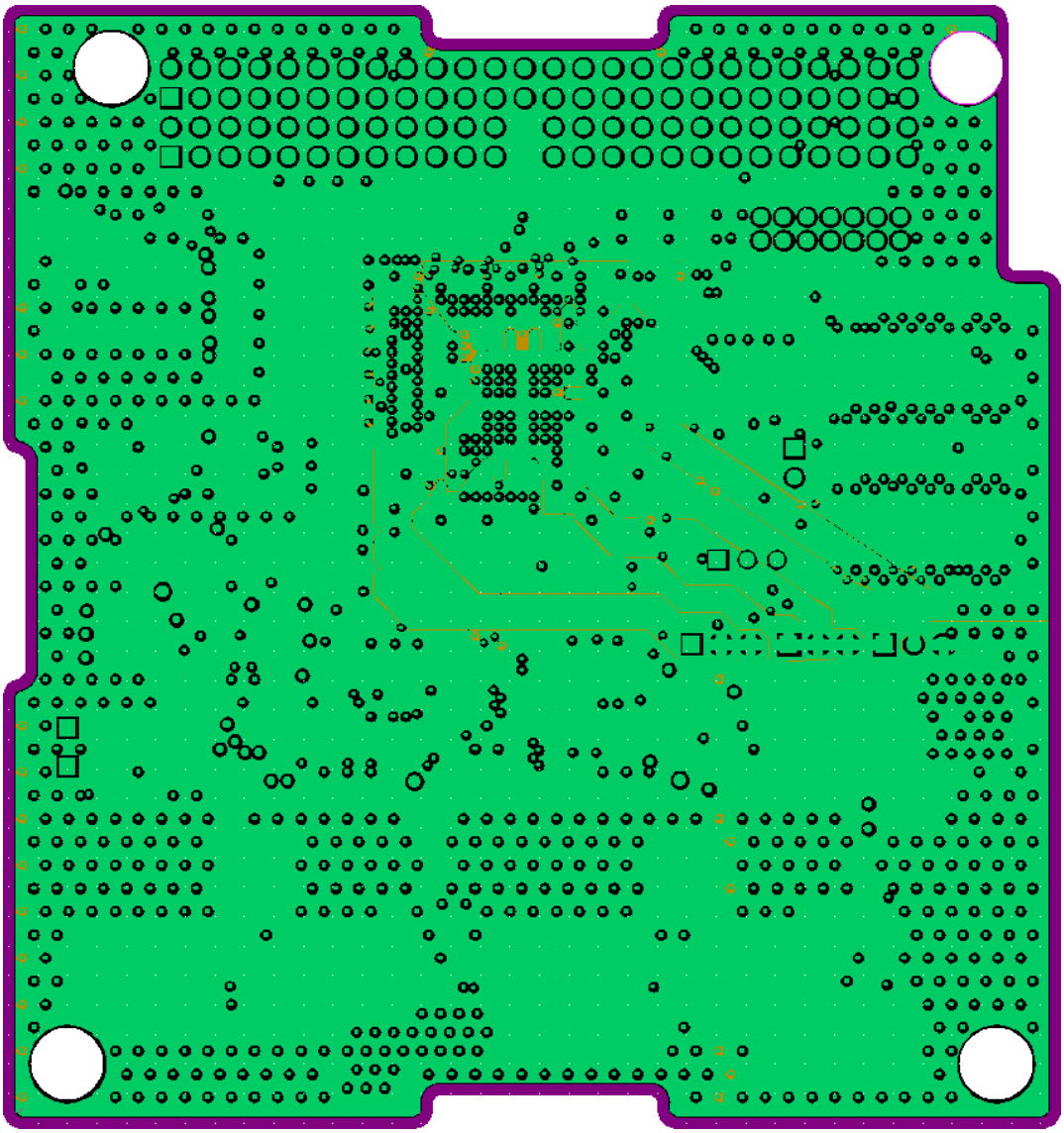
B.1. Top layer



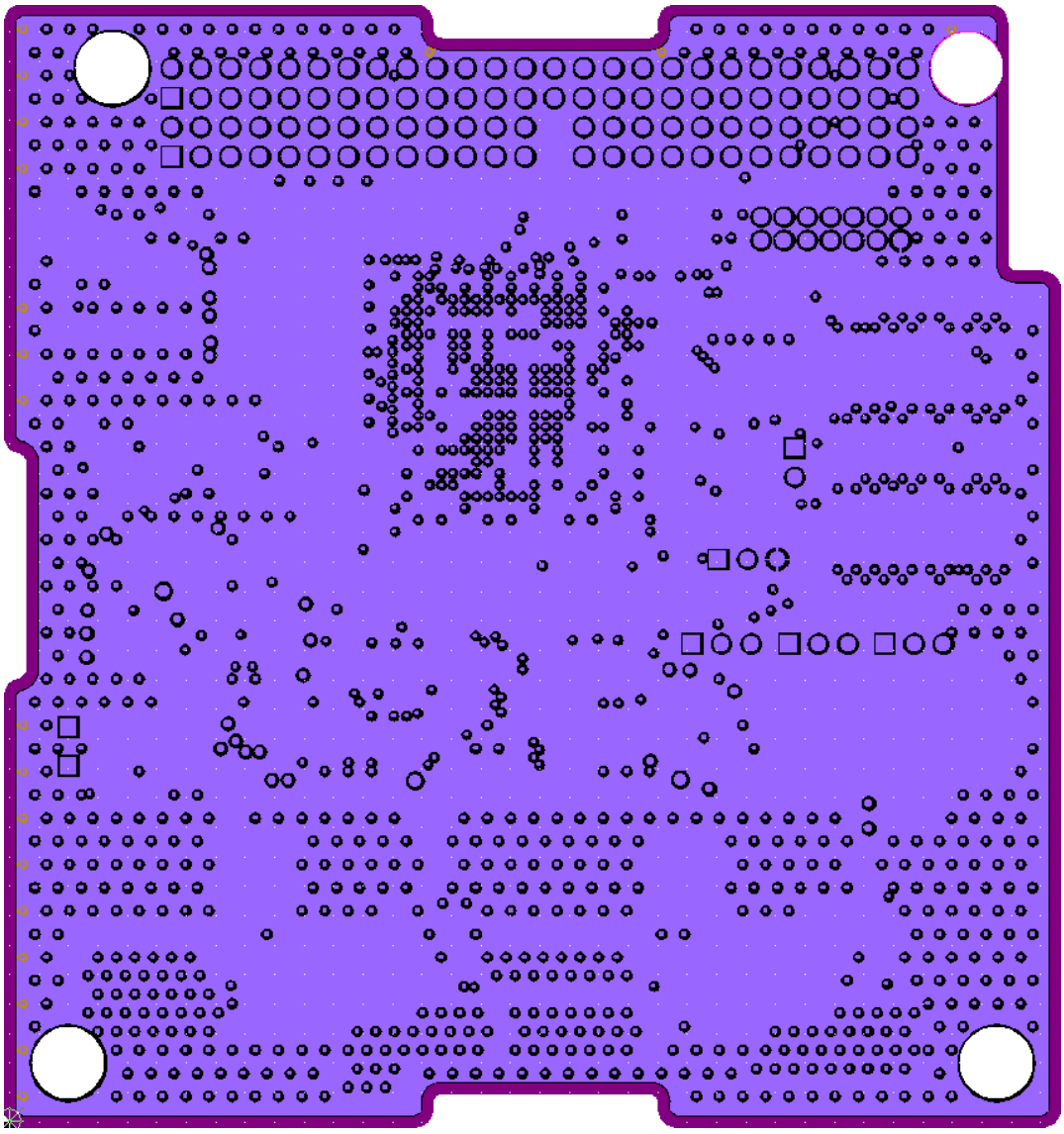
B.2. Inner layer 1



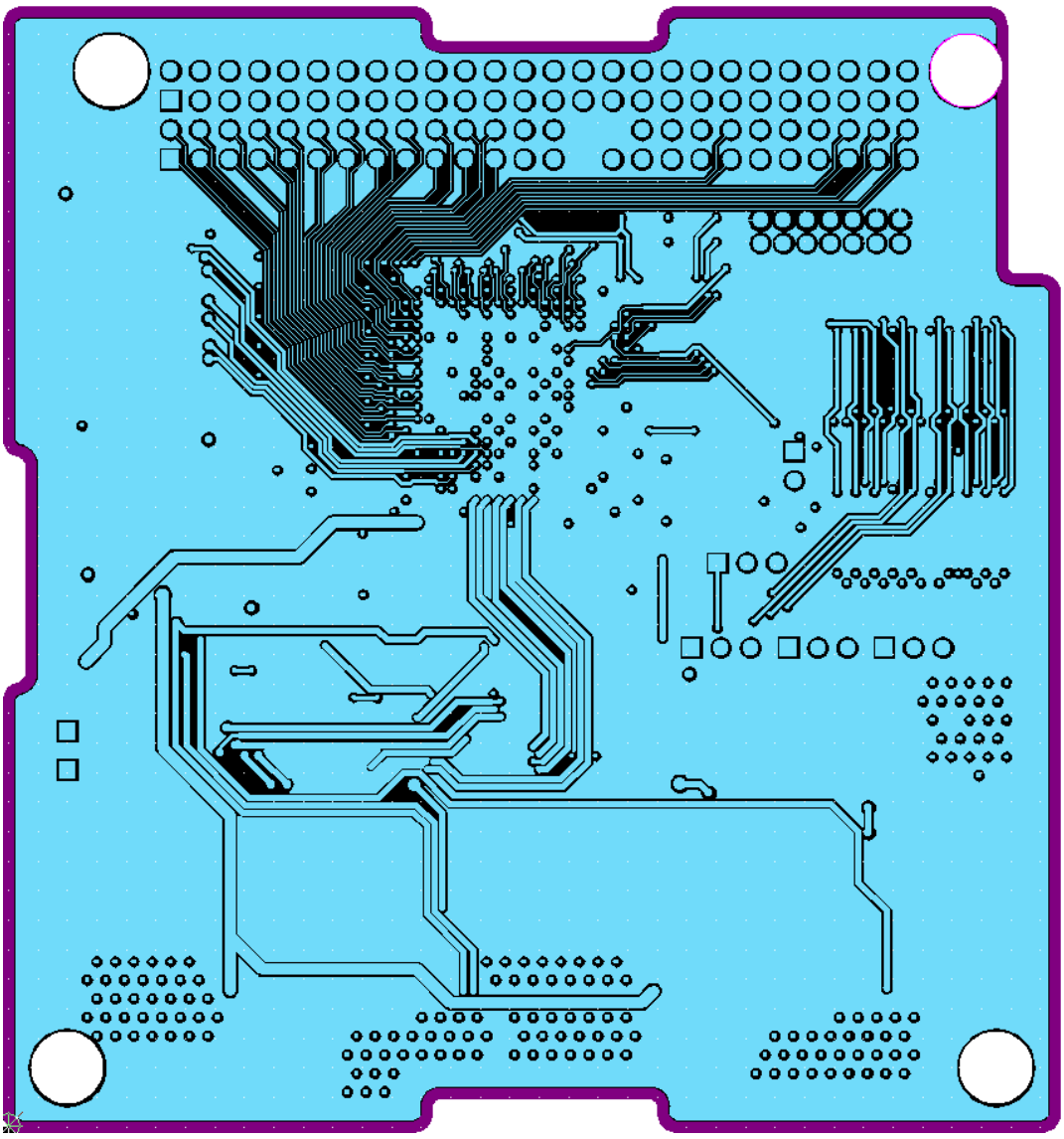
B.3. Inner layer 2



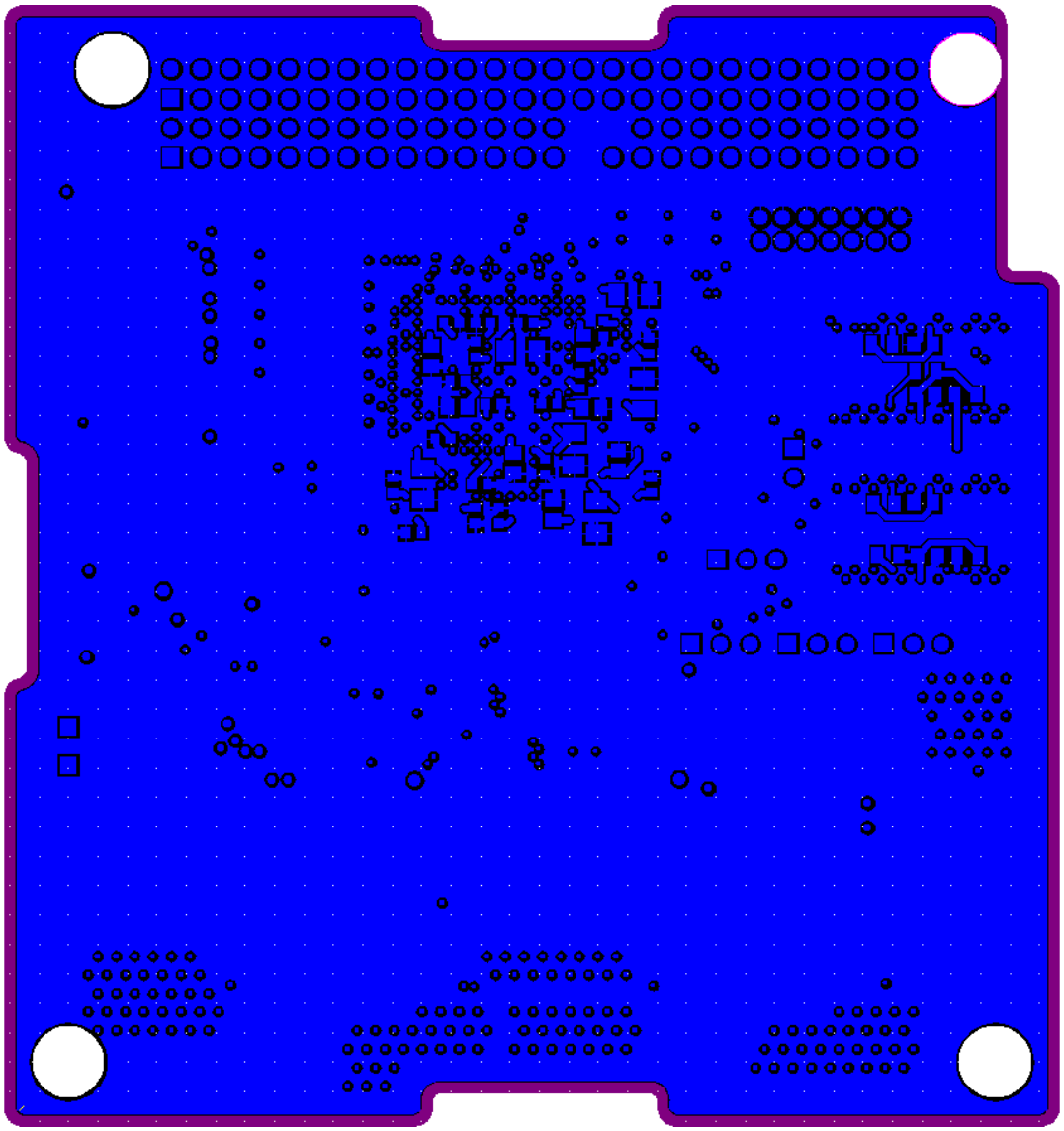
B.4. Inner layer 3



B.5. Inner layer 4



B.6. Bottom layer



Annex C. Bill of materials

Designator	Value	Description	Package	Quantity	Total Price [euro]
C1, C2, C3, C4, C5, C6, C7, C8, C9, C41, C43, C47, C48, C52, C55, C57, C58, C59, C60, C61, C62, C63, C64, C80, C83, C84, C85	0.1 µF, 50 V	Ceramic Capacitor, X7R	C0805	27	0.98
C44, C45, C49, C50, C51, C53, C54, C56, C65, C81	0.01 µF, 25 V	Ceramic Capacitor, X7R	C0805	10	0.36
C42, C46, C67, C73, C79, C95	1 µF, 16 V	Ceramic Capacitor, X7R	C0805	6	0.22
C15, C16, C19, C23, C28, C31, C39, C68, C74, C78, C82, C94	4.7 µF, 16 V	Ceramic Capacitor, X7R	C0805	12	0.45

Designator	Value	Description	Package	Quantity	Total Price [euro]
C66, C72, C75, C86, C88, C89, C90, C91, C92, C93	22 µF, 10 V	Ceramic Capacitor, X7R	C0805	10	2.25
C70, C76	100 pF, 50 V	Ceramic Capacitor, X7R	C0805	2	0.045
C10, C12, C20, C25, C29, C37, C69, C87	100uF 6.3V ±20%	Ceramic Capacitor, X7R	C1206	8	4.16
C11, C13, C14, C17, C18, C21, C22, C24, C26, C27, C30, C32, C33, C34, C35, C36, C38, C40	0.47 µF, 16 V	Ceramic Capacitor, X7R	C0603	18	0.63
C71, C77	22 nF, 50 V	Ceramic Capacitor, X7R	C0805	2	0.045
H1, H2		PC/104(TM) Elevated Socket Strip, Through-hole, Vertical, 2.54 mm Pitch, 52-Pin, Female	SMTC-ESQ-126-23-X-D	2	10
J1	2201778-1	Memory Socket		1	1.37
P3		Header, 7-Pin, Dual row		1	
P1, P4, P5, P6		Header, 3-Pin		4	

Designator	Value	Description	Package	Quantity	Total Price [euro]
P2		Header, 2-Pin		1	
Q1	IPD50P03P4L-11, 50 A, 8.3 mΩ	Power-Transistor	TO252-3	1	0.93
R1, R3, R19, R20, R21, R22, R24, R25, R26, R27	0 Ω, 50V	Chip Resistor	R0805	10	0.060
R2, R4, R5, R6, R7, R8, R9, R12, R14, R15, R16, R17, R18	4.7 kΩ, 50V	Chip Resistor	R0805	13	0.078
R10	10 kΩ, 50V	Chip Resistor	R0805	1	0.006
R11, R13	330 Ω, 50V	Chip Resistor	R0805	2	0.012
R23, R60, R61, R62, R63, R64	47 kΩ, 50V	Chip Resistor	R0805	6	0.036
R28, R29, R30, R31, R33, R35, R37, R51, R54	1 kΩ, 50V	Chip Resistor	R0805	9	0.054
R32, R36	10 kΩ	Thermistor, NTC	R0805	2	0.2
R34, R38	5.6 kΩ, 100V, ±0.05%	Chip Resistor	R0805	2	1.3

Designator	Value	Description	Package	Quantity	Total Price [euro]
R40	100 kΩ, 50V	Chip Resistor	R0805	1	0.006
R42	40.2 kΩ, 50V	Chip Resistor	R0805	1	0.006
R47, R48, R49	5 mΩ, 1W	Sense Resistor	R1206	3	1.43
R50, R53	75 kΩ, 50V	Chip Resistor	R0805	2	0.012
R52	150 kΩ, 50V	Chip Resistor	R0805	1	0.006
R55	34.8 kΩ, 50V	Chip Resistor	R0805	1	0.006
R56	169 kΩ, 50V	Chip Resistor	R0805	1	0.006
R57	53.6 kΩ, 50V	Chip Resistor	R0805	1	0.006
R58	357 kΩ, 50V	Chip Resistor	R0805	1	0.006
R59	66.5 kΩ, 50V	Chip Resistor	R0805	1	0.006
U1	XA6SLX45	Spartan-6 LX 1.2V FPGA	FGG484	1	82
U2, U3	MR4A08B	MRAM	TSOP-2-44	2	74
U4	SN74AHCT1G126-Q1	Buffer Gate	SC-70	1	0.45
U5	TPS3813K33MDBVREP	Enhanced Product Processor Supervisory Circuit with Window-Watchdog	6-pin SOT-23	1	5.87
U6	SN74HC595-EP	8-BIT Shift Register	SOP-16	1	4.85

Designator	Value	Description	Package	Quantity	Total Price [euro]
U7	SN74LV4053A-EP	Analog Multiplexer	SOP-16	1	2.13
U8	DSC1101	Low-Jitter CMOS Oscillator	3.2x2.5mm	1	1.2
U9	AD7124-4	Sigma-Delta ADC	TSSOP-24	1	9.9
U10	LM2902-EP	Low Power Quad Operational Amplifier	14-pin TSSOP	1	1.7
U11	TPS3307-18MDREP	Enhanced Product Triple Processor Supervisor	8-pin SOIC	1	6.2
U12, U13, U14	INA214-Q1	Current-sense amplifier	SC-70	3	4.5
U15, U16	LMZ10504EXTTZE	Step-Down Converter	7 pin TO-PMOD	2	40.5
U17	TPS76201QDBVRQ1	Single Output Automotive LDO, 100 mA, Adjustable 0.7 to 5.5 V Output, 2.7 to 10 V Input	5-pin SOT-23	1	1.24
U18	TPS79333DBVREP	Single Output LDO, 200 mA, Fixed 3.3 V Output, 2.7 to 5.5 V Input	5-pin SOT-23	1	0.95
U19	LM4128DQ1MF2.0	Voltage Reference	5-pin SOT-23	1	2.05
Total Price [euro]					168.4

Annex D. Stratospheric flight

Figure 34: The control unit placed in a box together with a radiation dosimeter

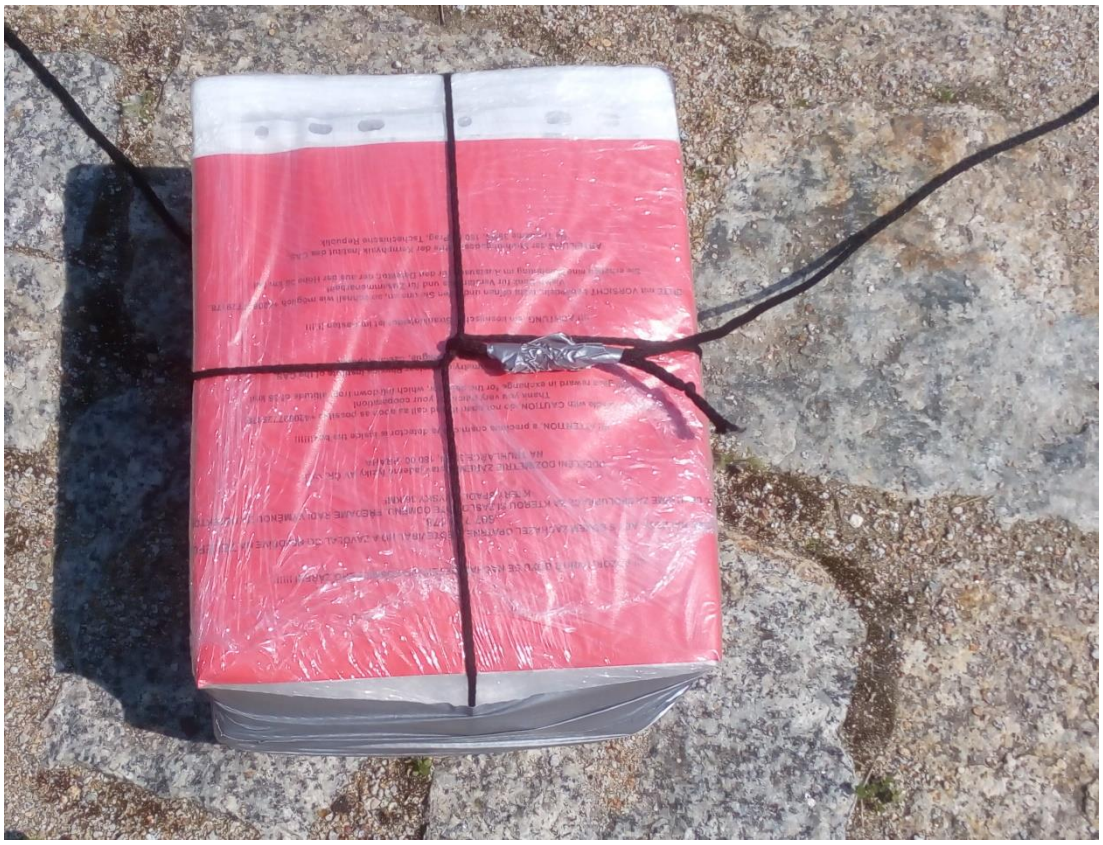


Figure 35: The box, attached to the balloon

Figure 36 and 37: Inflating the balloon and its start