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VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION
DEPARTMENT OF RADIO ELECTRONICS

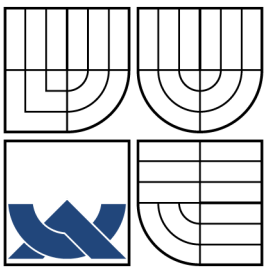
FAKULTA ELEKTROTECHNIKY A KOMUNIKAČNÍCH TECHNOLOGIÍ
ÚSTAV RADIOELEKTRONIKY

IMPLEMENTATION OF SPECTRAL SENSING METHODS IN FPGA

MASTER'S THESIS
DIPLOMOVÁ PRÁCE

AUTHOR Bc. ONDŘEJ MAŇAS
AUTOR PRÁCE

Brno 2015



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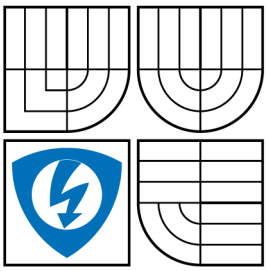

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IMPLEMENTATION OF SPECTRAL SENSING METHODS IN FPGA

IMPLEMENTACE METOD SNÍMÁNÍ SPEKTRA V OBVODU FPGA

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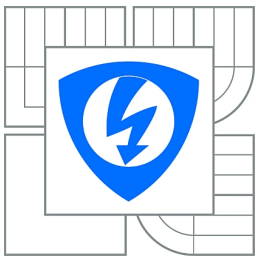
BRNO 2015



VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

Fakulta elektrotechniky a komunikačních technologií

Ústav radioelektroniky

Diplomová práce

magisterský navazující studijní obor
Elektronika a sdělovací technika

Student:	Bc. Ondřej Maňas	***ID:***	134357
Ročník:	2	***Akademický rok:***	2014/2015

NÁZEV TÉMATU:

Implementace metody snímání spektra v obvodu FPGA

POKYNY PRO VYPRACOVÁNÍ:

Seznamte se s problematikou snímání spektra (spectrum sensing) a s platformou skládající se z front-endu s přímou konverzí, deskou s A/D D/A převodníky a vývojovou deskou s FPGA, používanou na Univerzitě v Ulmu. V prostředí MATLAB simulujte vybraný algoritmus snímání spektra, například detektor založený na cyklostacionaritě. Vyhodnoťte jeho vlastnosti na vybraných komunikačních signálech.

Implementujte vámi zvolený detektor v obvodu FPGA na platformě pro sledování spektra, vyvinuté na Univerzitě v Ulmu. Správnou funkci ověřte nejprve simulací, poté proveďte testy na reálných komunikačních signálech.

DOPORUČENÁ LITERATURA:

[1] AXELL, E., et al., Spectrum sensing for cognitive radio: state of the art and recent advances, IEEE Signal processing magazine. 2012, vol.29, no.3, pp.101-116.

[2] KOSUNEN, M.et al., Survey and analysis of cyclostationary signal detector implementations on FPGA, IEEE journal on emerging and selected topics in circuits and systems. 2013, vol.3, no.4, p.541-551.

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Vedoucí práce: doc. Ing. Roman Maršálek, Ph.D.
Konzultanti diplomové práce:

doc. Ing. Tomáš Kratochvíl, Ph.D.
Předseda oborové rady

ABSTRACT

The aim of this thesis is software modelling and hardware implementation of a spectral sensing algorithm based on cyclostationary based detection. The proposed detector is fully implemented in FPGA and tested under further measurements in the real RF environment.

KEYWORDS

Spectral sensing, Detector, Cyclostationary based detection, FPGA

ABSTRAKT

Cílem této práce je návrh softwarového modelu a hardwarová implementace algoritmu snímání spektra založeného na cyklostacionární detekci. Navrhnutý detektor je plně implementován do obvodu FPGA a dále testován za podmínek měření v reálném rádiovém prostředí

KLÍČOVÁ SLOVA

Snímání spektra, Detektor, Cyklostacionární detektor, FPGA

MAŇAS, Ondřej *Implementation of spectral sensing methods in FPGA*: master's thesis. Brno: Brno University of Technology, Faculty of Electrical Engineering and Communication, Department of Radio Electronics, 2015. 84 p. Supervised by doc. Ing. Roman Maršálek, Ph.D.

DECLARATION

I declare that I have written my master's thesis on the theme of "Implementation of spectral sensing methods in FPGA" independently, under the guidance of the master's thesis supervisor and using the technical literature and other sources of information which are all quoted in the thesis and detailed in the list of literature at the end of the thesis.

As the author of the master's thesis I furthermore declare that, as regards the creation of this master's thesis, I have not infringed any copyright. In particular, I have not unlawfully encroached on anyone's personal and/or ownership rights and I am fully aware of the consequences in the case of breaking Regulation § 11 and the following of the Copyright Act No 121/2000 Sb., and of the rights related to intellectual property right and changes in some Acts (Intellectual Property Act) and formulated in later regulations, inclusive of the possible consequences resulting from the provisions of Criminal Act No 40/2009 Sb., Section 2, Head VI, Part 4.

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EVROPSKÁ UNIE
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2007–13
OP Výzkum a vývoj pro inovace

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INTRODUCTION

During the last decade, the world has witnessed considerable steps forward in many fields of technology. In the coverage of wireless communication technology, obtained data rates are certainly increasing by utilizing effective modulation schemes, coding techniques and advanced digital signal processing algorithms in general. Consequently user requirements on data rates or connectivity, wherever enabled, are increasing as well. It is essential that this trend never stops. Even though some issues have already been resolved, not a few great steps are still waiting for their accomplishment. One of these steps could be a solving spectral scarcity of the most used communication channels which have appeared.

The motivation for finding the solution is for example deployment of frequently mentioned Internet of Things (IoT). IoT is a concept where every device, which can offer any part of relevant information or controls, is connected into one network ensuring real time connectivity with the data central. One of the major parts is wireless connection. Therefore, during the deployment of IoT, a demand on supplying communication ability for a lot of new radio active devices under already established radio networks can be expected. As a result, engineers face managing limited channel resources and many users who desire allocation of those worthy resources.

In terms of ensuring the communication ability, the channel capacity is considered. The channel capacity is one, not only one, of the basic channel parameters. The well-known Shannon's Theorem (1) gives an upper bound of the channel capacity C, as a function of the available bandwidth B and the signal-to-noise ratio $\frac{S}{N}$ of the channel.

$$C = B \cdot \log_2 \left(1 + \frac{S}{N}\right) \tag{1}$$

Thus, the capacity of the channel can be increased by increasing B or $\frac{S}{N}$. The carrier frequency and these key parameters such as B and maximal signal power S_{max} are ordinarily legitimized for any frequency range by authorities, for example International Telecommunication union, Czech Telecommunication Union etc. Frequency bands are classified as environmental resources. The goal of this order is to protect providers of telecommunication services like mobile communication, broadcast television etc. These privileged users are called Primary Users (PU). An user without a privilege is called Secondary User. Nowadays, perspective spectral resources are almost occupied. For this reason, allocating free frequencies for any kind of new services (IoT) or expanding present services has begun to turn into a juristic and engineering issue.

One of the solutions how to reduce this essential problem is using higher RF bands. This tendency is a already running process which stretches back to the be-

ginnings of RF communication. The bottleneck is that the presence of water and oxygen in the air has very negative influence on atmosphere absorption which comes out especially in higher frequencies. The first sharp attenuation peak occurs at circa 22 GHz. More details can be found in [4]. So, usage of these channels are less cost-effective in terms of long range communications. This is one more reason to be focused on the optimization of today's RF band allocations structure.

In terms of recent utilization pattern, Primary User occupied allocated frequency band which is used to provide its services. Consequently, PU owns concession and cannot be disturbed. However, an occupied band could even be used by another user only in that manner. This condition is known as coexistent. Based on measurements and analyses which have been made on resource utilization (for example [5]) it is known that not every PU's channel in every band is always occupied. Thus, in time variant free frequency bands alias white spaces can be figured out and used by non-privileged SU. This opportunistic white space re-usage is mostly called Dynamic Spectrum Access (DSA). A simplified communication channels utilization based on DSA is illustrated in Fig. 1, where secondary user changes its communication channel parameters based on opportunistic unoccupied channel utilization.

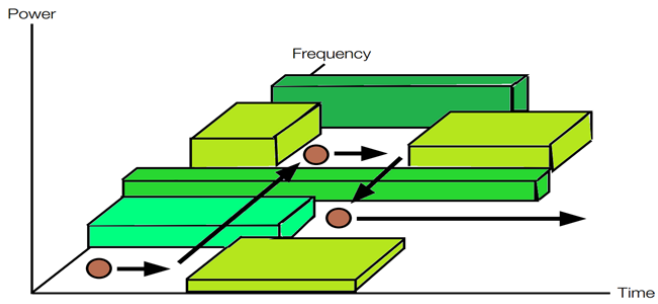


Fig. 1: Illustration of simplified DSA model of communication channels utilization – SU channel utilization is illustrated as a brown circle and PU's are illustrated as green rectangles [1]

. The concept of cognitive radio (CR) describes devices or radios which can - by reconfiguring their broadcasting parameters - ensure the ability to dynamically change channel utilization and simultaneously cooperate with other cognitive radios in its vicinity. The first proposals of cognitive radio possibilities were introduced by Joseph Mitola in 1998. This is Mitola's definition of cognitive radio:

> The point in which wireless personal digital assistants (PDAs) and the related networks are sufficiently computationally intelligent about radio resources and related computer-to-computer communications to detect user communications needs as a function of use context, and to provide radio resources and wireless services most appropriate to those needs.

Recently, deployment of cognitive radios in real environment is even standardised. IEEE standardised network communication which uses white spaces in television broadcast frequency bands. This standard is marked as 802.22 WRAN (Wireless Regional Area Network). The Next IEEE standard which works in TV white spaces is marked as 802.11af. This standard is dedicated for widely used computer networking known as Wi-Fi.

The key task of CRs is that secondary networks find white spaces and facilitate their optimal utilization. For the purpose of white space determining several techniques called spectral sensing methods are used. The aim of this thesis is the evaluation of mostly used sensing methods with consideration of their hardware implementation. One of these methods will be selected and implemented in FPGA. Moreover, the performance of implemented detector will be evaluated under PU's signals in the real RF environment. An implementation and evaluation will be done on a sensing platform which is dedicated for research and development of cognitive radio networks. The platform is developed at The University of Ulm, by Institute of Electron Devices and Circuits.

Based on measurements which proved that TV channels are a very opportunistic environment for secondary networks deployment, this thesis is certainly focused on sensing these TV services [5]. The TV broadcasting is also called Digital Video Broadcasting (DVB). In consideration on Terrestrial DVB (DVB-T), providers employ a modulation technique mostly used by other services as well. It is OFDM (Orthogonal frequency-division multiplexing). Hence, a developed detector dedicated for DVB-T channels would theoretically be possible to use for sensing other OFDM-based services.

1 THE SPECTRAL SENSING PLATFORM

The implementation of cognitive radio based on secondary networks into a scheme of already deployed primary services is not fully standardised. Even physical layer of CR is not standardised as well. CR is supposed to operate under a wide range of PU frequencies to increase a probability of finding unused channels. Requirements on a wideband sensing lead to a development of special receivers dedicated to a CR physic layer. A hardware of these receivers is rather called sensing platforms.

Selected platform introduced in [18] is a chain of particular devices dedicated to running and testing spectral sensing tasks and evaluating them. The platform is based on an SDR (Software Defined Radio) concept. Hence, the platform achieves capability to be flexible configured to test advanced sensing algorithms. As a classic diagram of Software Defined Radio receiver, the platform is consists of an RF front-end, an AD Converter and a baseband processing unit. These three blocks are described in the next sections.

1.1 Software radio and Software defined radio

A motivation for Software Radio and Software Defined Radio is that Cognitive Radio dynamically changes transceiver parameters as a reaction of actual conditions in the network. Due to, CR is required to include different communication building blocks to its physic layer. Furthermore, in case of spectral sensing, information about situation in network are gained by set of detection algorithms implemented in the layer as well. Hence, realizations CR's physic layer based on conventional analogue radio concept is not recently possible.

1.1.1 Software radio

Software radio contains standard subsystems like converters, modulators, filters etc. However, these components are defined by software description. From a hardware point of view, antennas and possibly circulator are directly connected to an AD Converter which converts analogue signal to digital representation. Furthermore, a set of mathematical operations recquired to gain relevant information is executed embedded. Software Radio has a set of advantages which are also a motivation for a development and deployment. Here are named several of them [6]:

- Reconfigurability,
- Re-usability,
- Reliability,
- Consistency and Stability of Parameters,

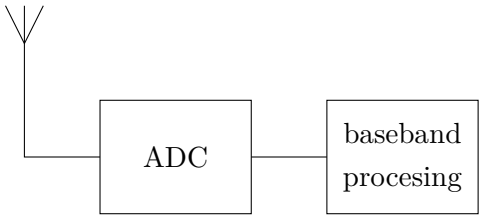


Fig. 1.1: Software radio block diagram

This concept is based on a fast ADC which can properly sample communication signals on a radio frequencies. In consideration on usability of Software Radio in conventional frequency bands, a demand on an ADC's sampling rate fulfilling Nyquist rule cannot be recently met effectively.

1.1.2 Software defined radio

In terms of reducing requirements on the ADC and still preserve advantages of SR. The ADC is moved far from an antenna into a baseband. A first down conversion is realized by an analogue part of radio called front-end. This is the first stage, where an unusable part of a signal's spectrum is suppressed converted to baseband frequencies. As a result, a demand on ADC is less critical. The reduced demand leads to decreased cost of the ADC which makes SDR available for wider usage.

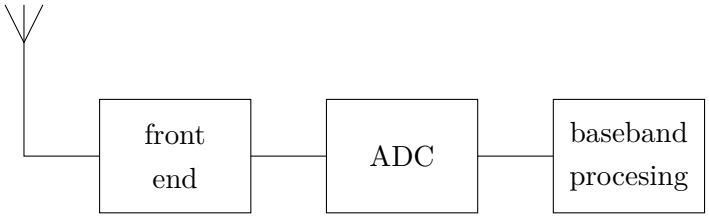


Fig. 1.2: Software defined radio block diagram

Furthermore, a radio's baseband processing unit based on DSP is necessary for a modern digital communication. As an example, OFDM is a widely used type of modulation technique(DVB-T, WiMax, LTE etc.). This technique employs Fourier transform which is generally implemented in transmitters and receivers as a functional DSP blocks.

1.2 RF front-end

CR is dedicated to operate under very low SNR to discriminate presence of faded PU and SU signals. A requirement on sensitivity is involved in whole detection process.

The sensitivity is defined as the weakest signal which can be reliably detected. The sensitivity level defined by a RF front-end depends on resulted noise figure at a front-end output. Consequently, CR operates over perspective radio frequencies up to approximately 6 GHz, where services e.i. DVB-T, GSM, UMTS, LTE, WiMAX etc. are situated. For speed up scanning time over all bands of interest, The front-end with wide baseband (BB) bandwidth is suitable. Since the bandwidth determines a number of tuning steps required to sense all range of interested frequencies. As a result, in terms of wideband sensing, the sensing time relates to BB bandwidth. On the other hand, a design of a very wideband low noise receiver is a challenging step which follows many issues as harmonic mixing, keeping linearity, IQ imbalance etc [18].

1.2.1 Up / down heterodyne architecture

Very wideband receivers can suffer on a spectral overlapping during mixing by an unwanted harmonic down-conversion. It is typical in that case, whether the highest spectral component of baseband signal is higher then a mixing frequency. Due to this problem, an Up / down heterodyne architecture is employed. Hence, an RF input is firstly up-converted by tuned LO_1 to IF. By tuning of LO_1, a final desired band is selected. In the next step, adjacent bands are suppressed by a following IF bandpass filter. The filter bandpasses bandwidth and desired BB bandwidth is equal. The filter is designed to achieve a constant central frequency according to LO_2 which is employed in the next stage. The next stage realizes direct down-conversion into the baseband.

1.2.2 Multi-RFIC front-end

A functionality of the RF part of the platform is spread into several components. An amplification and the u / down conversion are implemented into three integrated circuits on the technology 0.25 μm SiGe:C BiCMOS. The whole sensing platform chain is depicted in Fig. 1.3. The RF input signal is gained by wideband discone an-

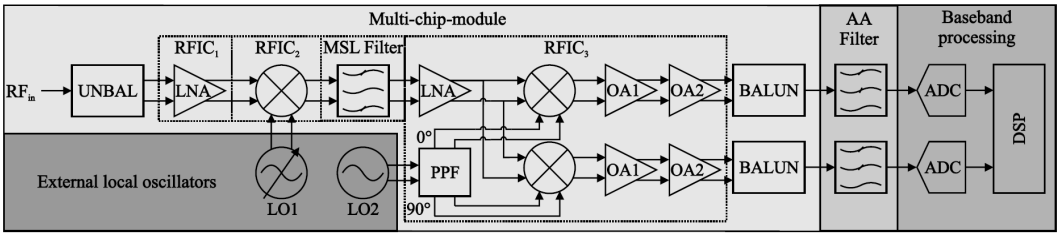


Fig. 1.3: The block diagram of spectrum sensing platform [18]

tenna. Since the RF front-end fits into fully differential architecture, a single ended signal on the input has to be transformed. For this purpose and pre-filtering, a balun is employed. The first RFIC in a chain is a wideband low-noise amplifier $RFIC_1$ followed by $RFIC_2$. $RFIC_2$ up-converts an incoming signal into a passband of IF cascode micro-strip filter. The filter is integrated into a common PCB for all RFICs and a power management circuit. The central frequency of implemented IF filter is 11.875 GHz. Filter's 3 dB bandwidth is 190 MHz. The filtered signal is again amplified and converted to baseband. The next step is the complex down-conversion realized by $RFIC_3$. Quadrature harmonic carriers are generated by a single poly-phase filter (PPF). After mixing, both channels are amplified by operational amplifiers to get beyond dynamic range of ADCs.

1.3 Analogue to digital converter

For conversion of analogue signal at the output of the front-end, dual channel AD Converter by Texas Instruments is used. At the same evaluation board there is placed Digital to Analogue Converter which is not used. The board is known as FMC150. An abbreviation FMC means that the board is plug-in expansion FMC connector connectible. The ADC has maximal sampling frequency at 250 MSPS. However, utilized sampling frequency is 245.76 MSPS. The property of this selected sampling rate is that, after a division by a power of 2, a result always contains only two non-zero digits. The resolution of ADC is 14 bits [19].

1.4 Baseband processor

The heart of software defined radio is a logic fabric known also as a baseband processor. A trunk task of the processor is a sample processing and information transfer to higher levels of OSI structure. The demand on a DSP performance, especially in case of SDR, is essential. The goal is very wideband signal processing as it was mentioned above. The sampling rate 250 Msps with the 14 bit wide word leads to a data throughput 7 Gbit per second at both ADC channels. An amount of data is demanding to usage of a special kind of digital processing unit.

The optimal solution of this performance issue is to design a unit dedicated exactly for targeted application. The unit is defined by fundamental building blocks of digital electronic systems as a flip-flops, lathes, logic gates etc. A realization of the unit as an integrated circuit is mostly called as ASIC (Application Specific Integrated Circuit). Every digital system implemented in one chip is fundamentally ASIC. A suitable option for a development and prototyping purpose is to utilize

of field programmable gate array (FPGA). In general, the FPGA consists of integrated logic building blocks connected through fully reconfigurable structure of connections. As a result, a strongly parallel architecture of the FPGA is very suitable for implementation of digital signal processing unit targeted on high throughput applications.

An advanced solution is integration of a the FPGA and a CPU core (Central Processing Unit) as one integrated circuit. This realization is known as a System on chip (SoC). As a result a time critical processing task can be implemented in the FPGA and e.g. human interface (desktop operation system), higher communication layer, statistics etc. can be executed be CPU [15].

1.4.1 Xilinx Virtex 6 [21]

For a baseband processing has been selected a high-performance FPGA Virtex 6 by Xilinx. As any FPGA, Virtex 6 consists of basic building blocks called function generators. They could be split into a logic part and a sequential part. The logic part otherwise called Look-Up Table (LUT) is an implementation of the truth table with six inputs and one output (Spartan 3–4 inputs). The output is connected to sequential part, especial to a D flip-flop (FF). The FF is controlled by an asynchronous set or reset and a clock enable signal. By combination of LUTs and FF, a logic slice is obtained. The Virtex 6 family Slice contains four LUTs and four D type flip-flops. Two slices are organized into Configuration Logic Blocks, which is connected to programmable switch matrix. Any digital system could be theoretically implemented into this structure.

A several primitives which are frequently used, its implementation by basic logic blocks are ineffective or those are digital-analogue blocks are implemented as a hard macro. It means that these entities are defined as building blocks as well as LUT or FF. Virtex 6 architecture employs hard defined blocks as RAMs, DSP48E1 slices, PLLs, clock management blocks, an ethernet first layer IP core etc.

Virtex 6's DSP48E1 slices are suitable for computing mathematical operations. The DSP48E1 basically consists of a 25×18 multiplier and an ALU, which realizes operation as summation and subtraction with arithmetic precision up to 48 bits. The multiplier and the ALU unit is placed to structure enabling efficient implementation of fundamental DSP entities e.g.FIR filter, Mixer, CIC filter etc.

DSP slices are placed into groups. Inside one group, slices are connected with their neighbours into several chains. This connection is realized by special dedicated buses. Each bus is accessible only by two neighbouring slices. DSP designs mapped into this topology can theoretically achieve speed clock of 500 MHz. This DSP slice

feature enables implementations of filter structures processing a sampled signal received directly from ADC output. A Virtex 6 version used in the baseband processor contains more then 400 DSP slices in one chip [16].

2 SPECTRAL SENSING AND DETECTION

The concept of Dynamic Spectrum Access (DSA) is fundamentally based on the ability to monitor unoccupied frequency bands and provide them for use. These bands are employed by secondary user to create secondary cognitive networks. In general, reliability and effectiveness of DSA implementation depend on the quality of gained information about an operating environment. Therefore, several requirements are targeted on spectral sensing methods and their implementation itself. Sensing methods should be resistant against all negative properties which wireless communication channels have. Those are, for example, noise uncertainty, channel fading, shadowing and channel variation in time (day/night, seasons, location). Another requirement is detection time which should be short enough to provide consistent information. Furthermore, spectral sensing methods should be fully independent of any information provided by PU. Totally independent sensing methods are called blind detection. Otherwise, standard requirements for devices deployed in the commercial sector are involved i.e. low computation complexity, low power consumption etc.

In this section, a brief detection problem description is presented. Further, mostly used types of detector methods are introduced. Based on the initial study, one of these detectors is selected for advanced examination.

2.1 Detection Theory

A final result of detection is a bipolar value which describes whether signal is present or absent. Therefore, the detection problem leads to two hypothesis:

Hypothesis H_0: channel is non-occupied
Hypothesis H_1: channel is occupied

In terms of signal detection:

Hypothesis H_0: received vector = noise
Hypothesis H_1: received vector = signal + noise

As a result, four situations can occur:

$P(H_0|H_0)$: Probability of correct noise detection P_{nd}
$P(H_0|H_1)$: Probability of missed detection P_{md}
$P(H_1|H_0)$: Probability of false alarm P_{fa}
$P(H_1|H_1)$: Probability of correct signal detection P_d

A reliability of detection is frequently characterized by probability of detection (P_d) and probability of false alarm (P_{fa}). Where low probability of detection results in increased interferences with PU. Whereas, higher false alarm rate increases the amount of missed spectral opportunities.

A final decision, whether a signal is present or absent is distinguished using a test metric. The test metric T represents evaluation of sensed signal. It means that signal presence or absence leads to observable changes of value of test metric. Hence it follows, the test metric is a monotonic function of signal to noise ratio (SNR). A determination of T is specific for every sensing method. As a result, the hypothesis problem can be rewritten as [25].

Hypothesis H_0: $\hat{T} = \epsilon$
Hypothesis H_1: $\hat{T} = T + \epsilon$,

where $\hat{T}$ is estimation of T by selected sensing algorithm. ϵ is a noise contribution to the test metric. The particular hypothesis is determine based on threshold T.

Probability P_d and P_{fa} directly depend on t examination. Based on probability density function (PDF) of particular number of observations of $\hat{T}$ for both hypothesis H_0 and H_1, P_d and P_{fa} can by estimated. P_{fa} can be determine from CMOS of H_0

distribution p_{H0}. Consequently, P_d can be determine from CMOS of H_1 distribution p_{H1}.

$$P_d = \int_t^{\infty} p_{H1}(T)\mathrm{d}T \tag{2.1}$$

$$P_{fa} = \int_t^{\infty} p_{H0}(T)\mathrm{d}T \tag{2.2}$$

Based on knowledge of probability distribution of $\hat{T}$ under H_0, which corresponds to that only noise presents. Neyman-Pearson test can be employed to set t under defined P_{fa}. Probability distribution for $\hat{T}$ under H_1 is not desired.

$$t = P^{-1}(1 - P_{fa}) \tag{2.3}$$

Receiver Operating Characteristic (ROC) describes relation between P_d and P_{fa} for scale of varied thresholds applied on observed test metrics $\hat{T}$.

2.2 Detection Methods

2.2.1 Matched Filter Detector

A detection based on Matched filter is an optional way for any communication system. A fundamental assumption is a piece of knowledge of detected signal such as bandwidth, modulating type, operating frequency etc. [7]. Matched filter employs a correlation between received signal $x(n)$ and known referred signal $s(n)$ of length N taps to maximize signal to noise ratio. Matched filter description is given below [8]:

$$T(x) = \sum_{n=1}^{N} x(n) \cdot s^*(n) \tag{2.4}$$

The assumption is also a key disadvantage of this methodology since PU signal has to be known and moreover each type of PU's system requires dedicated Matched filter in detector.

2.2.2 Energy Detector

Energy detection is method used in radiometry. The principle of this method is measuring signal power in narrow sub-bands in finite time and comparing them with a decision threshold as described as [8]:

$$T(x) = \sum_{n=1}^{N} |X(n)|^2 \tag{2.5}$$

Variable $x(n)$ is the signal in time domain, n is order of repetition and N is number of averages.

Energy detector can be equivalently implemented in frequency domain [13]:

$$P(f) = \frac{1}{N} \left| \sum_{n=1}^{N} x(n) \mathrm{e}^{-j2\pi fn} \right|^2 \tag{2.6}$$

Energy detector has many positive properties which lead to the fact that it is the most common method. Basically, energy detector is a blind detector operating under a very wide band of interest. The complexity of this detector is also suitable, since algorithm of Fast Fourier Transform could be employed. The performance of the detector depends on sensing time, especially on the number of averages N. On the other hand, the reliability of the detection depends on an estimation of an actual noise power level which complicates utilization of this detector. Therefore, use of some techniques as noise calibration [10] is required. This is a crucial disadvantage of energy detector especially in terms of detecting signal under negative SNR.

The sensing platform described in previous section is highly suitable for implementation of wideband energy based detector. More details about implementation are published in [17] and [18].

2.2.3 Cyclostationary Feature Detector

Communication signals have statistical properties which enable us to consider them as cyclostationary processes. A cyclostationary process can be described as a stationary process which is occurring periodically during observation. So, this unique pattern can be extracted and detected. The signal is assumed as cyclostationary if its nth-order non-linear transformation generates sine-wave components also called features. A second-order transformation is e.g. product of the signal with its delayed version [22]. For extracting the lowest sine-wave component, Cyclic Autocorrelation Function (CAF) is employed [24]. The test metric for second-order cyclostationary based detector can be described by this function.

$$\hat{R}_x^{\alpha}(\tau) = \frac{1}{N} \sum_{n=0}^{N-1} x(n) x^*(n-\tau) \mathrm{e}^{-j2\pi\alpha n/N} \tag{2.7}$$

A result $\hat{R}_x^{\alpha}(\tau)$ is amplitude and phase of the lowest sine wave component at a cyclic frequency α which is related to period of stationary process occurring. Variable τ defines the delay between the signal $x(n)$ and its copy.

The result of CAF can be used as the test metric, or rather its absolute value can. However, in [11] a statistical test is propose which determines the test metric

based on covariance matrix of CAF at another frequencies then α and estimating deviation.

Properties of signal which could be used for feature generation are e.g. sampling rate, sine-wave carrier signal, cyclic prefix and pulse-shape filter response etc. A disadvantage of this method is increased complexity. Information about α and τ are required.

2.2.4 Eigenvalue based Detection

The communication signal correlation properties can be also extracted by eigenvalue decomposition. As a first step, a determination of covariance matrix R_x from sampled signal $x(n)$ is required [13], [12].

$$R_x = \frac{1}{N}(XX^T) \tag{2.8}$$

Variable N is a cubic matrix dimension and X is matrix of received samples $x(n)$.

The next step is the estimation of eigenvalues vector. In cases where input signal samples x are correlated, eigenvalue vector of R_x has large eigenvalue spread. A difference between the smallest and largest value is employed to detection for example by maximal-minimal eigenvalue method [13].

$$T_{MME} = \frac{\max(\lambda)}{\min(\lambda)}; \tag{2.9}$$

In literature many sensing methods how estimate test metric for eigenvalue based spectrum sensing can be found. Basically, they can be divided into methods which use information about noise power and which do not [28]. The selected method MME is included in the second group.

A software model of eigenvalue based detector and its simulation of detection mostly used communication signals is present in next section.

2.3 Eigenvalue detector modelling

A detection method based on Eigenvalue (Eg.) decomposition could be included in the category of narrow band universal blind detection methodologies. In this section, an eigenvalue based detection is evaluated by software simulations. Finally, possibilities of implementation are introduced. The performance of the detection is determined based on software models of two mostly used communication signals. Those are OFDM following DVB-T standards [33], [34] and QPSK modulated.

2.3.1 Simplified DVB-T transmitter model

In this section, a simplified model of a DVB-T transmitter is described. In terms of the simplification, only a stream of OFDM symbols is generated. Symbols are consist of random generated data and unused carriers. The parameters of generated OFDM signal can be observed in Tab. 3.2 [34].

An OFDM architecture suggested by DVB-T(2k and 8k), is to parallel data into N_u branches. Each branch has its own modulator (BPSK, QPSK etc.). These branches are extended to N_c by constant value and transformed into time domain by IFFT. Other unused IFFT inputs are left to zeros. The result is one OFDM symbol in time domain. A Cyclic Prefix consisted of defined number of samples is copied from the end of symbol and added to the begining. The number could be $\frac{1}{4}$, $\frac{1}{8}$, $\frac{1}{16}$ and $\frac{1}{32}$ of symbol length. At the output of modulator is signal with B_{dvb} bandwidth.

Tab. 2.1: Basic parameter of 2k and 8k mode [34]

	2k	8k
IFFT/FFT width N_f	2048	8192
Number of carrier N_c	1705	6816
Number of useful carriers N_u	1512	6048
Modulation schemas	QPSK, BPSK, 16-QAM, 32-QAM etc.	
Cyclic prefixes CP	$\frac{1}{4}$, $\frac{1}{8}$, $\frac{1}{16}$, $\frac{1}{32}$	
Sampling Frequency F_{dvb}	64/7 MHz	64/7 MHz
Subcarrier spacing	4.4643 kHz	1.116 kHz
Bandwidth B_{dvb}	7.612 MHz	7.609 MHz

2.3.2 Simulation scenario

For the simulation scenarios an advanced test metric is selected in [13] as well.

$$T_E = \frac{\max\lambda}{\frac{1}{M}\sum_{i=0}^{M-1}\lambda} \tag{2.10}$$

The estimation of λ is the same as described in section 2.2.4. A divisor is replaced by mean value of λ. The set of measured T_E is obtain from 6000 measurements.

In a first scenario, QPSK based signal is chosen as a sensed signal. The symbol frequency is selected to 1 MHz. The signal is sampled with sampling rate 8 MHz. Therefore up-sampling factor (UF) is equal to 8. On the output of transmitter, a square root raised cosine (RC) filter with roll-of factor 0.3 is employed. Both modeled transmitters operate in additive white Gaussian noise (AWGN) channel under

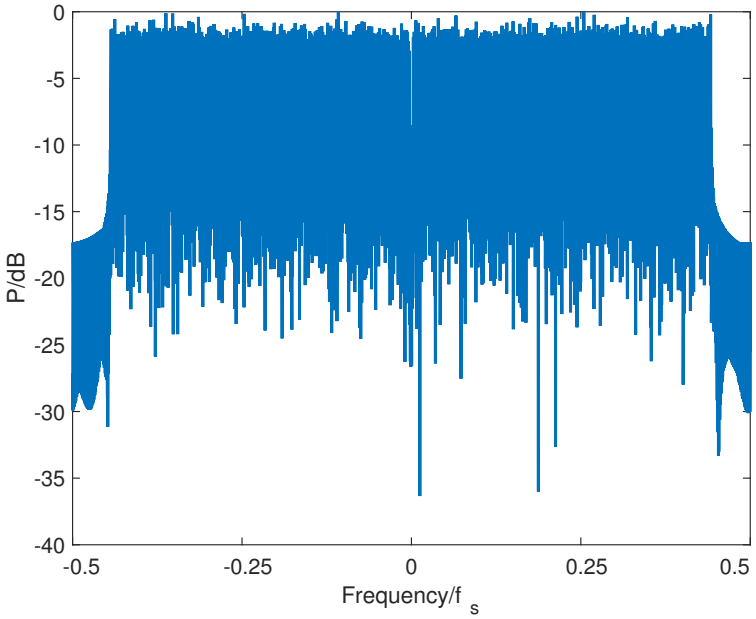
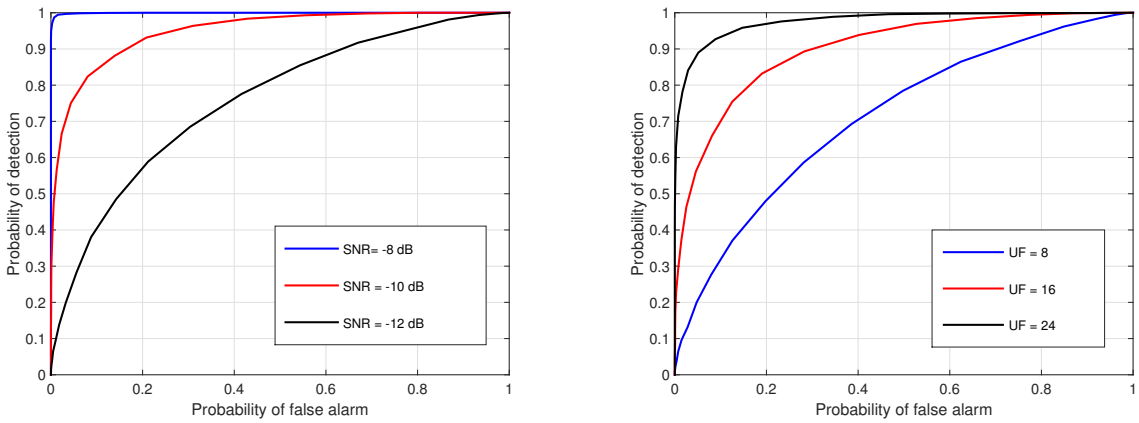


Fig. 2.1: Power Spectral Density of simulated DVB-T signal in 2k mode ($F_s = F_{dvb}$)

different levels of SNR. A size of covariance matrix N is chosen as 64. A resulted receiver operation characteristic is depicted in Fig. 2.2a. From the curve can be observe that for $SNR = -8\,\text{dB}$. Probability of detection is 100 % with corresponding P_{fa} 1 %. On other curves, sensitivity degradation influenced by decreased SNR is depicted.



(a) QPSK $N = 64$, $UF = 8$ (b) M_3 - DVB-T $N = 64$, $SNR = -8\,\text{dB}$

Fig. 2.2: Receiver operational characteristics for Eigenvalue based detection simulation scenario part 1

In the second scenario, DVB-T 2k signal ($CP\frac{1}{4}$, QPSK) is generated. The second

scenario contains three sub-scenarios $M1$, $M2$ and $M3$. A parameters map can be observed in Tab. 2.2. An ROC for M_1 and M_2 are depicted in Fig. A.1. Graphs describe influence of swept parameters on performance of Eg. detection. For parameters $UF = 8$, $SNR = -8\,\text{dB}$ and $N = 64$ and both scenarios, P_d is near to 100 % with corresponding P_{fa} 1 %. ROC of M_3 is depicted in Fig. 2.2b. In the sub-scenario M_3, a twice increased re-sampling factor UF improves P_d more than 20 % each next step of UF. It is related to $P_{fa} = 1\,\%$. This improvement is very suitable for wideband receivers, since a decimation stage with a high down-sampling rate can be decreased. Moreover, acquisition time is decreased as well.

Tab. 2.2: The parameters of the second scenario simulation

	N	SNR[dB]	UF
M_1	16, 32, 64	-8	8
M_2	64	-8, -10, -12,	8
M_3	64	-8	8, 16, 24

2.3.3 Survey of implementation

One of eigenvalue based detector disadvantages is computation complexity, especially in terms of complex number. An example of implementation of the eigenvalue decomposition of real matrix with size $N = 10$ is published in [30]. The next computational demanding step is matrix multiplication XX^T (2.8). It could be implemented as described in [29].

In consideration to implement the eigenvalue based detector into the sensing platform a suitable solution of computing large eigenvalue problems can be implementation into the system on chip SoC 1.4. In terms of the decomposition implementation, one of public C-libraries e.g. CLAPACK [31] can be theoretically used. LAPACK provides routines for solving linear algebra problems especially eigenvalue value problem. The core of CLAPACK (Linear Algebra PACK in C) is e.g. used by Mathworks Matlab [32]. By addition hardware acceleration implemented in a FPGA part of SoC, sufficient realization of the detector based on eigenvalue decomposition can be obtain. Moreover, in term of covariance matrix R_x computing, inefficiently memory operation and controls can be executed by a CPU. Hence it follows, the platform chain baseband processor ML605 would be replaced by e.g. ZedBoard with Xilinx zynq-7000 [15].

2.4 Cyclostationary OFDM based Detectection

The Orthogonal Frequency Multiple Access is a wide-band modulation technique dedicated to high-speed wireless networks. Its use is standardized by e.g. DVB-T, WiMAX, 4G and 3G networks etc. IEEE 802.22 Wireless Regional Area Network (WRAN) and IEEE 802.11af are developed for an implementation of spectral sharing principles at frequency bands allocated to television broadcast services. Proved by [5], underutilized DVB-T channels seem to be an opportunistic RF environment for a secondary networks set up.

Hence, a proposed OFDM detector is dedicated for DVB-T channels sensing. The simulation model of DVB-T system has been introduced in previous section.

2.4.1 Cyclostationary detection based on cyclic prefix

In terms of inter-symbol interference reduction, a cyclic prefix is added to each OFDM symbol. CP is a redundant sequence, which is copied in time domain from useful data signal. The CP is selected from the end of each symbol. Hence, the same sequence is repeated two times per one symbol. Therefore, the autocorrelation of actual received signal and one symbol duration delayed version of the signal is periodic in time. In Fig. 2.3, CP insertion of data sequence T is depicted. Moreover, A result of particular delay is illustrated as well. As a result, the OFDM signal can by assumed as second-order cyclostationary process [23].

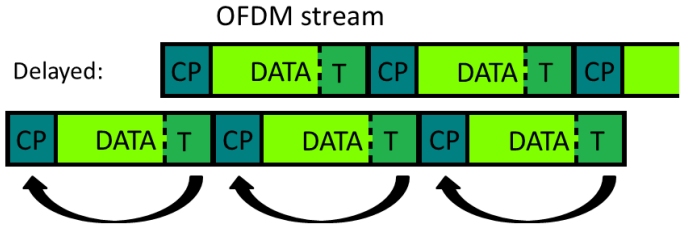


Fig. 2.3: Cyclic prefix insertion illustration with illustration of an one symbol duration delayed version of generated signal

Cyclostationary test

A detector proposed in [24] employs a conjugate cyclic autocorrelation function (CAF) $\hat{R}_x^{\alpha}$ at cyclic frequency α. A period of α is equal to duration of CP T_{CP} and OFDM symbol T_s.

$$\alpha = \frac{1}{T_{CP} \cdot T_s} \tag{2.11}$$

$$\hat{R}_x^\alpha = \frac{1}{N}\sum_{n=0}^{N-1} x(n)x^*(n-\tau)\mathrm{e}^{-j2\pi\alpha n/N} = R_x^\alpha + \epsilon(\alpha) = X(\alpha) + jY(\alpha) \tag{2.12}$$

Where $x(n)$ is the received signal of length N, τ is a lag parameter of the autocorrelation. Further, $\epsilon(\alpha)$ is estimation error. R_x^α is a determined frequency component at α. For the ability to detect OFDM signals, their parameters as τ and α have to be known. In the case of periodicity present in $x(n)x^*(n-\tau)$, R_x^α is a non-zero value. Otherwise R_x^α is equal to zero. The cyclic autocorrelation function for a set of frequencies k can be rewritten as [25].

$$F(k) = \frac{1}{N}\sum_{n=0}^{N-1} x(n)x^*(n-\tau)\mathrm{e}^{-j2\pi kn/N} = X(k) + jY(k) \tag{2.13}$$

Conceptually, an estimation of the CAF for the component at frequency α in eq. (2.12) is replaced by Fourier transform of $x(n)x^*(n-\tau)$ with N components. As a result, cyclic frequency α is an element of $\mathbf{A}$. Variable $\mathbf{A}$ is set of $\{k_0, k_1, k_2, \ldots k_N\}$. Therefore, it can be assumed that $F(\alpha)$ is equal $\hat{R}_x^\alpha$. Hence it follows to a two hypothesis problem [24].

$$H_0 : \forall\alpha \in \mathbf{A} \rightarrow \hat{R}_x^\alpha = \epsilon(\alpha) \tag{2.14}$$

$$H_1 : \exists\alpha \in \mathbf{A} \rightarrow \hat{R}_x^\alpha = R_x^\alpha(\alpha) + \epsilon(\alpha) \tag{2.15}$$

A test metric $\hat{T}_t$ for discrimination between H_0 and H_1 is defined as [25].

$$\hat{T}_t = \hat{r}\hat{\Sigma}^{-1}(\hat{r})^T \tag{2.16}$$

where $\hat{r}$ is arranged as vector from complex $\hat{R}_x^\alpha$ as [25].

$$\hat{r} = [\Re\{\hat{R}_x^{\alpha_k}\}, \Im\{\hat{R}_x^{\alpha_k}\}] = [X(\alpha), Y(\alpha)] \tag{2.17}$$

A covariance matrix $\hat{\Sigma}$ is estimated from $F(k)$ as follows

$$\begin{bmatrix} E\left[X(k)^2\right] & E\left[X(k)Y(k)\right] \\ E\left[X(k)Y(k)\right] & E\left[Y(k)^2\right] \end{bmatrix} \tag{2.18}$$

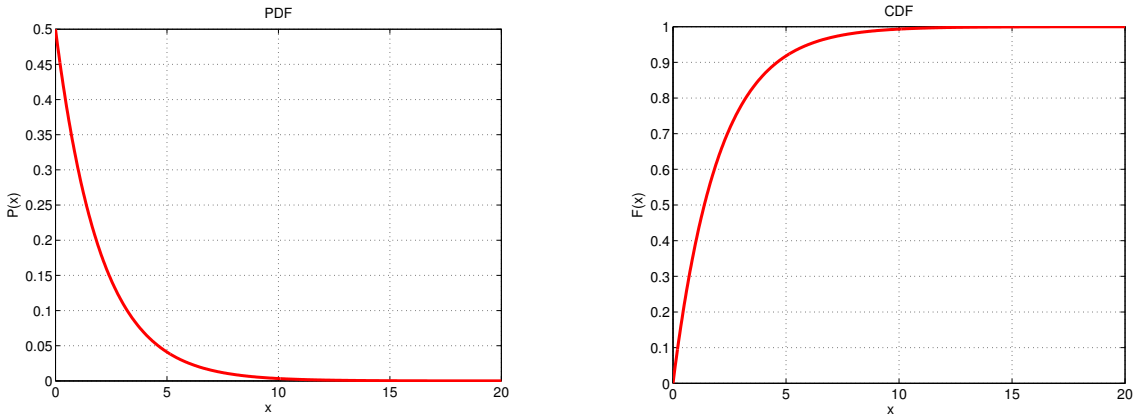
$$E\left[X(k)^2\right] = \frac{1}{N}\sum_{k=0}^{N-1} X(k)^2 \tag{2.19}$$

$$E\left[Y(k)^2\right] = \frac{1}{N}\sum_{k=0}^{N-1} Y(k)^2 \tag{2.20}$$

$$E\left[X(k)Y(k)\right] = \frac{1}{N}\sum_{k=0}^{N-1} X(k)Y(k) \tag{2.21}$$

The estimation error $\epsilon(k)$ is asymptotically normal zero mean complex random variable. Therefore in case of H_0, $\hat{T}_t$ for asymptotically normal zero mean random values is the distribution of chi-square with two degrees of freedom χ_2^2 [25]. The probability density function and cumulative distribution function of χ_2^2 is depicted in Fig. 2.4. As a result, constant P_{fa} rate can by determined from cumulative distribution function $F(\cdot)$ of $\hat{T}_t$ for H_0 hypothesis as follows [25].

$$F_{\chi_2^2}(T_t) > 1 - P_f a \tag{2.22}$$



(a) Probability density function of chi-square distribution with two degrees of freedom

(b) Cumulative distribution function of chi-square distribution with two degrees of freedom

Fig. 2.4: Functions of chi-square distribution with two degrees of freedom

Multi-cycle test metric

The test metric introduced in section below employs the component at the lowest cyclic frequency α. However, since the result of the autocorrelation is periodic signal with waveform close to a square wave, the spectrum of the autocorrelation $F(k)$ contains cyclic frequencies at higher multiples $m; m \in \mathbb{N}_{>1}$ of α. An involving $m\alpha$ for determination of a final test metric $\hat{T}_T$ is know as multi-cycle detection and can be described [27].

$$\hat{T}_T = \sum_{n=0}^{N-1} w_m \hat{T}_t^{\alpha_m} = \mathbf{w}^T\mathbf{T}. \tag{2.23}$$

Where

$$\mathbf{w} = [w_1, w_2, \ldots, w_L]^T, w \geq 0 \tag{2.24}$$

$$\sum_{n=0}^{N} w_m = 1 \tag{2.25}$$

is a weight vector length L for multi-cycle detection, a summation of w_m is equal to 1 to keep equality with single-cycle detector. Further,

$$\mathbf{T} = [\hat{T}_t^{\alpha_1}, \hat{T}_t^{\alpha_2}, \ldots, \hat{T}_t^{\alpha_L}]^T, \tag{2.26}$$

is vector of $\hat{T}_t^{\alpha_m}$, where every $\hat{T}_t^{\alpha_m}$ is estimated for α_m. A number for $\hat{T}_t^{\alpha_m}$ for estimation of $\hat{T}_T$ is defined as N.

The simplest version of multi-cycle detection employs weights set as $||\mathbf{w}|| = 1$ hence w_i is equal to $\frac{1}{L}$ eventually [27].

$$T_T = \frac{1}{L} \sum_{n=0}^{N-1} T_t^{\alpha_m} \tag{2.27}$$

Determination of $\mathbf{w}$ for cases different than eq. (2.27) leads to optimization problem [27] the solution of which is not a part of the content of this thesis.

2.4.2 Software model and Simulations

In order to prove the functionality of the proposal detector introduced in previous section. The detector model is tested on DVB-T signals in 2k mode operating in additive white noise channel. Parameters of DVB-T 2k can be observed in eq. (3.2).

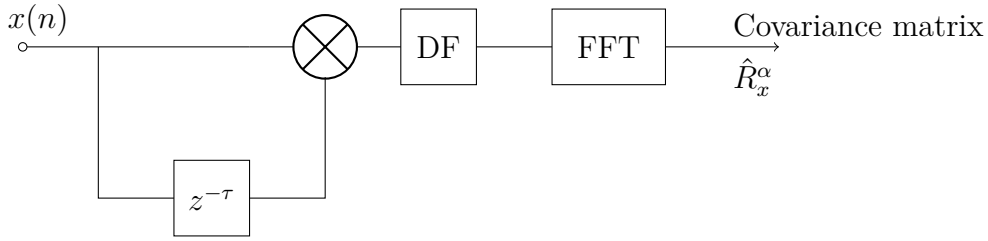


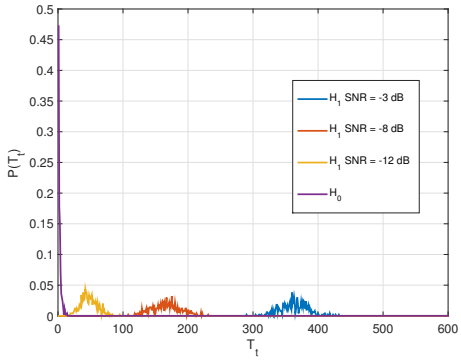
Fig. 2.5: CAF Scheme of OFDM Detector [24]

A block digram of the detector is depicted in Fig. 2.5. The diagram can be divided into two stages. The first stage is consist of a delay block $z^{-\tau}$, a complex multiplication and decimation filter with decimation factor DF. These three blocks are defined in time domain. The delay block realizes delayed version of an input signal $x(n)$. The delay τ is exactly one OFDM symbol without CP which is in term of 2k

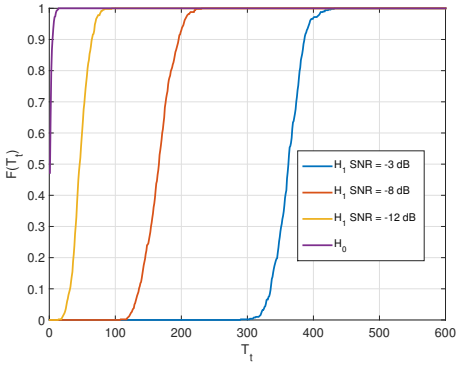
mode 2048 samples. The signal $x(n)$ is multiplied with conjugated $x^*(n-\tau)$. In terms of extracting components at cyclic frequencies α, between output of multiplication and FFT a decimation filter with decimation factor 32 is adopted. An FFT width N_{FFT} is selceted 2048.

At the beginning, it is essential to define a default simulation assumptions for simulation scenarios presented in this section below. The assumptions are shown in Tab. A.1.

Forthis initial set up, test of detector sensitivity under different level of $SNR = -3\,\text{dB}$, $-8\,\text{dB}$ and $-12\,\text{dB}$ is made. A probability density function of $\hat{T}_t$ under hypothesis H_1 and H_0 is depicted in Fig. 3.21. A cumulative distribution function is depicted in Fig. 2.6.



(a) PDF for H_1 and H_0 hypothesis based on $\hat{T}_t$



(b) CDF for H_1 and H_0 hypothesis based on $\hat{T}_t$

Fig. 2.6: Probability of detection and cumulative density function for hypothesis H_0 and H_1 based on test metric T_t for DVB-T 2k with CP equal to $\frac{1}{16}$

With decreasing SNR for each test, the distance between mean value T_t under H_1 and H_0 decrease as well. Even for a hypothesis test under SNR $= -12\,\text{dB}$, $100\,\%$ P_d under $0\,\%P_{fa}$ cannot by ensured. For hypothesis H_0, $\hat{T}_t$ has probability distribution has χ^2_2 as was presented in previous section. By applying eq. (2.4.1), the threshold based on selected constant P_{fa} can be set.

2.4.3 Decimation factor

By adopting a decimation filter with $DF = 8$ between complex multiplier and FFT, the data acquisition time is 8 time higher, however spectral estimation after multiplication is 8 time precise since the time of observation is 8 time higher as well.

Hence, a spectral coefficient which represents α is written as [24].

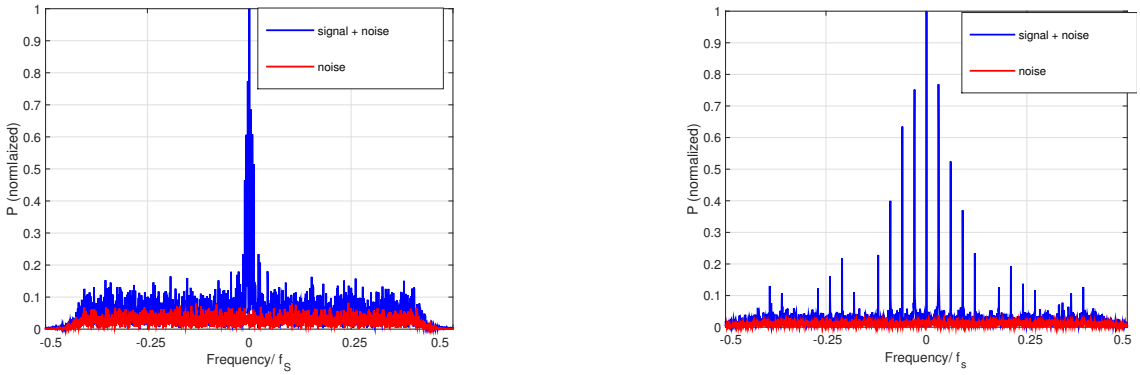
$$\alpha = \frac{N_{FFT} \cdot DF}{N_c + N_c \cdot CP}. \tag{2.28}$$

Figure 2.9 shows representations of cyclic spectra for different decimation factor DF. It can be observed that with increasing time of observation precision of spectral representation around cyclic frequency α is increased as well. Since the ratio of α to a FFT frequency step is proportional to DF. In case of sensing DVB-T signals, where symbols are in term of 2k mode 32 times higher than standardised in IEEE 802.g WLAN (detected in [24]). The higher DVB-T symbol duration leads to requirement of higher DF.

In the figure 2.9, the cyclic frequency α and its higher multiplies can be observed. Extra required parameters for determination α are $CP = \frac{1}{16}$, $Fs = \frac{64}{7}$ MHz and selected DF which is equal to 64. The equation (2.11) rewritten for absolute frequency α is

$$\alpha = \frac{1}{T_{CP} + T_s} = \frac{F_s}{N_c + N_c \cdot CP} = \frac{F_s}{2048 + 2048 \cdot \frac{1}{16}} = 4.2017 kHz. \tag{2.29}$$

The frequency 4.185 kHz on normalized frequency axis in Fig. 2.7b is at $4.185\,kHz/\frac{Fs}{64} = 0.0294[-]$



(a) Decimation Factor = 8

(b) Decimation Factor = 64

Fig. 2.7: Effect of Decimation factor on Cyclic spectrum estimation - DVB-T 2k (CP = 1/16, SNR = 10 dB, Fs = $\frac{64}{7}$ MHz

The selection of DF and N_{FFT} set the data acquisition time T_{aq} as is expressed in as

$$T_{aq} = \frac{N_{FFT} \cdot DF}{F_s} + T_s, \tag{2.30}$$

where T_s is required to store one symbol in the delay block at the beginning of sensing. The acquisition time for different DF and both DVB-T modes are shown in Tab. 2.3. In general, T_{aq} for 2k and 8k mode differs only in 0.672 ms, since 8k mode symbols are exactly 0.672 ms longer than symbol in 2k mode. Therefore, in approximately same T_{aq} time of sensing 8k signal, one third of the number of symbols is obtained. It leads to less extracted features in time domain, however this is compensated by a feature showing presence duration on the output of autocorrelation, which is three times longer than in case of 2k mode. Hence, detection performance of 2k and 8k mode is equal. This is proven by ROC for DVB-T 2k and 8k scenario. The ROC is depicted in Fig. 2.8. A deflection in performance is caused by longer sensing time in term of DVB-T 8k mode.

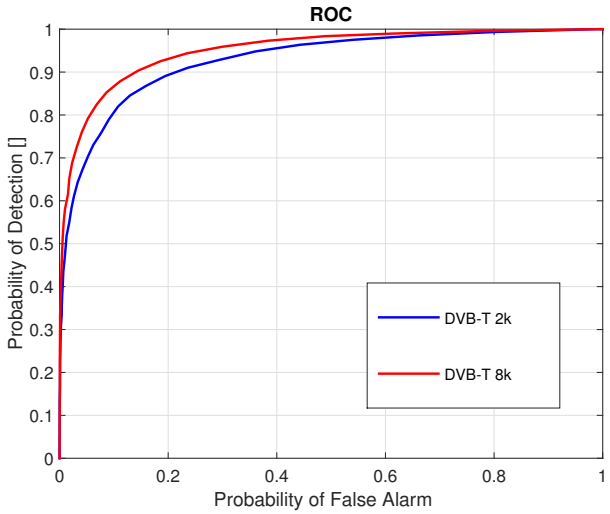


Fig. 2.8: Comparison of detection performance for 2k mode and 8k mode

A performance comparison for $DF = 16$, $DF = 32$ and $DF = 64$ is illustrated as ROC in Fig. 2.9a. A decreasing sensitivity is effected by decreasing T_{aq}.

In this section, T_{aq} is estimated for both DVB-T modes. However, the acquisition times determine how much time is required to gain all required data by channel sensing. The final sensing time depends on T_{aq} and additionally on the time required to process received data.

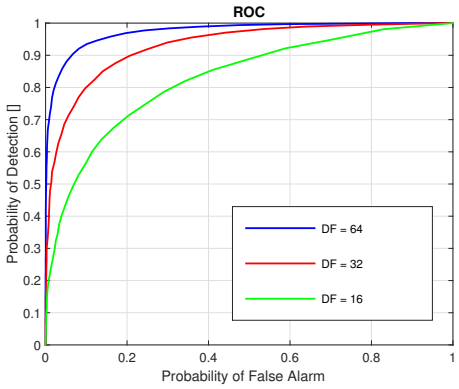
2.4.4 Cyclic prefix length

Conceptually, the cyclic prefix is employed to reduce inter symbol interference (ISI). On the other hand, CP is redundant piece of information of signal which decreases the resulting data throughout. Hence, the goal is to find a middle floor between ISI suppression and gained data rate. DVB-T provides a set of several length of cyclic

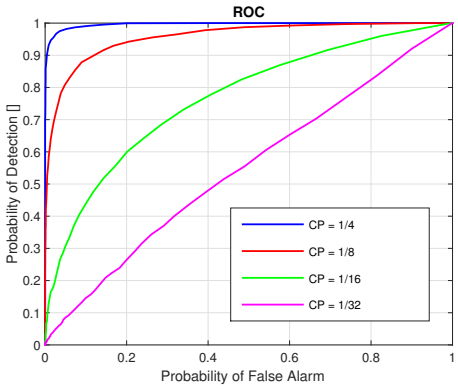
Tab. 2.3: Sensing acquisition time of DVB-T signal for different DF; $N_{FFT} = 2048$

DVB-T	**2k**		**8k**	
DF	T_{aq} [ms]	Num. of Sym.	T_{aq} [ms]	Num. of Sym.
16	3.8	17	4.5	5
32	7.4	33	8.1	9
64	14.6	65	15.2	17

prefix to optimally set balance. However, the length of CP has crucial influence on the result of cyclic autocorrelation function, since signal is correlated within duration of CP. The influence of CP length on detection performance is depicted in Fig. 2.9b.



(a) ROC for differ decimation factors



(b) ROC for differ CP lengths SNR = -12 dB

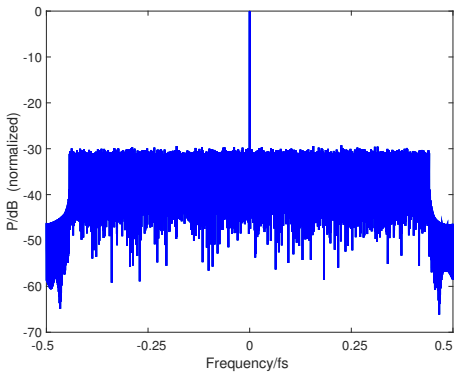
Fig. 2.9: Effect of Cyclic Prefix length and Decimation factor on Cyclic spectrum estimation on the detector performance

2.4.5 Carrier frequency inaccuracy and DC offset

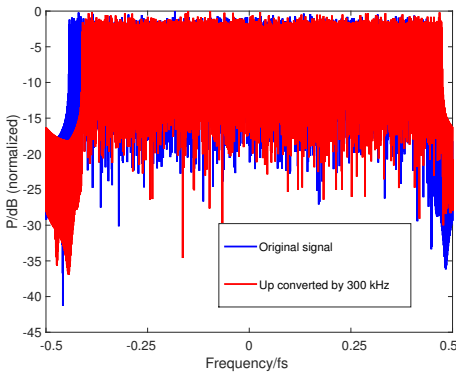
The sensing platform consists of the front-end based on a direct down conversion. For these type of receivers, a DC offset on the baseband output is typical. A robustness against DC offset is tested by adding DC part into DVB-T signal. The resulted PSD of DVB-T signal can be observed in Fig. 2.10a.

An influence of imprecise LO tuning is simulated by DVB-T signal shifted in frequency at 300 kHz. The PSD of original and shifted signal is depicted in Fig. 2.10b. In first two figures, resulted signals are depicted without noise addition. The cyclic

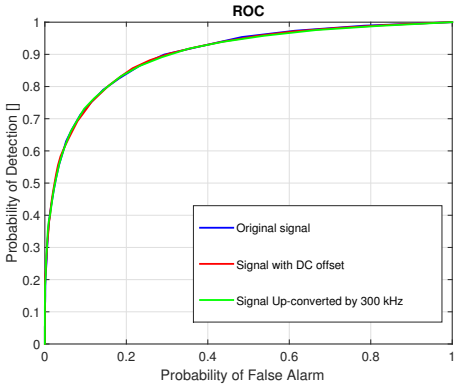
prefix is selected $\frac{1}{16}$. The sampling rate corresponds to original standardised rate equal to $\frac{64}{7}$ MHz.



(a) PSD of DVB-T 2k with DC offset



(b) PSD of original DVB-T 2k signal and up-converted version



(c) ROC for Original signal, signal with DC offset and up-converted version (SNR = -10 dB)

Based on results of simulation under SNR -10 dB illustrated in Fig. 2.10c, neither carrier frequency offset nor DC offset have negative influences on detection performance. However, this assumption is limited by DC offset amplitude utilized in the first simulation scenario. This can be also applied for the second scenario, where a carrier frequency offset is 300 kHz. A higher frequency offset was not selected, since Nyquist rule would be violated by the highest sub-carrier.

2.4.6 Multi-cycle detection

The multi-cycle detection was introduced in 2.4.1. For simulation scenario, the simplest version is chosen. Since all weights are equal to one, respectively to $\frac{1}{L}$. The variable L refers to number of employed cyclic frequencies. As an input, multiplies of α introduced in 2.4.1 are sorted. The component order at α can by determine as described in eq. (2.4.3). A negative α can by determined as $N_{fft} - \alpha$. A list of a twenty α components used in this scenario is attached in Tab. A.2. In the scenario, six detectors are involved. Names are given to detectors are in the format M_x, where x is the number of involved cyclic frequencies. A special case is a detector named S, it is one cycle detector used in all previous simulations.

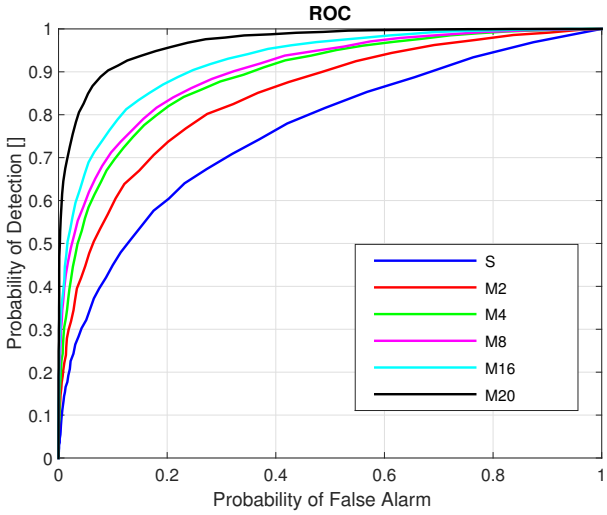


Fig. 2.11: ROC for single-cycle detector S and multi-cycle detectors M_x, where x is number of cycles (SNR = -12 dB ; $DF = 16$)

Tab. 2.4: Obtained P_d for single-cycle detector and multi-cycles detectors within P_{fa} 1 %

Name	P_d
S	14 %
M_2	22 %
M_4	28 %
M_8	39 %
M_{16}	41 %
M_{20}	66 %

In figure 2.11, ROC for each detector can be observed. Furthermore, from each ROC curve a threshold is set to P_{fa} equal to 1 %. Resulted P_d for each detector are

shown in Tab. 2.4. By usage of higher cyclic components, the performance of sensing can be improved. For example, in case of comparison between S and M_{20}, P_d can be improved by 52 % at P_{fa} 1 %.

3 IMPLEMENTATION

The aim of this chapter is to present utilized digital hardware blocks. The design is implemented into Xilinx Virtex 6 FPGA. For purpose of designing is used ISE 14.6 and collection of provided development tools support by Xilinx. A fixed point arithmetic in Q format with first signed bit is used. The targeted FPGA contains DSP slices with multiplier input 25×18. Hence, an arithmetic precision is selected to fit into this DSP slice structure.

The chapter is split into two section. The first section describes theoretical background and hardware design of baseband preprocessing block. The second section is dedicated to implementation of cyclostationary based detector.

3.1 Baseband preprocessing

The detector is dedicated for sensing OFDM channels. A crucial condition is that input signal is at DVB-T original baseband sampling rate. On the other hand, the ADC output provide approximately 25 times higher sampling rate than is required for OFDM system. To provide intersection between the front-end output and the detector input, the OFDM channel has to by processed in order to meet a detector input signal requirements.

One of the usual baseband preprocessing steps is converting particular selected channel to central zero frequency known as selecting. That channel conversion is for simplicity already realized by front-end LO_1 tuning. A disadvantage of the direct signal conversion is that, the front-end contributes a DC offset at its output. However, based on software simulation in previous chapter, A presence of DC offset does not have negative influence on detector functionality.

A basic premise is to change a sampling rate of the ADC out signal to achieve original DVB-T sampling rate f_d. It leads to conversion ADC sampling rate f_a 245.76 MHz to $f_d \frac{64}{7}$ MHz. In terms of conversion rate determination, the f_a and f_d ratio is not integer number.

The baseband preprocessing entity is split into three sections. In the first section, the input signal at f_a is down-converted to a medial sampling rate f_m 15.36 MHz. The f_m is selected based on the lowest frequency which can be achieved by dividing f_a power of two and it is still higher than f_d. Further, in the second section, the decimation stage is followed by a channel filtering stage. This stage realizes a fine filtering of adjacent channels. To obtain the DVB-T channel at the original sampling frequency f_d, the channel is down-sampled with fractional decimation factor. A Fig. 3.1 provides an overview about sampling rate conversion spread into those three sections.

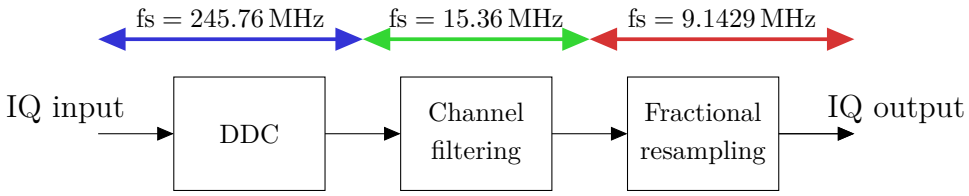


Fig. 3.1: Baseband preprocessing block diagram

3.1.1 Digital down converter and channel filter

A Digital Down Converter (DDC) is a first filtering stage employed in sample preprocessing. The DDC realizes sampling rate down-conversion by $\frac{f_a}{f_m}$. Hence, a decimation factor is chosen as 16. DVB-T channels in Both modes 2k and 8k have frequency bandwidth approximately of 7.612 MHz. Therefore, the decimation filter passband is selected 7.68 MHz to involve whole DVB-T signal bandwidth. Since, the filter's main purpose is to ensure anti-aliasing during down-sampling, a low-pass type is selected. A passband cut-off frequency f_{pc} accords to the signal bandwidth. Its frequency is 3.84 MHz. A stop-band cut-off frequency f_{sc} according to Nyquist rule is selected as half of targeted sampling rate, hence f_{sc} is 7.68 MHz.

The next step of designing digital filters is the passband ripple σ_p and stop band attenuation σ_s selection. The σ_p in terms of OFDM receivers has crucial effect on constellation and channel estimation recovery [37]. Since sub-carriers energy distortion influenced by σ_p. However, in terms of a low-cost filter design, dedicated not for a data decoding, the maximal σ_p is set as 1 dB. The σ_s is selected based on a standardised spectral mask [33]. That mask is relaxed by 30 dB to meet low filter complexity. The σ_s is 80 dB. Filters design methodology is selected to obtain filters with Finite Impulse Response(FIR) known as FIR filters.

The following filtering stage is called as a channel filtering. The channel filter is employed to realize fine filtering. An frequency response follows DVB-T standards suggestions to achieve maximal adjacent channels rejections. The passband cut-off frequency f_{ps} is set according to [33]. As a result, the f_{ps} is set at 3.82 MHz. In a same manner, a stop-band frequency f_{3s} is set at 4.18 MHz as well as the stop-band attenuation $\sigma_3 s$ is set to be equal to 40.2 dB.

Two stages decimation filter and cut-off frequencies planning

Based on the optimization method of decimation and interpolation filters [38], those filters can be split into more stages to reduce their complexity. The complexity is defined as number of multiplication operations (taps) required for a filter realization defined by particular specification as σ_p and σ_s, Θ_s and Θ_p. Θ_s and Θ_p are angular

Tab. 3.1: DDC stage specification

Input sampling frequency	245.76 MHz
Output sampling frequency	15.36 MHz
Decimation factor	16
Passband cut-off frequency	3.84 MHz
Stopband cut-off frequency	7.68 MHz
Passband ripple	1 dB
Stopband attenuation	80 dB

Tab. 3.2: Channel filtering stage specification

Sampling frequency	15.36 MHz
Passband cut-off frequency	3.82 MHz
Stopband cut-off frequency	4.18 MHz
Passband ripple	1 dB
Stopband attenuation	40.8 dB

frequencies of f_{sc} and f_{pc} normalized to sampling frequency F_s. Variables σ_p and σ_s utilized in eq. (3.2), are not in logarithmic scale.

$$\Theta_s = \frac{2\pi f_s c}{F_s} \tag{3.1}$$

$$N = \frac{-20\log_{10}\sqrt{\sigma_p\sigma_s} - 13}{2.32|\Theta_s\Theta_p|} \tag{3.2}$$

A dividing one filtering stage into more stages can be involved into filter design only if their decimation or interpolation factor can by expressed as product of two or more integers. As a result, decimation filter proposed in this section is split into two stages $P(z)$ and $Q(z)$ with common decimation factor of 4. Decimation factors are named M_1 and M_2. Both stages have different sampling frequency F_{1s} and F_{2s} and of course Θ_{1s}, Θ_{2s}, Θ_{1p} and Θ_{2p} are unique for both stages. The next step is proposal of a frequency plan which means setting of optimal cut-off frequencies for both stages.

In consideration at the first stage, the equation (3.2) implies that increasing transition region defined by Θ_{1s} and Θ_{1p} decreasing number of taps N. The f_{pc} is static and cannot be minimized since DVB-T channel specification. On the other hand, Θ_{1s} is set at $\frac{\pi}{M_1}$ to suppress higher frequencies which can be replicated to obtained signal after down-sampling. However, after decimation stage is employed the channel filter $G(z)$ to realize fine filtering, therefore replicates out of DVB-T

channel are suppressed by this filtering stage. Hence, the channel filter stop-band cut-off frequency has to be also involved in frequency planning. Stop-band cut-off frequencies are figure out from last stage which is expressed as

$$\Theta_{xs} = \pi - \frac{2\pi f_{(x-1)s}}{F_{xs}}. \tag{3.3}$$

Variable x selects parameters of current stage set and $(x-1)$ selects parameter of previous stage set. It can be also rewritten as

$$f_{xs} = \frac{F_{xs}}{4} - f_{(x-1)s} \tag{3.4}$$

Hence follows,

$$f_{3s} = 4.18MHz \tag{3.5}$$

$$f_{2s} = \frac{F_{2s}}{4} - f_{3s} = 15.36 - 4.18 = 11.18MHz \tag{3.6}$$

$$f_{1s} = \frac{F_{1s}}{4} - f_{1s} = 61.44 - 26.54 = 50.26MHz \tag{3.7}$$

$$\tag{3.8}$$

Tab. 3.3: Three-stage design specification

	First stage	**Second stage**	**Third stage**
Input sampling frequency	245.76 MHz	61.44 MHz	15.36 MHz
Output sampling frequency	61.44 MHz	15.36 MHz	15.36 MHz
Decimation factor	4	4	1
Passband cut-off frequency	3.84 MHz	3.84 MHz	3.84 MHz
Stopband cut-off frequency	50.26 MHz	11.18 MHz	4.18 MHz
Passband ripple	0.5 dB	0.5 dB	1 dB
Stopband attenuation	78 dB	78 dB	44 dB

Requirements on passband ripples for both decimation filters after splitting have to by divided by 2, hence both stages of decimation filter have to meet pass band ripple lower than 0.5 dB. All three stages are designed based on the Tab. 3.3 of specifications. As methodology is utilized Parks–McClellan algorithm for designing FIR filters. A resulted filter length for each stage is shown in Tab. 3.4. A stop-band attenuation of The channel filter is increased to 45 dB to achieve Spectral mask limits. A frequency response of each filter in cascade and result combination can be observe in Fig. 3.3. In this figure can be observed influence of introduced frequency planning. Filters frequency responses keep wide transition region to reduce number

of taps, however their stop-bands regions exactly overlaps pass-bands of following filters. It can be clearly observed in case of Stage1 response and Stage2 response. The stopband cut-off frequencies crossing occurring at 50.26 MHz.

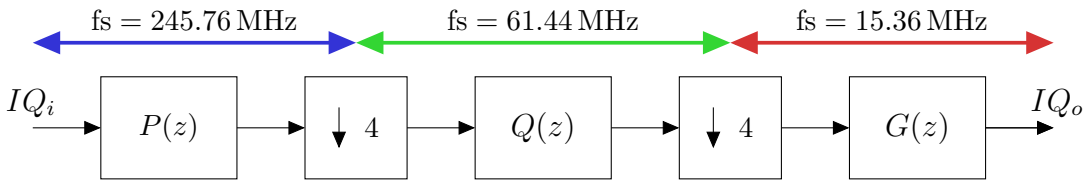


Fig. 3.2: Cascaded 3-stage filter

Tab. 3.4: Cost of implementation of cascaded filter stages

	Stage 1 $P(z)$	Stage 2 $Q(z)$	Stage 3 $G(z)$
Number of tabs	15	24	71

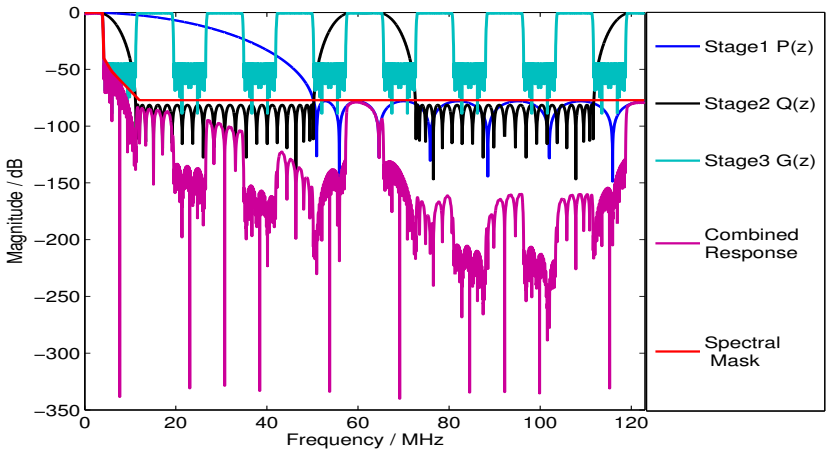


Fig. 3.3: Floating point frequency response of cascaded filter stages

Fixed-point arithmetic and implementation

The signal from ADC input is connected directly to first stage of decimation filter $P(z)$. ADC precision is 14 bits, it defines input data bit width. Virtex 6 DSP slices multipliers have input precision 18×25 bits. For filter design is used the software development interface especially FIR compiler 5.0 which efficiently implement FIR filters structures in targeted FPGA. Designed filters implementation is either based on resource utilization estimated by the compiler. The resource utilization depends

basically on a ratio R between system clock frequency F_{clk} and input data sampling frequency F_s.

$$R = F_{clk}/F_s \tag{3.9}$$

With increasing clock frequency, utilized multipliers are shared between filter sections and even more two filters with equal coefficients sets can share utilized resources as well. A different sampling rate on filter inputs and outputs are in same system clock domain, the difference is emulated by control signal i.e. new data valid.

The FIR compiler offers basically two architectures Systolic Multiply Accumulate (SMA) or Transposed Multiply Accumulate (TMA). The TMA realizes implementations with shorter latency of valid output however its implementation into DSP48E1 structure does not support optimizations of symmetric coefficients sets [16]. Hence, in this term TMA resource utilizations is approximately doubled. Since, decimation filters and channel filter are defined by symmetric coefficients sets, The SMA is selected for implementation of proposed cascaded filter structure.

A settings of basic filters specifications and resource utilization are shown in Tab. 3.5. Different word-lengths between previous stage output and following next stage input is shifted left and truncated whether it is necessary. The compiler can generate filter implementation which shares resources between I and Q branches. However, level of sharing depends on R. In term of R is equal to one, the resource sharing cannot be employed.

Tab. 3.5: Resource utilization and Fixed-point arithmetic precision for implementation of proposed cascaded filters in I and Q branches

	Stage1 $P(z)$	Stage2 $Q(z)$	Stage3 $G(z)$
Input data width [bit]	14	21	25
Coefficient width [bit]	14	18	18
Sample ratio R	1	4	16
Output data width [bit]	21	34	37
DSP48E1 utilization	15	18	14

Frequency responses of all three stages utilizing fixed point arithmetic and final cascaded filter response are depicted in Fig. 3.4. An stop-band attenuation deviation on approximately 108 dB is result of fixed point arithmetic utilization. Since dynamic range DR_{dB} of fixed-point representation with precision 18 bits leads to maximal DR_{dB} of 108 dB.

$$DR_{dB} = 20\log_{10}\frac{2^{18}}{1} = 108dB \tag{3.10}$$

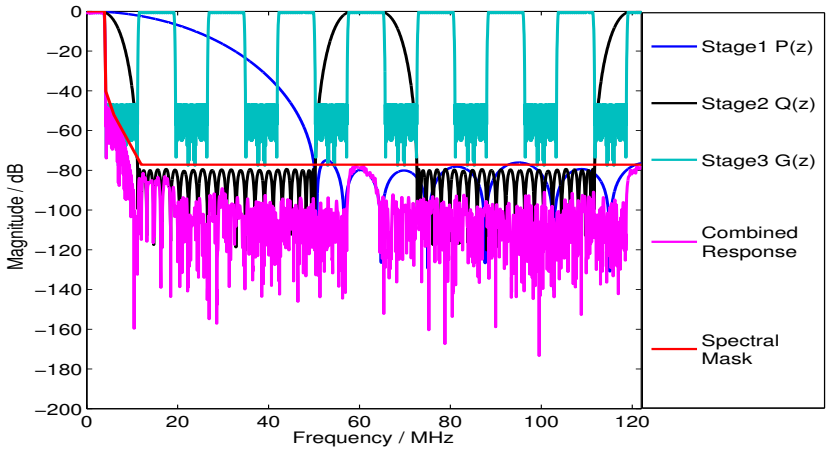


Fig. 3.4: Fixed-point frequency response of cascaded filter stages

The requirements on adjacent channel attenuation is achieved in all frequency range. A detail of resulted filter frequency responses up to 8 MHz, for both arithmetic representations can be observed in Fig. 3.5.

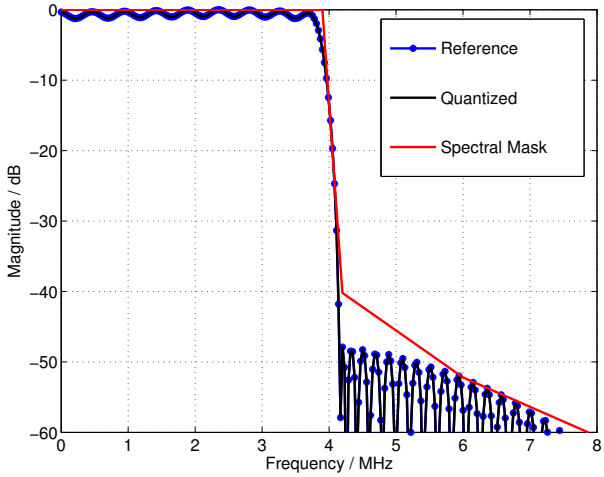


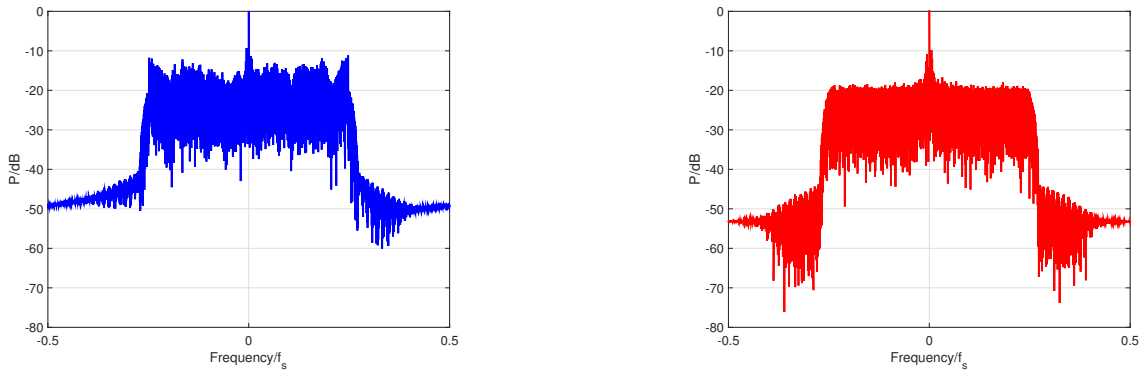
Fig. 3.5: Detail of cascaded filter frequency response in floating point (Reference) and fixed point(Quantized) representation up to 8 MHz

Measurement test

A result of testing designed and implemented 3-stage cascaded filter under real DVB-T channels measurements is depicted in Fig. 3.6b. Under first scenario A, the front-end's LO is tuned to central DVB-T channel frequency at 482 MHz. A measurement time is set to 8.4 ms. Measured PSD is depicted in Fig. 3.6a. A scenario B is defined by same measuring time and the LO is set at an unoccupied channel.

A resulted PSD is depicted in Fig. 3.6b. Both measured PSD are normalized to maximal measured value which is in scenario B at a central frequency. The sampling frequency is 15.36 MHz.

By comparing measured PSD in both scenarios, A DVB-T channel presence in scenario A can be determined based on measured energy.



(a) (b)

Fig. 3.6: Measured: (a)Occupied DVB-T 8k channel at 482 MHz (b)Non-occupied channel

3.2 Fraction re-sampling

A final part of baseband preprocessing is the input signal re-sampling to original DVB-T sampling rate $\frac{64}{7}$ MHz. This sampling rate is used by DVB-T transmitters and in terms of DVB-T cyclostationary detection, reconstruct input signal at this sampling rate is essential [39].

The output signal of previous filter stage is sampled at 15.36 MHz. A fractional ratio between these two sampling frequency domains is equal to 1.68.

A direct method realizing fractional re-sampling is splitting the fraction ratio into dividend and divisor in basic form M/N, hence it leads to an utilization of a two-stage filter which is consist of an up-sampling by M followed by a down-sampling stage with factor N. Aliasing filters employed in both stages can by merged as one low-pass filter. In case of re-sampling by 1.68, Up-sampling by 25 and down-sampling by 42 could by employed ($\frac{42}{25} = 1.68$). The up-sampling of the signal with a sampling rate approximately 9 MHz and up-sampling factor 25 leads to increasing sampling frequency to more than 378 MHz. A theoretically maximal system clock rate of DSP48E1 slices is 500 MHz. Hence, the realization is theoretically achievable.

However, the filter can by decomposed into much more optimal poly-phase structure. Based on Nobel identity, single-rate filter section with impulse response

$h(n)$ can by decomposed into M filters with impulse response $h_t(n); t \in \mathbb{N}_{<M}$ operating on original input signal sampling frequency f_s. Filters outputs are sequentially read out by output commutator at sampling rate $M\dot{f}_s$. To obtain resulted sampling rate M/N, only Nth sample is selected from commutator output. A block digram of poly-phase structure is illustrated in Fig. 3.7 [43].

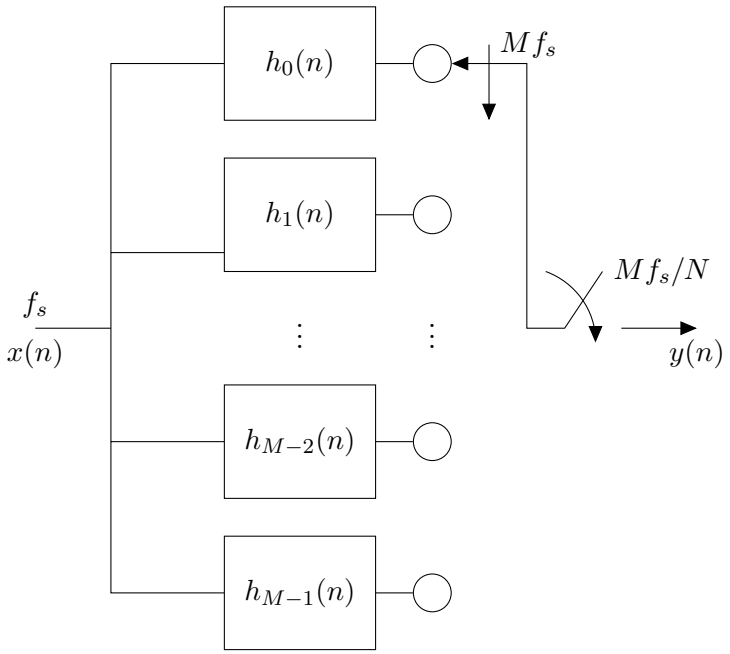


Fig. 3.7: Block diagram M/N re-sampler decomposed into poly-phase structure [43]

In case where ratio M/N is still to much high to by implemented, the filter can be replaced by another filter with ratio e.g. $M/2N; M > N$. As a result, every even output sample which has to by selected by Nth selector is distributed between two commutator samples, ini other words that sample is delayed by $0.5 \cdot f_s$. Further, if the ratio is changed to e.g. $M/3N$ that resulted fractional delay is not constant in this case. However, fractional delayed samples can be estimated by special filter type called FD filters (Fractional Delay filters). FD filters are mostly realized by Farrow filter structure.[43]

3.2.1 Farrow structure

Farrow structure has been introduced in 1988 and it is named by its author Trevor C. Farrow [40]. Mr. Farrow suggested that every filter's impulse response $h(k)$ could be expressed as an Nth-order polynomial $c(k)$. As a result, a sample delayed by delay Δ after $y(n)$ $(y(n - \Delta))$ can be estimated as well. For description Farrow

filter fundamentals, The equation of discrete convolution expressing regular digital filtering is used [41].

$$y(n) = \sum_{k=0}^{N} h(k) \cdot x(n-k) \tag{3.11}$$

Following Farrow's suggestions, eq. (3.11) can be rewritten as

$$y(n-\Delta) = \sum_{k=0}^{N} c_{\Delta}(k) \cdot x(n-k) \tag{3.12}$$

So, Variable $h(k)$ has been substituted by $c(k)$. The polynomial expression $c_{\Delta}(k)$ can be described as [42]

$$c_{\Delta}(k) = \sum_{i=0}^{M} b_i(k) \cdot \Delta^i \tag{3.13}$$

Where $M-1$ is a polynomial order and $b(k,i)$ is set of polynomial coefficients. After exchanging the order of the summations

$$y(n-\Delta) = \sum_{i=0}^{M} \left[\sum_{k=0}^{N} b(k,i) \cdot x(n-k) \right] \Delta^i \tag{3.14}$$

the eq. (3.12) can be finally expression as

$$y(n-\Delta) = \sum_{i=0}^{M} g_i(x(n)) \cdot \Delta^i \tag{3.15}$$

According to eq. (3.15), based on $x(n)$ and known approximation of h, the $y(n-\Delta)$ for any Δ ; $0 < \Delta < 1$ can be determined. As a result, Farrow filter structure can be theoretically used for realization of any fractional re-sampling. This is provided by settings particular fractional delays. Moreover, by application Horner's rule for e.g. 3th order polynomial approximation eq. (3.15) can by described as

$$y(n-\Delta) = g_0 + \Delta[g_1 + \Delta[g_2 + g_3\Delta]] \tag{3.16}$$

Hence, Farrow's topology can be implemented as M FIR filters operating in parallel. As Farrow filters coefficients sets, coefficients of polynomial approximation by e.g. B-spline are used. A filter impulse response approximation accuracy depends on order of the polynomial. To achieve same accuracy with lower polynomial order, a sectional approximation can be applied. The impulse response h is divided into sections and approximated separately. As a result, S approximation polynomials for S sections are obtained. Coefficients set length of FIR filters employed in Farrow structure is defined by S as well. Furthermore, the Δ resolution depends only on a arithmetic precision.

3.2.2 Arbitrary Re-sampling

Farrow structure enables implement prototype of FIR filter, IIR filter and also polynomial types as e.g. Lagrange filter. In [42], Mr. Fred Harris has presented re-sampling methodology based on high-order FIR filter. This method is followed and moreover implemented in FPGA.

As a prototype filter is applied an anti-aliasing (lowpass) FIR filter. The FIR filter is designed using least-squares error minimization algorithm to obtain liner-phase characteristic. Moreover Kaiser window is applied on resulted coefficients set. One of advantages is reduction side-lobe amplitude which leads to obtaining smoother impulse response suitable for polynomial approximation.

An anti-aliasing normalized cut-off frequency is chosen as $\frac{1}{2}\cdot 42^{-1}$. The number 42 is related to maximal rate changing factor. Number of coefficients is set as $2\cdot N\cdot 42+1$, where N is accuracy factor. A prototype filter specification is shown in Tab. 3.6.

Tab. 3.6: The parameters

Type	FIR (Least-squares error minimization)
Input sampling rate	15.36 MHz
Operating sampling Frequency	384 MHz
Number of Coefficients	421
Pass-band cut-off frequency	9.1429 MHz
Kaiser window β factor	10

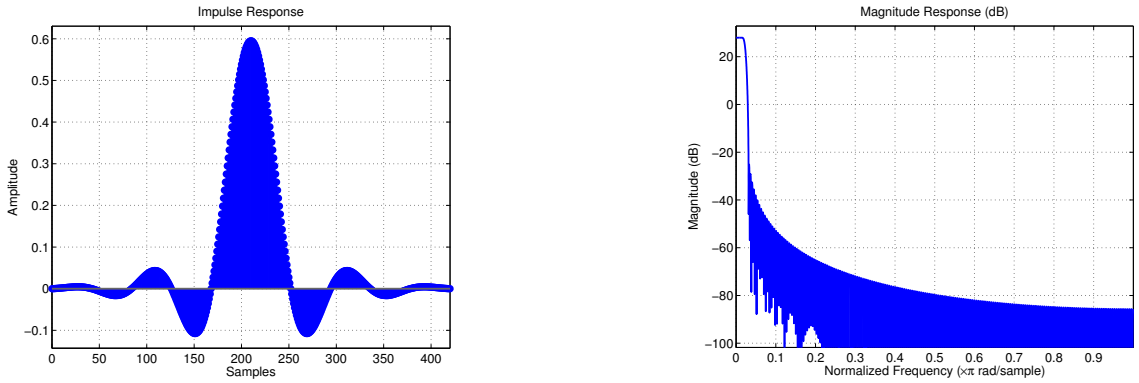


Fig. 3.8: Frequency response and impulse response of the prototype low-pass filter

The next step is approximation of prototype filter impulse response. The impulse response is divided into 10 sections and for each section, Tailor series of 3th order is figured out. As a result, matrix of 4×10 is obtained, where 0th polynomial coefficients are associated with $b(k, 0)$ which is simultaneously coefficient set of last

FIR filter in Farrow chain. In the same order, coefficients set $b(k,1)$, $b(k,2)$ and $b(k,3)$ are obtained as well.

Fractional delay estimation

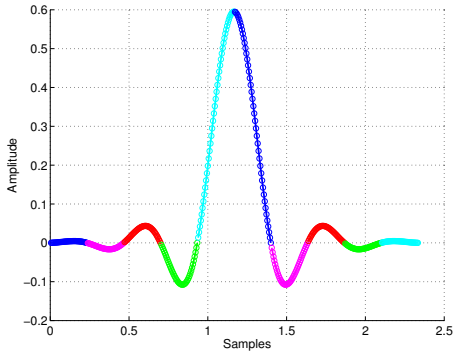
The output samples of Farrow's filters are running at the input sampling frequency 15.36 MHz. To obtain re-sampled output at sampling rate $\frac{64}{7}$ MHz, The delay Δ has to be estimated. It is according to eq. (3.15). However, Δ is applicable only in ratio of two following samples ($0 < \Delta < 1$). Therefore, to obtain samples in ratio M/N, Particular samples are not used in output samples estimation and can be discarded. Hence, output samples are at first down-sampled by integer down-sampler with non-symmetric selection. The sampler is controlled by I_d to obtain 42–to–25 samples. The I_d is assumed as bipolar value (True, False). An integer delay is realized as distance between two occurrences where I_d is equal to True. I_d is actualized every new sample at original input sampling rate. Further, a valid resulted output sample is estimated based on FIR filter outputs which represents $g_i(x)$ and particular Δ. Essentially, A delay between two samples is equal to M/N (1.68). So, valid data come through on multiplies of $1.68 \cdot F_s$. Further, the delay can be split to integer part delay (per samples) and fraction part. The integer part is realized by I_d controlling and the fractional part by Δ. Hence, a sequence of delays between samples:

$\{0, 1.68, 3.36, 5.05, 6.72 \ldots N \cdot 1.68\}$ can be expressed as integer delays (per samples)
$\{0, 1, 3, 5, 6, \ldots floor(N \cdot 1.68)\}$ and fractional delays Δ
$\{0, 0.68, 0.36, 0.05, 0.72, \ldots N \cdot 1.68 - floor(N \cdot 1.68)\}$

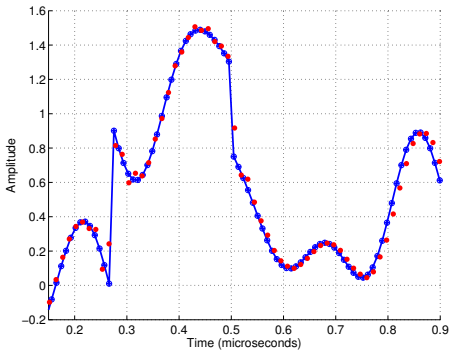
The operation $floor(\bullet)$ returns fraction part of the argument.

By observation time series of Δ and I_d, Both part of delay can be assumed as periodic. The Δ is periodic every 25th sample at output sampling frequency. Three periods of Δ are depicted in Fig. 3.10b. The one period is length of 25 clock cycles at targeted sampling rate. The pattern of both I_d and Δ can be stored in a memory. In Fig. 3.9b is depicted result of initial test. Based on ratio between number of input samples and output samples, The re-sampling ratio 1.68 is proved. A software model of proposed Farrow filter is applied on the signal measured on the output of the 3-stage cascaded filter and processed with different approximation order. The resulted PSD for each scenario is depicted in Fig. A.2. The resulted PSD of processed signal by the prototype filter is also depicted in Fig. A.2. With decreasing approximation order the signal to noise ratio decreasing as well. In performance comparison the prototype filter and approximation order equal to 3. The SNR estimation is approximately 10 dB smaller in case 3rd polynomial approximation. The f_s is equal

to $\frac{64}{7}$ MHz.

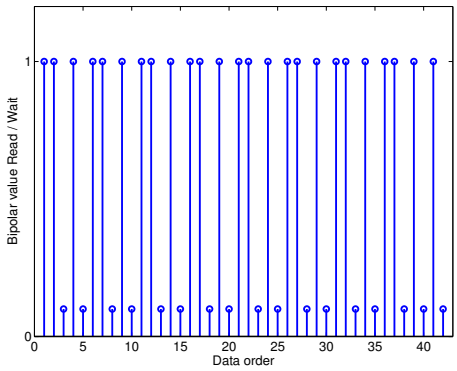


(a)

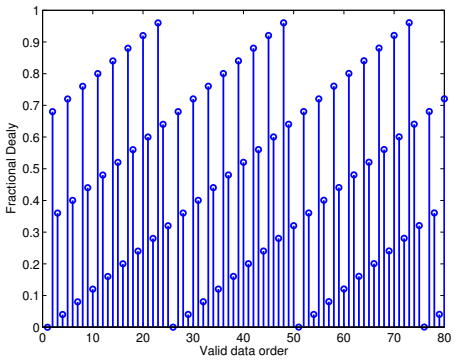


(b)

Fig. 3.9: (a)Prototype filter's impulse response partitioned into 10 sections, (b)Random test signal (Blue) and its 1.68 down-sampled version (Red)



(a)



(b)

Fig. 3.10: (a)Valid data control signal I_d.
(b) The fractional delay Δ

Implementation

Farrow filter structure can by implemented as parallel connection of FIR filters. A number of employed FIR filters depends on selected order of polynomial approximation. In terms of saving FPGA resources only 2th polynomial approximation is involved. It leads to utilization of three independent FIR filters. A number of filters coefficients is related to number of approximation sections. The farrow filter design presented in this section splitting prototype filter's impulse response into 10 sections. Since resulted impulse responses are not symmetric, the transpose architecture of FIR filters is selected. One filter realizations with two paths for I and Q branches

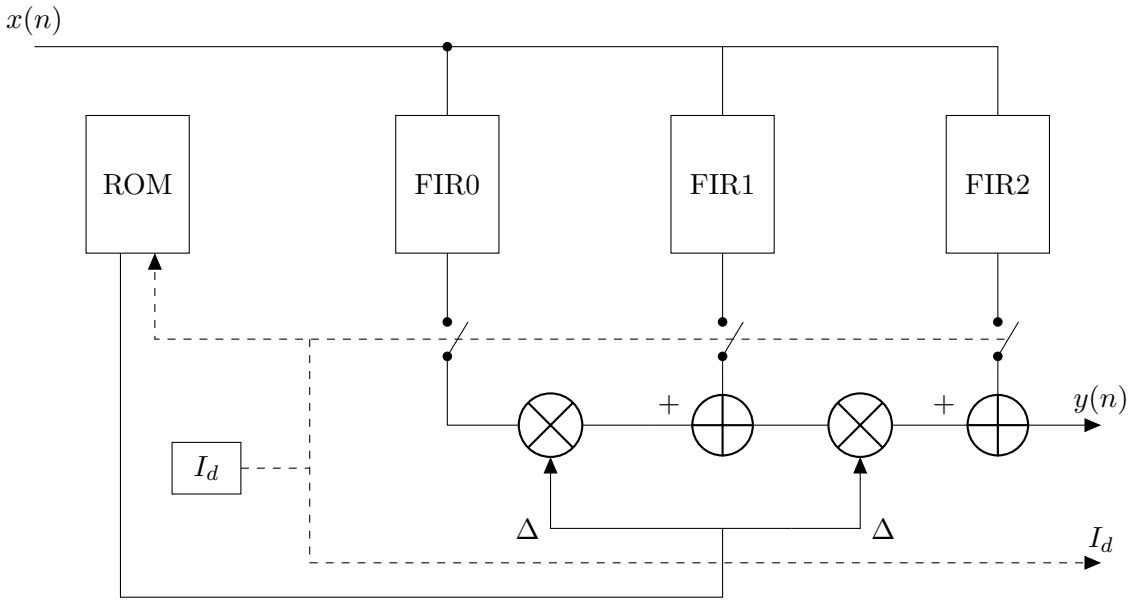


Fig. 3.11: Block diagram of Farrow filter

employed 6 DSP slices, as a result 18 DSP slices are utilized in Farrow re-sampling implementation. A 33 bit-width filter outputs are truncated back to 25 bit-width.

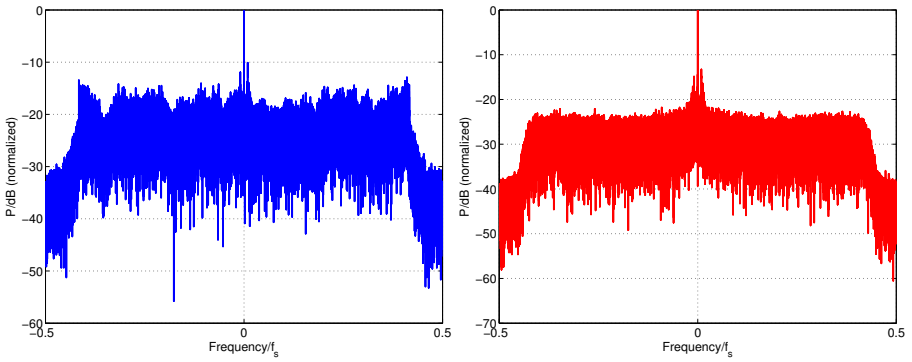
Integer delay I_d control is realized as shift register with a feedback-loop from an output to input. An initial 42 bit-width value is depicted in 3.10a. The value is

$$0b11010110101101011010110101101011010110101101010.$$

In terms of integer down-sampling realization, the control signal I_d as Chip Enable CE of D type register is used. This signal also controls a counter which increments address of a ROM memory. The ROM memory contains one period of Δ. Each Δ is scaled by 2^{14} to fit into 14-bit width value. The memory deep is 25 rows. Output samples from FIR filters are multiplied and accumulated as is described in eq. (3.16) and illustrated in Fig. 3.11 . To enable DSP slices sharing between I and Q branches. The Q branch is delayed by one clock cycle. The fully pipelined architecture of DSP slices are employed. In the implemented architecture are used two DSP slices for both branches, however the system clock is approximately 16 times higher then sampling rate, therefore utilization of DSP slices can be reduced to one DSP slice. It can be obtained by higher level of inputs and feedback loop multiplexing. The one clock cycle Q branch delay is not corrected back. The delay is further used in next sections of detector architecture.

Measurement test

Measurement scenarios specification accords to scenarios specification introduced in section 3.1.1. Measured signals are gained in different time. Resulted PSD are depicted in Fig. 3.12. In comparison the PSD of measured signal gained on the 3-stage filter output and the PSD of measured signal gained on the re-sampling stage output, an estimation of SNR degradation is 10 dB. This result corresponds to software model simulation. To improve proposed Farrow filter structure accuracy, an implementation of the farrow filter employing higher approximation order is required.



(a) (b)

Fig. 3.12: Measured: (a)Occupied DVB-T 8k channel at 482 MHz (b)Non-occupied channel

3.2.3 Power of two clock domain crossing

The whole block of baseband preprocessing is situated in ADC clock domain of 245.76 MHz. To relax timing constrains of detector implementation, the output signal is re-clocked to a domain of 122.88 MHz. The clock of 122.88 MHz is 13.44 higher than sampling frequency of processed signal. It still provide possibility of resource sharing by multiplexing. Both clock domains are provided by dedicated clock management block which ensures same phase of both clocks. As a result, both clock domain are fully synchronized. The clock crossing of data buses does not require involving any logic. However, a pulse-width of control signals representing valid data at the output ND are doubled.

3.3 Cyclostationary based detector implementation in FPGA

The concept of Cyclostationary detection was introduced in previous chapter. In terms of detector implementation in FPGA, basic suggestions are given in [24] and [25]. A design parameters are set to meet constrains of sensing DVB-T 8k broadcasting [46].

Following suggestions, the basic block digram of the detector is depicted in Fig. 3.13. Throughout this section, a description of each functional block is presented. The description is started at the baseband preprocessing output to the detector and proceeds step by step to final hypothesis test determination. The detector is consistent of a time domain and frequency domain processing section followed by a section dedicated for the test metric estimation.

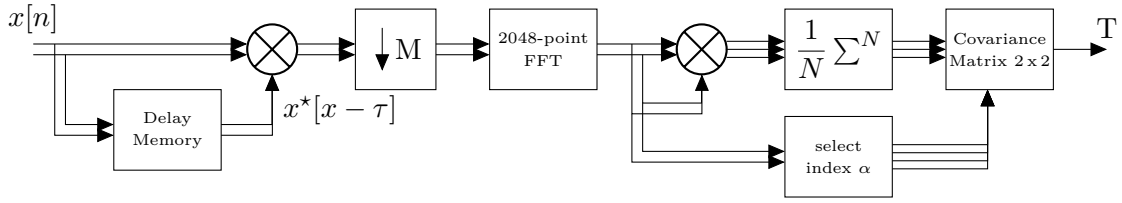


Fig. 3.13: Block diagram of cyclostationary detector [25]

3.3.1 Processing in Time domain

Delay memory block

The delay memory block is realizes exactly one DVB-T 8k symbol length delay. The symbols are consist of 8192 samples. Those samples have to by stored in memory and read out again after 8192 clock cycles. Hence, each memory row is read first and rewritten next system clock cycle. A read/write operation is controlled by an ND signal.

Since, the delay memory block is followed by a complex multiplier with input 25×18, The narrower input is fed by branch which contains the memory block. So, requirements on a memory size is to store 8192×18 bits. For realization of memory block is employed hard macro defined BRAM32–32kb. Four blocks are utilized for each I and Q branch.

Complex multiplier

The equation for complex multiplication $x = a + bi$ and $y = c + di$ is described as

$$x \cdot y = (a + bi) \cdot (c + di) \tag{3.17}$$

$$x \cdot y = ac + ibc + iad - bd \tag{3.18}$$

$$x \cdot y = (ac - bd) + i(ad + bc) \tag{3.19}$$

From resulted equation can be observed that for realization complex multiplication can be used one DSP slice for each branch. The DSP slice has to be set to execute multiply and accumulate/subtract operation. Since time domain processing running on approximately 13 times higher rate, by input/output multiplexing of the DSP slice is possible to reduce resource usage to one DSP slice. In the detector design is used direct DSP slice utilization which utilize one DSP slice for one operation. The optimization is left to future redesign.

Decimation

A targeted decimation factor is set to 32. For its realization is used Cascade Integrator-comb (CIC) filter. The CIC filter is characteristic for its multiplier-less structure. However, its disadvantage is slow decay frequency response starting on the zero frequency. This could be observed in Fig. 3.14. The stop cut-off frequency is at 142.9 kHz ($\frac{F_s}{2 \cdot 32}$). Cyclic frequencies α are expected in terms of 8k mode for $CP = \frac{1}{4}$ at a frequency which can be determined by eq. (2.4.3). These parameters is chosen based on deployed DVB-T channels specification [46]. The frequency α is at

$$\alpha = \frac{F_s}{8192 + 8192 \cdot \frac{1}{4}} = \frac{\frac{64}{7} \cdot 10^6}{10240} = 892\,Hz \tag{3.20}$$

As a result, expected α is at normalized frequency to CIC output sampling rate 0.0031 ($\frac{0.892}{285.7}$). Therefore influence of the slow decay can be neglected. Therefore no correction stage is required. In terms of increasing DF, the correction stage design can follow solution presented in [45]. The CIC filter is designed by the Xilinx development tool as 5-stage CIC filter dedicated for decimation with a differential delay equal to 1.

FIFO memory as a last block of the time domain processing

Related to [24] and [25], the decimation stage is followed by an FFT stage. The samples stream at decimation output is sampled at 285.8 kHz. So, a buffer employed before Fourier transform is required. Moreover, after all required samples are buffered,

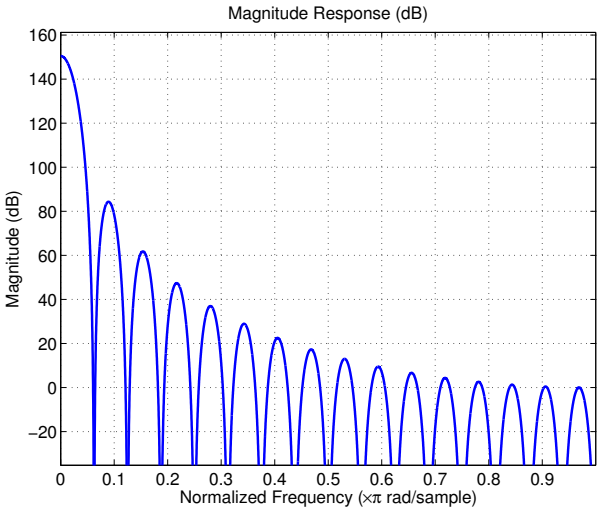


Fig. 3.14: Frequency response of CIC filter

the remain processing time depends fundamentally only on number of required clock cycles and a clock frequency. To achieve desired short sensing time, further processing in frequency domain is placed into the faster clock domain. For this purpose, The FIFO memory which realizes sample buffering is moreover designed as two port FIFO with independent clock port controlling to provide interface between to clock domains. The second faster clock domain is at frequency 245.76 MHz.

3.3.2 Frequency domain processing and test metric estimation

Fast Fourier transform

To obtain the cyclic spectrum, detector's circuit has to involves a block of Fast Fourier Transform (FFT). The FPGA provider Xilinx provide several versions of architecture. Those are Streaming architecture, Radix4, Radix2 and Radix2Lite. The architecture should be selected based on an application. The detector acquiring signal data in scale of milliseconds (precise times in section 2.4.3) and after that figures out Fourier transform and based on result estimates the test metric. So streaming architecture can be refused at first. Based on Xilinx's estimation of resource versus throughput for all tree architecture options, the Radix2 architecture is selected. It is trade off between these two parameters. However, the architecture can be replaced by another architecture with no changes in the rest of the detector design.

The FFT width is selected to 2048 coefficients for input data width 22 bits. The FFT output is shifted and truncated into 18 bit width bus. After Fourier transform is finished. The resulted spectrum estimation is sent to test metric estimation

block as a stream of data with length 2048.

Fourier transformation require 15575 clock cycles, as a result the FFT block clocked by 122.88 MHz require 126 µs. On the other hand, by doubling FFT system clock to 245.76 MHz, the required computing time is two times shorter therefore 63.3 µs

Variance and covariance estimation

The test metric estimation is based on covariance matrix. Inputs for a test matrix estimation block are a variance of all Fourier transform components k $E(X^2(k))$ and $E(Y^2(k))$. Variances are estimated from imaginary Y and real X part of spectral coefficients separately. A last required input for test metric estimation is their covariance $E(X(k) \cdot Y(k))$. The estimation is described in section 2.4.1.

The variance and covariance estimation can by also expressed as a Multiply-accumulate operation (MAC). This operation is fully suitable for implementation in DSP slice.

Xilinx provides a Device Macro Instantiation (DMI) for hard defined macros as Block-RAM or DSP slice (DSP48). The purpouse of DMI is to provide possibility to instantiation these blocks within several options of functionality. Options are set by generic variables. The DMI is open source therefore it can be edited to achieve any option which is supported by macro block. The DMI certainly contains a hard macro instantiation in fundamental form which according to entity of really implemented hardware block. A DMI for MAC realization is named MACC_MACRO. Using MACC_MACRO, the variance and covariance can by implemented by three DSP slices.

In the proposed detector design the variance and covariance estimation are implemented by DSP slices dedicated for single operation, therefore DSP slices utilization is equal to six. The 18 bit-width FFT output data is connected to multipliers which realize squaring of the real or imaginary part and multiplication between them. The DSP slices outputs are connected to following DSP blocks realizing summation. The result of summation is stored in register implemented in DSP block as output register. For realization of accumulation, a feed-back loop from the DSP slice output to the second DSP48 input is employed. The DSP slice output register is reset on new sensing relation start. The block is controlled by control signal new data valid provided by FFT block.

Cyclic frequency selection

The aim of this block is storing FFT components$R_x(\alpha_1), R_x(\alpha_2), R_x(\alpha_3)$ and $R_x(\alpha_4)$ at cyclic frequency α_1 and its multiplies α_2, α_3 and α_4 to output registers. For the test

metric estimation are used for cyclic frequencies. On a start of data streaming by FFT block, a counter is enabled. An order of cyclic frequencies occurrence in FFT stream has to be known and stored in register. For four cyclic frequencies selection, four comparators are used. Each comparator compares different cyclic frequency order and counter register. In case of match, associated output register is written by actual value on FFT block output. Both real and imaginary part are treated equally.

This block has four parallel outputs which are changed only two times per sensing relation. Therefore in terms of optimization or involving more cyclic frequencies into test metric, parallel outputs can by replaced by FIFO memory. This optimization step is also advantage for following test metric core which will be described in next section. An adding of FIFO memory has also influence on number of comparators which can be reduced to one. Since cyclic frequency order in FFT data stream is sequential, the sequence can be stored in ROM and a next order is read out on each comparator match. The FIFO memory is read by test metric core logic. As a result, the number of involved α_n has influence only on FIFO and ROM size.

Test metric estimation

The test metric estimation is described in section 2.4.1. The eq. (2.17) can by rewritten as [25]

$$T_t(\alpha) = \frac{X^2(\alpha)\hat{E}[Y^2(k)] + [Y^2(\alpha)\hat{E}[X^2(k)] - 2X(\alpha)Y(\alpha)\hat{E}[X(k)Y(k)]}{\hat{E}[X^2(k)]\hat{E}[Y^2(k)] - \left(\hat{E}[X(k)Y(k)]\right)^2} \tag{3.21}$$

The eq. (3.21) is suitable for that case when only one cyclic frequency α is involved. That case is called as a single-rate detection. In case of involving more cyclic frequencies, the test metric is based on multi-cycle detection 2.4.1. The multi-cycle detection involves result of single-rate detection and summarize them as is expressed in eq. (3.22).

$$T_T = \frac{T_t(\alpha_1) + T_t(\alpha_2) + T_t(\alpha_3) + T_t(\alpha_4)}{4} \tag{3.22}$$

The next step is substitution eq. (3.21) into eq. ttmetric. Since a denominator $\hat{E}[X^2(k)]\hat{E}[Y^2(k)] - \left(\hat{E}[X(k)Y(k)]\right)^2$ is constant for all selected cyclic frequencies. Therefore, the T_T can be described as

$$T_T = \frac{A(\alpha 1) + A(\alpha 2) + A(\alpha 3) + A(\alpha 3)}{4 \cdot B} = \frac{A}{4 \cdot B} \tag{3.23}$$

where, an operator A accords to the numerator in eq. (3.21), The denominator is expressed as B. The final test metric T_T is implementable in this format. The estimation of T_T according to (3.23) contains 40 multiplying operations, 6 add/sub operations and one division. The T_T computing is fitted into an ALU unit consist of Multipliers M1, M2 and Accumulator/Subtracter. The division problem is solved in a next section. The ALU employs 6 DSP slices. Multiplier M2 is consistent of four DSP slices realizing 34×34 multiplier. Left two DSP slices are employed for realization M1 and ACC/SUB.

The ALU is depicted in Fig. 3.15. Pipe-lining registers are not included. Used arithmetic precisions are illustrated in the figure as well(Blue notes). The precision is expressed in signed Q format. e.g. a number 18 according to Q(1,17).

At the beginning the numerator A is computed. The M1 realizes squaring and multiplication of X and Y for each α. A switching between XX,YY and XY are controlled by I_{11}. During computing A I_3 is not active and I_{11} and I_2 are equal. The M2 multiplies result of M1's multiplication with elements of the covariance matrix. The multiplication by 2 is not depicted. The control signal *sign* in terms of A computing sets the operation mode between ACC/SUB. The results for each *alpha* are scaled and accumulated (subtracted) in Register D. The switching between all α is controlled by I_0. After computation of A is finished, the result is sent to output

by setting of I_4. For computation of B, the multiplier M1 is not used and $sign$ is set statically in the subtract mode. Controls signals I_2 and I_3 Select covariance matrix elements as is expressed in eq. (3.21)

The estimation of A requires only $4 \times 3 + 5$ clock cycles which is 17 clock cycles in total. The estimations of number of cycle is based on number of required ACC/SUB operation plus 5 clock cycles for pipe-lining In terms of computing B, the number of cycles is $2 + 5$ which is 7. However, by fully pipelined structure the total number of clock cycles required is 22. The test metric core is clocked by clock signal of 245.76 MHz. Therefore the added time to sensing time is 895 ns.

The controls signal are generated by the state machine. The machine states are saved in ROM memory. A next machine state is controlled only by program counter which increment address of the ROM.

Based on simulations in section 2.4.6, the involving higher number of cyclic frequencies leads to higher P_d within constant P_{fa}. Moreover, a cost of multi-cycle detection extending under presented guidelines for further implementation is neglecting. The input of cyclic frequencies are fundamentally treated as stream. Therefore storing coefficients of Fourier transform in FIFO memory could improve performance with the negligibly cost.

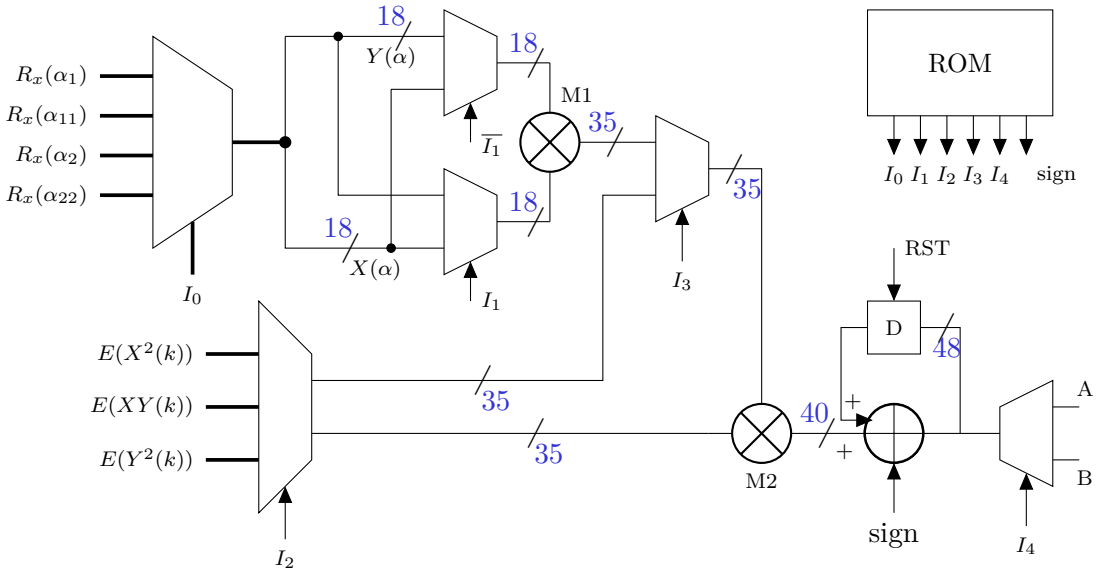


Fig. 3.15: Test metric estimation core

3.3.3 Hypothesis selection

A hypothesis determination is based on comparing estimated test metric T_T and a threshold T_{thr}. For hypothesis H_1 can by applied

$$T_T > T_{thr} \tag{3.24}$$

By substitution of eq. (3.23)

$$\frac{A}{4 \cdot B} > T_{thr} \tag{3.25}$$

is obtained. By replacing division by multiplication,

$$4 \cdot T_{thr} B > A \tag{3.26}$$

The hypothesis determination is without division which reduce complexity.

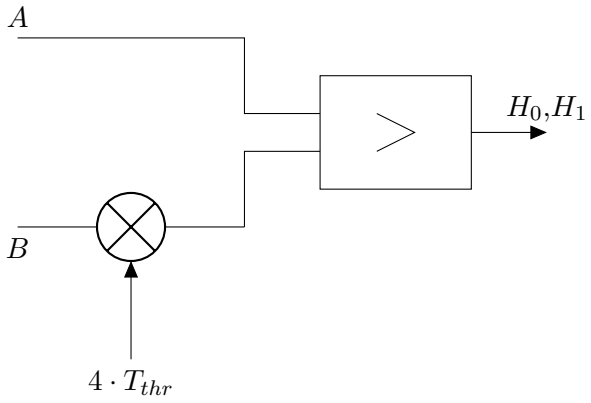


Fig. 3.16: Block diagram of Hypothesis selection

3.4 Arithmetic precision optimization

One of goals of this section is the low complexity implementation into the DSP slice structure. To keep effective utilization of bit-width representing fixed-precision arithmetic, the utilization throughout whole design is tracked and optimized by binary shifting to left with coefficient B. The left LSB bits are truncated.

Tracking and optimization are done under real DVB-T signals measured on the platform. Since software models of used blocks supported by Xilinx (FIR and CIC) are not available, the tracking is done directly under behavioural model of designed detector and further under its implementation. For purpose of tracking, all basic blocks inputs before binary shifting are checked by an overflow checker.

The overflow checker compares the particular number of MSB bits based on $B+1$. If they are not all equal, overflow occurs. The output from each checker is stored in a register with an OR feedback loop. If the register is set to logic one after one measurement, the shifting is assumed as overflow causing and the B is decreased.

The B for each fundamental block input is set based on measurements. One MSB bit is left as undertrunking. The scenario parameters and an input signal are in detail introduced in the section 3.5.2. For proper B settings more measurements and observations are required. The B is selected in order how fundamentals blocks are connected i.e. the B between $P(z)$ and $Q(z)$ are selected at first. A resulted binary shifting coefficients and the shifting position are shown in Tab. 3.7.

Tab. 3.7: Based on measurements, figured out shifting factor B throughout all detector design blocks

Source block	Destination block	B
$P(z)$	$Q(z)$	3
$Q(z)$	$G(z)$	3
$G(z)$	Farrow filter	2
Complex. Multiplier	Decimation filter	2
FFT stage	Pre-test metric estimation blocks	5
Variance and covariance est.	Test metric core	4
M1	M2	1
M2	Accumulator/Subtracter	14
Accumulator/Subtracter	A and B	9

3.5 Detector design evaluation

In this section are presented outcomes related to the detector design introduced in previous section. At beginning, a software model of the designed detector is introduced. Furthermore, the detector performance is tested under the real signal provided by potential primary users.

3.5.1 Software model

For evaluation of functionality and performance of the detector, its software model is designed in mathematical environment MATLAB. As an input signal is used DVB-T signal introduced in section 2.3.1. The input signal is quantized to ADC

resolution 14-bits. DVB-T parameters is chosen according to the most used configuration by DVB-T providers [46]. Those are 8k mode with cyclic prefix length of $\frac{1}{4}$. The DVB-T transmitter operating under SNR -14 dB. The settings of detector parameters follow parameters introduced in previous section. In general, the decimation factor is equal to 32, the FFT length is equal to 2048. Hence, data acquisition time is 8.1 ms. Detector estimates the test metric based on multi-cycle detection. Four cyclic frequencies are used. The simulation scenario is defined for two detectors differs in utilized arithmetic precision. Those are floating-point precision and fixed-point precision. The fixed-point precision differs throughout whole design and exact selected resolution is described in previous sections. The binary shifting is involved as well. Values are optimally scaled with proposed bit-width decreased by 1 since undertrunking. The receiver operational characteristic is depicted in Fig. 3.17 Based on ROC curves for both detector, the deviation of detector performance utilized fixed-point arithmetic can be observed.

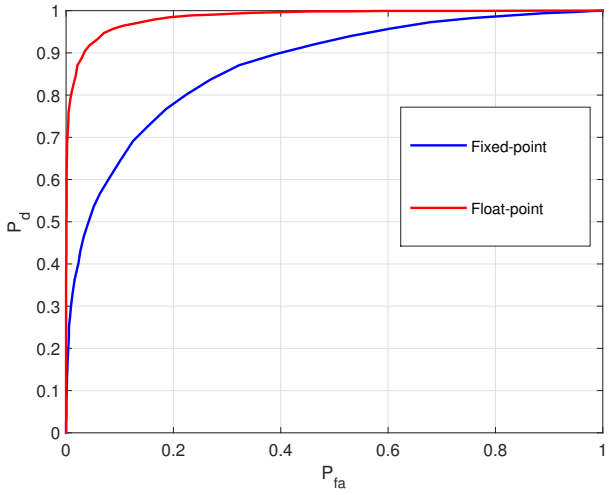


Fig. 3.17: ROC of detectors utilizing floating point and fixed point arithmetic SNR = -14.7 dB

3.5.2 Measurements

A performance of detector implemented in the sensing platform was tested under real measured signals. A DVB-T channel for sensing was selected according to [46]. A partition of table in [46] which contains essential information about the channel is attached in A.3. A selected DVB-T channel's central frequency is at 482 MHz, mode = 8k CP = $\frac{1}{4}$. The sensing time is 8.164 ms (Tab. 2.3 and section 3.3.2) . The spectrum of sensed DVB-T channels is depicted in Fig.3.18.

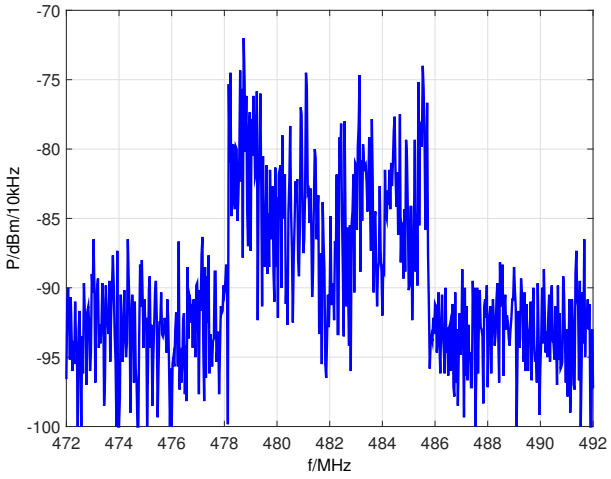


Fig. 3.18: Power spectral density of selected DVB-T channel at 482 MHz measured by Spectral analyzer at 10kHz resolution bandwidth

A proof of valid sensing DVB-T or QFDM signals is extraction of strength components at cyclic frequencies. The cyclic spectrum is depicted in Fig. 3.19. The lowest cyclic frequency is at 892.85 Hz. This cyclic frequency is marked by red arrow.

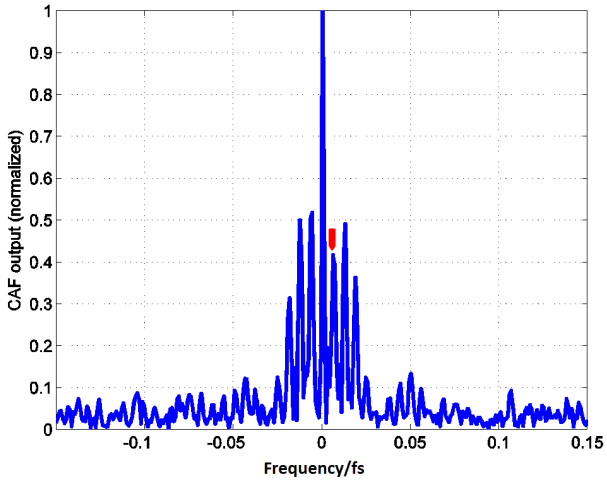


Fig. 3.19: Cyclic spectrum of received DVB-T signal - The lowest cyclic frequency is marked by a red arrow. (fs = 285 kHz)

Hypothesis test

In a scenario for hypothesis H_1. The DVB-T channel as in previous measurement is selected. A number of measurements per one observation is 4096. In a scenario for hypothesis H_0, the receiver was tuned to an unused channel. A resulting PDF

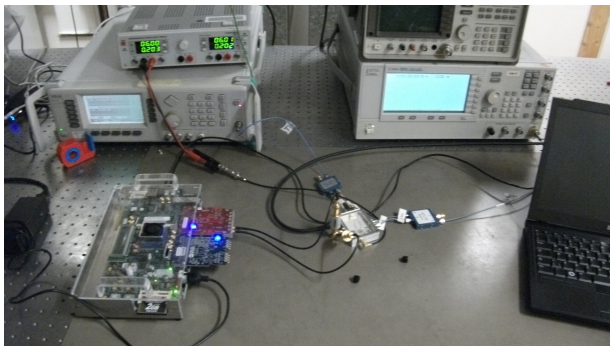


Fig. 3.20: Picture of the measurements set up. The front end is situated in the middle of the picture. The FPGA board is on the right side. To front end are connected two sine-wave generators used as local oscillators. Connected antenna is not depicted.

for both hypothesis is depicted in Fig. 3.21. From the PDF for H0, a typical probability distribution of χ^2_2 can be observed. By Neyman-Pearson test [25]

$$T_{thr} = F^{-1}_{H0}(1 - P_{fa}) \tag{3.27}$$

for P_{fa} equal to 1 %, the T_{thr} has been estimated from cumulative distribution function F_{H0}. As a result, the T_{thr} achieved P_d equal to 97.7 %. The detector's SNR robustness has not been evaluated, since SNR of received signals are unknown.

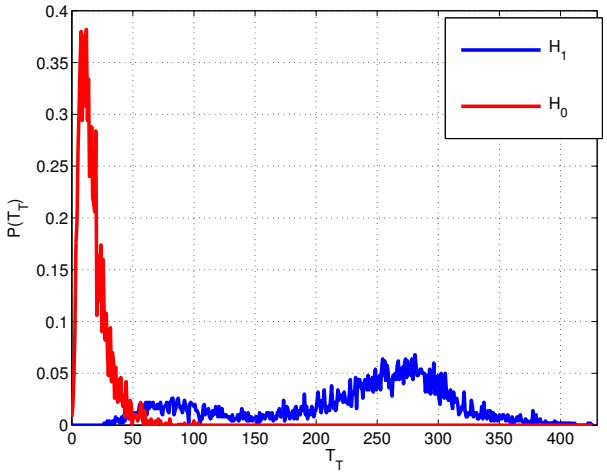


Fig. 3.21: PDF of the test metric T_T of an occupied (H_1) and non-occupied (H_0) DVB-T channel

CONCLUSION

In this thesis, a cyclostationary based detector dedicated for sensing of digital television broadcast channels has been implemented in FPGA and evaluated under real RF environment. A proposed software models of DVB-T signals have been employed in simulations of sensing primary users by selected cyclostationary based method. Moreover, strong and weak points have been summarized and taken into account in detector implementation. The detector has been implemented into a very wide band sensing platform which has been introduced. A preprocessing block required for successful OFDM detection has been proposed and implemented. The preprocessing block consist of a multi-rate filter based on Farrow structure, which is suitable for realization of a fraction re-sampling.

A fully implemented test metric estimation has been proposed and implemented. The detector functionality has been tested under DVB-T 8k channels. Cyclic features has been successfully extracted. Based on Neumann-Pearson test a threshold for further sensing has been determined.

The proposed hardware design of cyclostationary based detector is suitable as basic block for further development of cyclostationary based detectors.

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LIST OF SYMBOLS, PHYSICAL CONSTANTS AND ABBREVIATIONS

DSP	Digital Signal Processing
BP	Bandpass
BB	BaseBand
DSP48	DSP slice DSP48E1
MAC	Multiply-Accumulate operation
DDC	Digital Down Converter
OFDM	Orthogonal Frequency Multiple Access
CR	Cognitive Radio
4G	Fourth generation network
PU	Primary User
SU	Secondary User
IoT	Internet of Things
M2M	Machine to Machine
CR	Cognitive Radio
RFIC	Radio Frequency Integrated Circuit
FFT	Fast Fourier Transform
IFFT	Inverse Fast Fourier Transform
IEEE	Institute of Electrical and Electronics Engineers
WRAN	wireless regional area network
SDR	Software defined radio
RF	Radio Frequency
AD	Analog to Digital
ADC	AD Converter

SDR	Software Defined Radio
SR	Software Radio
LNA	Low Noise Amplifier
DCR	Direct Down-Conversion
LO	Local Oscillator
DAC	Digital to Analogue Converter
MSPS	Mega Sample Per Second
OSI	Open System Interconnection
GPU	Graphics processing unit
ASIC	Application Specific Integrated Circuit
FPGA	Field-Programmable Gate Array
SNR	Signal to Noise Ratio
LUT	Look-Up Table
CLB	Configuration Logic Blocks
FF	Flip-Flop
RAM	Random Memory Access
PLL	Phase Locked Loop
IP	Intellectual Property
FIR	Finite Impulse Response
CIC	Cascade Integrator-Comb
ALU	Arithmetic Logic Unit
DSA	Dynamic Spectrum Access
ROC	Receiver Operating Characteristic
DVB-T	Digital Video Broadcasting – Terrestrial
WiMAX	Worldwide Interoperability for Microwave Access

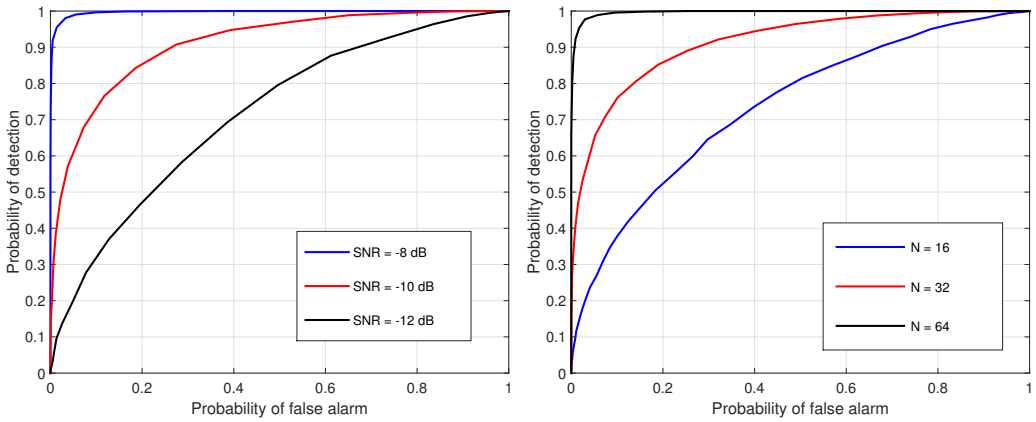
LTE	Long-Term Evolution
WRAN	Wireless Regional Area Network
CAF	Cyclic Autocorrelation Function
RX	Receiver
TX	Transmitter
CP	Cyclic Prefix
BPSK	Binary-Phase Shift Keying
QPSK	Quadrature-Phase Shift Keying
DF	Decimation Factor
UWB	Ultra Wide-Band
SCF	Spectral Correlation Function
FM	Frequency Modulation
ISI	Inter-Symbol Interference
PDF	Probability Density Function
AVG	Averaging
TR	Transformer
GSM	Global System for Mobile (communications)
UMTS	Universal Mobile Telecommunications System
IQ	Real and Quadrature
BiCMOS	Bipolar CMOS
PCB	Printed Circuit Board
FCM	IDK
WLAN	Wireless Local Area Network
ISE	Integrated Synthesis Environment
IIR	Infinite Impulse Response

CIC	Cascade Integrator-Comb
PPF	Poly-phase filter
UF	Up-sampling factor
RC	Raised Cosine
AWGN	Additive white Gaussian noise
CLAPACK	Linear Algebra PACK in C
PSD	Powe Spectral Density
DDC	Digital Down Converter
SMA	Systolic Multiply Accumulate
TMA	Transposed Multiply Accumulate
FD	Fractional Delay
ROM	Read Only Memory
CE	Clock Enable
SW	Soft-ware
EuMC	European Microwave Conference
CMOS	Complementary Metal Oxide Semiconductor
ND	New Data
CS	Chip Slect

LIST OF APPENDICES

A APPENDIX

A.1 Eigenvalue based detection



(a) M_1 - DVB-T $N = 64$, $RF = 8$ (b) M_2 - DVB-T $RF = 8$, SNR =-8 dB

Fig. A.1: Receiver operational characteristics for Eigenvalue based detection simulation scenario

A.2 OFDM Detection

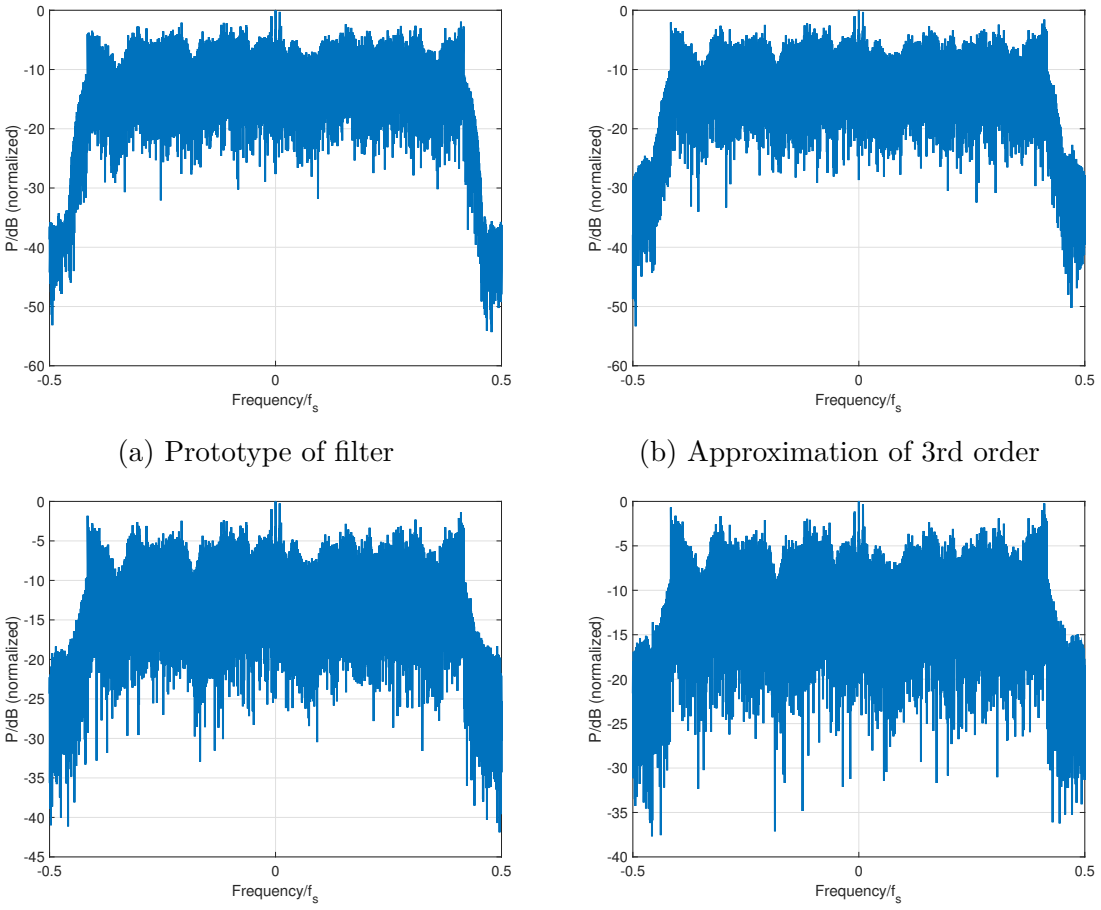
Tab. A.1: Simulation environment for OFDM sensing detector

OFDM parameters	
Number of carriers	2048
Modulation	QPSK
Used Cyclic prefixes	$\frac{1}{16}$
ISI filter	none
Channel type	AWGN
Signal to Noise ratio	-11 dB
Detector parameters	
Sampling frequency	$\frac{64}{7}$ MHz
Number of FFT coefficients	2048
Decimation Factors	32
Used Averaging	none
Rate type detection	Single rate detection
Lag parameter	known
Cyclic frequency	known
Number of observations	6000

Tab. A.2: List of first ten α coefficients for either positive and negative frequencies for DVB-T 2k, CP=$\frac{1}{6}$, $N_{fft} = 2048$

19	37	55	73	91	109	128	146	164	182
1868	1886	1904	1923	1941	1959	1977	1995	2013	2031

A.3 Farrow filter



(a) Prototype of filter

(b) Approximation of 3rd order

(c) Approximation of 2nd order

(d) Approximation of 1st order

Fig. A.2: Influence of selected approximation order on SNR

A.4 FPGA Implementation

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	4813	301440	1%
Number of Slice LUTs	3112	150720	2%
Number of fully used LUT-FF pairs	2545	5380	47%
Number of bonded IOBs	205	600	34%
Number of Block RAM/FIFO	15	416	3%
Number of BUFG/BUFGCTRLs	2	32	6%
Number of DSP48E1s	47	768	6%

Fig. A.3: Table of Virtex 6 resource utilization

A.5 Measurements

Bundesland Baden-Württemberg								
Station	Channel	Fc [MHz]	Modulation	FEC	FFT	Interval	Program	ERP
Ulm	22	482	16 QAM	2/3	8k	1/4	ZDF, 3sat, KiKa/ZDFneo, ZDFinfo	50 kW
Ulm	40	626	16 QAM	2/3	8k	1/4	SWR-BW, Bayerisches Fernsehn, BR (Süd), hr, WDR (Köln)	50 kW
Ulm	43	650	16 QAM	2/3	8k	1/4	Das Erste, arte, Phoenix, EinsPlus	50 kW

Tab. A.3: DVB-T channel utilization in Ulm [46]

B PUBLICATIONS

MAŇAS, Ondřej, ELSOKARY, Ahmed, VALENTA, Václav and MARŠÁLEK, Roman. Implementation of Cyclostationary Based Detection. In: *Sborník přispěvku studentské konference Kohutka 2015*. Brno: VUT v Brně, 2015, s. 44-47. ISBN 978-80-214-5239-8.