THE ANALYSIS OF CERAMIC RESISTOR ARRAYS IN SMT

Václav Novotný, Radek Vala

Doctoral Degree Programme (3), FEEC BUT

E-mail: novotny.vaclav@azd.cz, radek.vala@sanmina.com

Supervised by: Josef Šandera

E-mail: sandera@feec.vutbr.cz

Abstract: This paper is focused on the area of current electrical manufactory in conjunction with possibilities of computer analysis and monitoring psychical phenomena by computing systems. There are also described processes of preparation and manufactory of testing boards for evaluation of reliability of solder joints on specific microelectronic part which has its place in contemporary electronic production and subsequent analysis of physical processes on these boards under condition of thermal cycling in thermal chamber and their influences on overall reliability of the entire component. For purposes of analysis were chosen SMD resistor arrays in configuration 8x0603 which were soldered on typical substrate FR-4 by SAC305 solder. These soldered resistor arrays are also modeled in Solidworks and analyzed by ANSYS. The results achieved by experimental measurement are complemented by simulations of models.

Keywords: Resistor, Arrays, Solder, Joint, Reliability, SAC305, ANSYS, Cycling

1. INTRODUCTION

The Reliability of soldered joints is one of the areas of microelectronic manufactory and its importance and significance is gradually increasing because processes become more complex and it brings groups of new demands on fast, accurate and correct definition of each parameter of production process. The fact of increasing of complexity of technological process is given especially by very rapid development in the area of microelectronic manufactory, new technologies and requirements for high level of miniaturization in some application areas [1]. These facts is need to get in conjunction with the end cost of the manufacturing process and new challenges around environmental improvements which lead to greener manufactory and it can be often in conflict with the previous factors. The most significant and visible in this area is effort to replace hazardous substances or at least reduce their share in the complete product if this is possible. Furthermore, it is a necessity to reduce demands on the energy which is consumed in the production process. These requirements are applied and implemented in two European standards which have huge impact on industrial production. First standard is called RoHS (Restriction of Hazardous Substance) and it has main aim which is substitution or limitation of toxic materials from manufactory. Furthermore, it is standard WEEE (Waste Electrical and Electronic Equipment) where the goal is add and increase for effectiveness about disposal and recycling of all types of waste from manufactory [2]. In the electrical production is currently in solving the reliability of new types solder pastes because reliable solder Sn63Pb37 was eliminated from the process due toxic lead. Among the substitutes include mainly lead-free solder paste SAC305 which is very similar to eutectic solder and it is possible to consider this solder as reliable because were obtained a lot of information about her reliability [3]. The reliability of SAC305 is still good and useful to watch for obtain of large data set and it is appropriate to introduce simultaneously computer analysis because it reduces costs during tests of new types of solders and processes to manufactory and it is certain that it is needed because SAC305 is not solder only with advantages and the results of experiments about the reliability of computer analysis will be useful also for other types of solder pastes in the next future.

2. PREPARATION OF TESTING BOARDS FOR ANALYSIS

The evaluation of reliability is usually performed by using of different kinds of testing methods which includes thermal cycling in the thermal chamber or some vibration tests. The main subject of testing are soldered joints on ceramic resistor arrays in configuration 8x0603. There is some need for miniaturization on current printed circuit boards because it is necessary to produce compact products and these packages offer some saving of space on PCB. The saving of space can be about 30 % in comparison with using of eight classic SMD 0603 resistors. This fact is shown on figure (1).

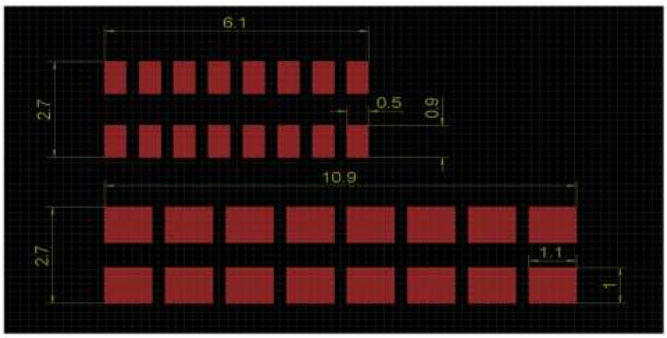

Figure 1: Comparison of solder pads for classic SMD 0603 part and pads for resistor arrays

Other advantage of choice of these parts is their relatively large size of ceramic package of resistor arrays and it is good feature for experiments because advanced microelectronic components are often made from ceramic materials or contains some share of ceramic materials and it can be problematic in conjunction with typical FR-4 substrate. There are many factors which can be negative for overall reliability of soldered connection. The main problem can be especially different coefficients of thermal expansion and it leads to increasing of stress in solder joint under condition of thermal cycling in thermal chamber. There were prepared about 35 same samples of boards for testing and ever board includes two resistor arrays. It means that there is available about 70 resistor arrays for evaluation of reliability of solder joints. It is sufficient number of samples according to standard IPC-9701A where is prescribed about 35 samples. Temperature profile for soldering in vapors is shown on figure (2a) and soldered test board on figure (2b). The FR-4 substrate is type Isola DE104 [4], thickness of cooper pads about 18 µm and pads are protected by lead-free HAL. The resistor arrays were soldered by vapor soldering in chamber Asscon Quicky 300 and there was used SAC305 solder paste Indium 8.9HF [5].

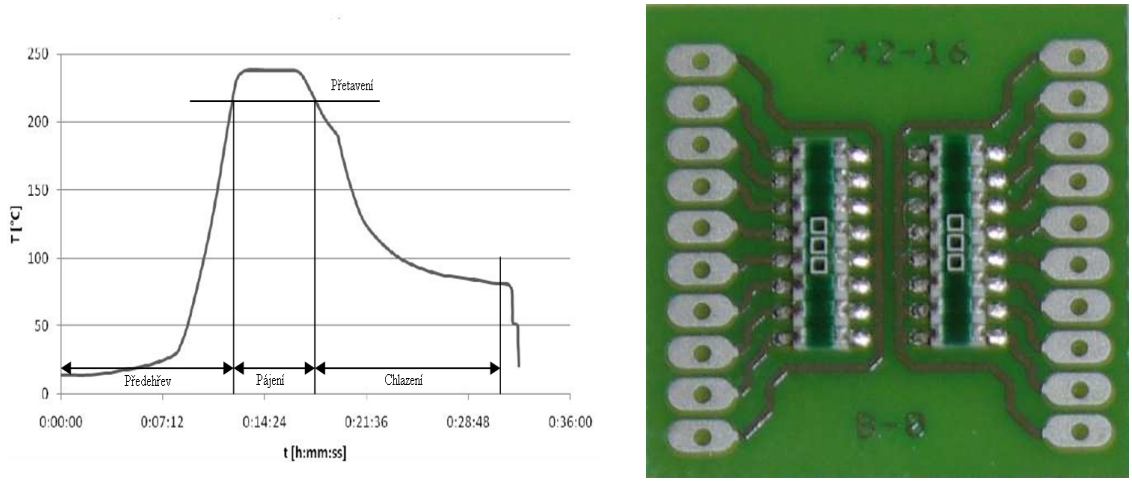

Figure 2: (a) Temperature profile for soldering by vapors (b) Assembled test board with soldered resistor arrays

3. PROCESS OF CREATION OF MODEL FOR SIMULATION PURPOSES

The models for simulation of reliability of resistor arrays were created exactly according to their real pattern. The complete model is composed from ceramic resistor array, FR-4 substrate, cooper pads and solder joints. Furthermore there are included some intermetallic layers for more precise simulations. It is common that there are created two types of intermetallic layers. One type of intermetallic layer is between cooper solder pad and solder joint which is composed from SAC305 and typical compound of intermetallic layer is Cu6Sn5 [6]. Other type of intermetallic layer is on the interface of ceramic resistor array and solder joint and in this case it is Ni3Sn4. It is because surfaces of pads for soldering on ceramic arrays are made from nickel and there is created compound Ni3Sn4 during interaction with solder paste SAC305 [7]. The models of ceramic resistor arrays and complete model with FR-4 are shown on figure (3).

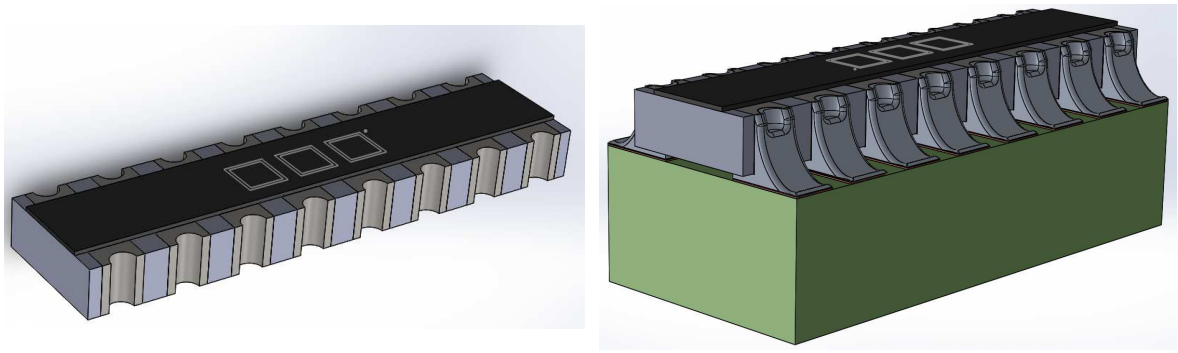

Figure 3: Solidworks – (a) model of ceramic resistor array (b) complete model of ceramic resistor array with FR-4 substrate

The hardest part of creating of model is to draw model of solder joint and to capture right angle of wetting, because there are very complex shapes. The best methods is to make some microsections of testing boards and it offers precise view on the solder joint. In this case there were used some images from ERSA microscope for initial simulations because it is very fast and simple method. The method of preparation of microsection will use for other experiments in future and for refinement for actual simulations. The example of image from ERSA microscope is shown on figure (4a) and the detail of model of solder joint on figure (4b).

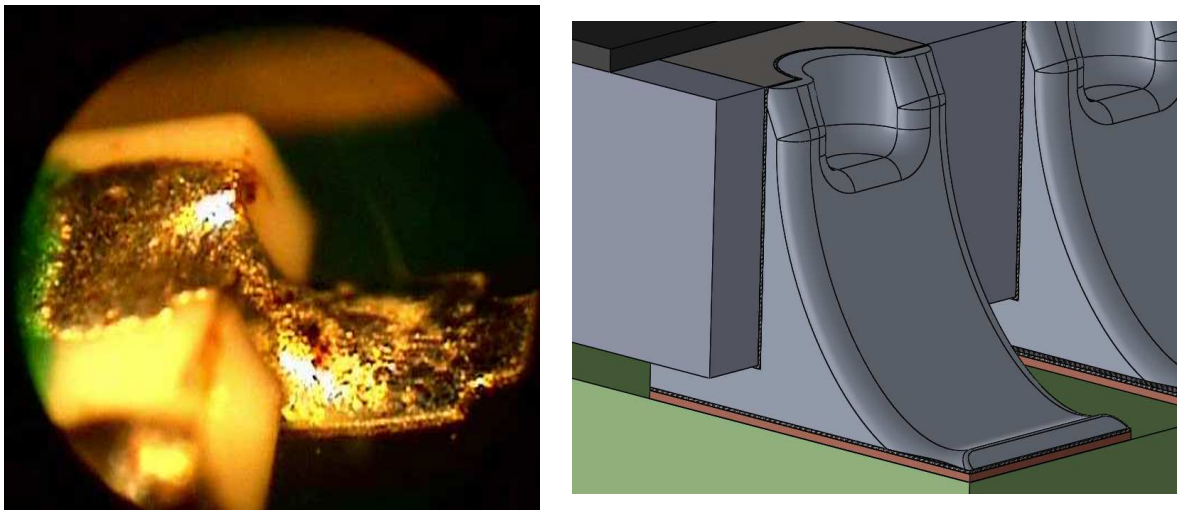

Figure 4: (a) Detail of solder joint on ceramic resistor arrays achieved by ERSA microscope (b) Created model of solder joint by his pattern from ERSA

4. THE RESULTS OF PRACTICAL EXPERIMENTS AND SIMULATIONS

Temperature cycling was performed due to standard IPC-9701A [8] and for purposes of cycling was chosen temperature chamber CTS T-40/25 and there was used cycling profile which is shown on figure (5). Selected profile is in category of automotive and closely for area of underhood in the car. This profile has temperature range from -30 °C to 120 °C with 30 minutes of dwell time on maximal and minimal temperature. There is supposed for experiments that will be achieved about 4000 cycles in the case of same solder SAC305 and same cycling profile. This paper presents results after 2000 cycles because the experiment is still in progress. One of the test boards after 2000 cycles is shown on figure (5b).

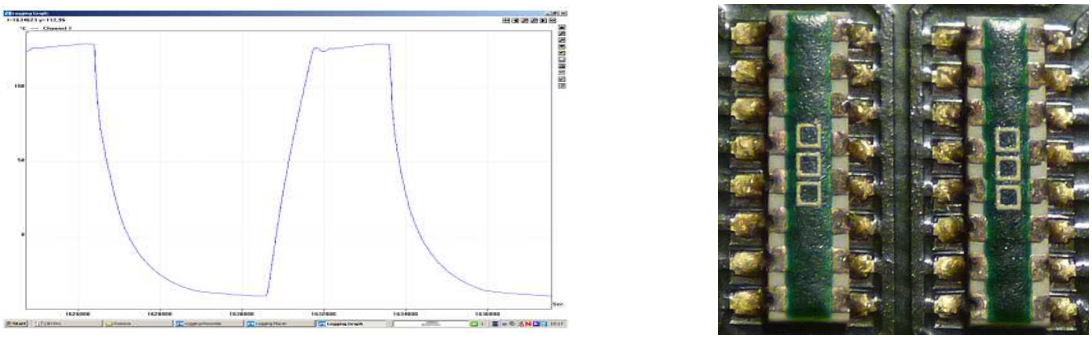

Figure 5: (a) The selected temperature profile for cycling of test boards (b) One of the test boards after 2000 cycles

There is major assumption for experiments that lowest reliability of solder joints on ceramic packages will be in area of corners of packages because there is the highest level of stress due to different thermal coefficients of expansion of FR-4 substrate and ceramic resistor array [9]. The assumption of the lowest level of stress is about center of ceramic package. All of these assumptions have been confirmed by experimental measurements in temperature chamber and in this paper are introduced results achieved after 2000 cycles. The results shows that first failures of solder joints start on corners of resistor array. This is shown on figure (6a). There are soldered joints on one side of resistor array from number one to eight and the reliability of soldered joints increases toward the center of package. There are not values in the area of A4 solder joints because it was completely without failures to 2000 cycles. The results obtained by practical measurements were also confirmed by simulations in ANSYS. Figure (6b) achieved from ANSYS shows that the highest level of stress is on the first solder joint and gradually decreases towards center.

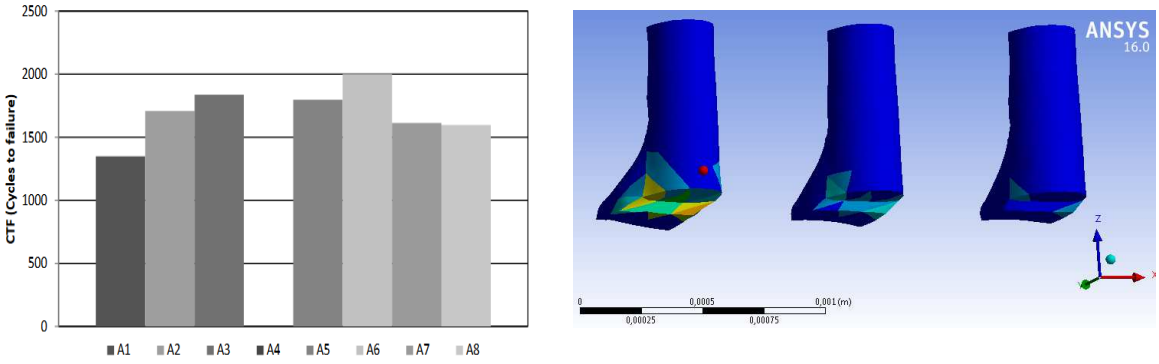

Figure 6: (a) Number of cycles to failure of solder joints according to area of location of solder joint (b) Thermal-Structural simulation of resistor array under condition of thermal cycling

CONCLUSION

Article provides theoretical information about the area of reliability of solder joints on ceramic resistor arrays and possible reasons for application in surface mount assembly. There were also made test boards with resistor arrays in the experiment and were compared with results achieved by simulations in ANSYS. There was assumption that ceramic resistor arrays can contain some problematic areas and it was confirmed by practical measurements and simulations in ANSYS. The results show that lower reliability of solder joints is in the corners of ceramic package of resistor array and there were identified first fractures in solder joints about 1400 cycles in comparison with center of package, where first failures were identified about 2000 cycles and further. These results were also in conjunction with ANSYS simulations. Solder joints with other types of solder pastes will be further investigated in thermal cycling chamber.

ACKNOWLEDGEMENT

Funding for this research was obtained through grant project FEKT-S-17-3934 “Utilization of novel findings in micro and nanotechnologies for complex electronic circuits and sensor applications”.

REFERENCES

[1] ŠANDERA, J. 2010. *Technology and reliability of solder connection electronic modules and compoments [i.e. components] in surface mount assembly: short version of habilitation thesis*. Brno: VUTIUM. ISBN 978-80-214-4221-4.

[2] ENGELMAIER, W. 1989. *Surface Mount Solder Joint Long-term Reliability: Design, Testing, Prediction*. In: . AT&T Bell Laboratories, Whippany, New Jersey, USA: MCB UP Ltd, s. 9. DOI: http://dx.doi.org/10.1108/eb037660. ISSN 0954-0911.

[3] ŠVECOVÁ, O. 2012. *Reliability of lead-free solders and the selected methods to estimate its lifetime*. Brno. Doctoral thesis. Brno University of Technology, Faculty of Electrical Engineering and Communication. Supervisor of doctoral thesis Doc. Ing. Josef Šandera, PhD.

[4] *Isola DE104 Laminate* [online]. Isola corp. Dostupné z: http://www.isola-group.com/wp-content/uploads/2013/04/DE104-Laminate-and-Prepreg-Data-Sheet-Isola.pdf

[5] *Indium8.9HF Pb-Free Solder Paste: Product datasheet* [online]. 2014. Indium Corporation [cit. 2016-03-02]. Available from: http://www.indium.com/

[6] PUTTLITZ, Karl J a Kathleen A STALTER. Handbook of lead-free solder technology for microelectronic assemblies: a special issue of Journal of Materials Science: Materials in Electronics. New York: Marcel Dekker, 2007, xi, 1026 p. Mechanical engineering (Marcel Dekker, Inc.), 170. ISBN 08-247-4870-0.

[7] SANAPALA, R. *Characterization of FR-4 Printed Circuit Board Laminates Before and After Exposure to Lead-free Soldering Conditions*. ProQuest, 2008. [cit. 2014-04-17]. 75s. ISBN 054966193X, 9780549661931

[8] IPC-9701. *Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments*. Northbrook, Illinois, 2002.

[9] ŠANDERA, Josef. *Měření termomechanické spolehlivosti pájených spojů*. [online]. [cit. 2014-04-24]. Dostupné z: http://www.smtplus.cz/pdf/termomechspolspoju.pdf