



DIGITAL  
LIBRARY

dspace.vutbr.cz

# Tunable Fractional-Order Capacitance Multiplier Using Current Gain Adjustment

ŠOTNER, R.; JEŘÁBEK, J.; LANGHAMMER, L.

Proceedings of the 2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS)

eISBN: 978-1-7281-6044-3

DOI: <https://doi.org/10.1109/ICECS49266.2020.9294960>

Accepted manuscript

©2020 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. ŠOTNER, R.; JEŘÁBEK, J.; LANGHAMMER, L. "Tunable Fractional-Order Capacitance Multiplier Using Current Gain Adjustment", 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2020.

DOI: 10.1109/ICECS49266.2020.9294960. Final version is available at  
<https://ieeexplore.ieee.org/document/9294960>

# Tunable Fractional-Order Capacitance Multiplier Using Current Gain Adjustment

Roman Sotner, Jan Jerabek, Lukas Langhammer  
Faculty of Electrical Engineering and Communication  
Brno University of Technology  
Brno, Czech Republic  
Email: sotner@feec.vutbr.cz

**Abstract**—This paper brings new solution of linearly adjustable fractional-order capacitance multiplier. The adjustable current gain, linear in wide range of input current and with linear dependence on driving voltage, serves for these purposes and offers one-decade variation of equivalent capacity (pseudo-capacitance) between 24 and 429  $\mu\text{F/sec}^{3/4}$ . The operational range was tested by PSpice simulations and by measurement using RC approximant of constant phase element of the order 0.25 in bandwidth from 20 Hz up to 1 MHz.

**Keywords**—Constant phase element, electronic adjustment, fractional-order, immittance function, multiplication factor

## I. INTRODUCTION

In many cases, value of required capacity (discrete element vs integrated solution of capacitor) in application is insufficient for implementation or practically unreachable. Therefore, many solutions of active capacitance multipliers (C-MLT) have been proposed [1]. However, this feature always requires presence of certain suitable active element(s) [2]. The circuit solving indicated feature (electronically adjustable capacity) is known as adjustable impedance converter (converting value of an equivalent capacity or inductance) [1]. These principles can be beneficially used also for adjustment of the fractional-order elements using solid-state device (fractors) [3]-[7] or so-called constant phase elements (CPEs) [8], [9], because these devices are fabricated with specific equivalent value and order and there is no way how to change value without fabrication of new device. However, tunable applications (filters, oscillators, regulators, etc.) [1] require adjustment of value of passive element very often. Therefore, it is necessary to address these needs. We designate this device as CPE-MLT in further discussions.

We can note integrable topologies of C-MLTs using operational transconductance amplifier (OTAs) [2], current conveyors (CCs) [1], [2], etc. However, standard current conveyors have no possibility of direct electronic control/adjustment of parameters. The issues with linearity of the OTA (simple adjustment of transconductance is clear but there is nonlinearity of transfer response) call for searching of further solutions. Simple implementation of C- or CPE-MLTs can be designed with commercially available devices as shown in this paper.

## II. BRIEF STATE-OF-THE-ART

The adjustable capacitance multipliers and various immittance converters have been studied deeply in recent years. Brief comparison of previous (standard integer-order)

solutions [10]-[28] indicates (see Table I) that the majority of electronically adjustable multiplication factors (parameters suitable for tuning) are controlled in dependence on nonlinear value of transconductance  $g_m$  (in dependence on input voltage). Also intrinsic resistance of current input terminals ( $R_X$ ) is very nonlinear parameter in many standard cases. The performances, indicated by this feature of active device, are valid only in small-signal consideration in many cases [1], [2].

Our solution brings possibility to use linear (in wide range of input currents) current gain adjustment (linear due to good linearity of transfer responses of CCs in comparison to OTA, etc. and also low gain ranges of transfers up to units) for multiplication factor variation. Also dependence of current gain on driving force (voltage) is linear. It is not typical feature of  $g_m$  or  $R_X$  dependence on driving bias current [1], [2] and, therefore, it is advantageous for control of parameters of particular application.

TABLE I. BRIEF COMPARISON OF ELECTRONICALLY ADJUSTABLE SOLUTIONS

Reference	Number of passive; Active devices; Test*	Type of adjustment (controlled value of)	Differential-mode	Tested for fractional-order design	Widely linear parameter used for adjustment
[10]	1; 3; m	$g_m$	No	No	No
[11]	0-2; 4; s	$R_X$	Yes	No	No
[12]	1; 4; s	$g_m$	Yes	No	No
[13]	1; 4; s	$R_X$	Yes	No	No
[14]	1; 3; s	$R_X$	Yes	No	No
[15]	1;2; s	$R_X, g_m$	No	No	No
[16]	(1-2); (2-3); s	$g_m$	Yes	No	No
[17]	2; 1; s	$g_m$ , current gain	No	No	N/A
[18]	1; 3; s	$R_X$	Yes	No	No
[19]	3; 2; s	$g_m$	Yes	No	No
[20]	1; 4; s	$g_m$	Yes	No	No
[21]	2; 1; s	$g_m$	Yes	No	No
[22]	3; 2; s	$g_m$	Yes	No	No
[23]	2; 1; s	$g_m$	No	No	No
[24]	2; 1; s	$g_m$	No	No	No
[25]	2; 1; s	$g_m$	Yes	No	No
[26]	1; 5; s	$g_m$	Yes	No	No
[27]	2; 2; s	$g_m$	Yes	No	No
[28]	2; 2; b	$g_m$	No	No	No
Fig. 1	2; 1; b	current gain	Yes	Yes	Yes

\*test: s – simulated; m – measured; b – both; N/A – not available

### III. PROPOSED TOPOLOGY

The circuit topology of the CPE-MLT is given in Fig. 1. The topology is shown in fully differential form. The circuit uses differential difference amplifier (DDA) [1], [2], and electronically controllable current conveyor of second generation (ECCII) [1], [2] offering current gain ( $B$ ) adjustment that also serves as adjustable multiplication factor of the CPE-MLT. The ideal input impedance has form:

$$Z_{in}(s) = \frac{1}{s^\alpha C_\alpha \cdot B} \approx \frac{1}{s^\alpha C_\alpha \cdot V_{SET\_B}}, \quad (1)$$

where connected impedance  $Z_{CPE}$  ( $C_\alpha$ ) represents so-called passive RC approximant of fractional-order behavior [8], [9]. Figure 2 shows details about construction of ECCII (having two Z output terminals – direct and inverted).

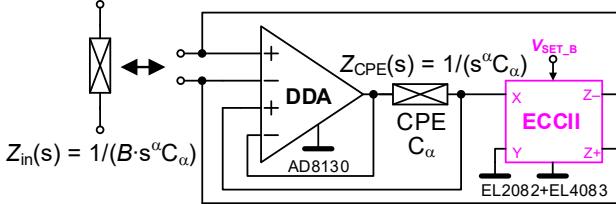


Fig. 1. Topology of the proposed CPE-MLT.

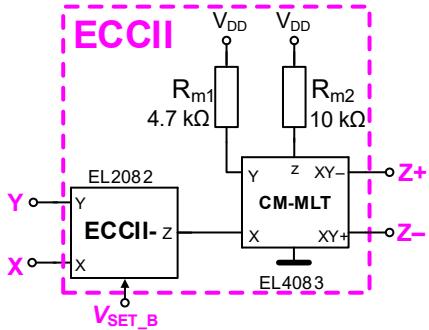


Fig. 2. Internal concept of ECCII.

TABLE II. VALUES OF PASSIVE ELEMENTS USED IN CPE

$C_\alpha = 225 \mu\text{F/sec}^{3/4} (\alpha = 1/4)$ , $C_p = 4.7 \text{ pF}$ , $R_k = 2.15 \text{ k}\Omega$										
$i$	1	2	3	4	5	6	7	8	9	10
$R_k$ kΩ	3.33 kΩ	2.1 kΩ	1.33 kΩ	842 Ω	532 Ω	336 Ω	210 Ω	135 Ω	85 Ω	53 Ω
$C_k$ μF	3 nF	748 nF	182 nF	49 nF	12 nF	3.3 nF	780 pF	200 pF	50 pF	13 pF

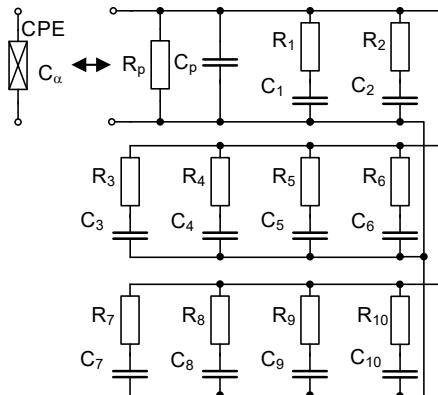


Fig. 3. RC approximant of used CPE in discussed application.

The ECCII (purple color) includes the current-mode multiplier (CM-MLT) based on EL4083 device (several OPA860 elements can be used as effective alternative [29]) where the current transfer between black-colored X and XY+, XY- terminals, respectively, is defined as:

$$I_{XY+} = -I_{XY-} = \frac{I_X I_Y}{2I_z} = I_X \cdot k, \quad (2)$$

where  $k$  is set by external resistors (values in Fig. 2) to value:

$$k = \frac{I_Y}{2I_z} \approx \frac{R_{m2}}{2R_{m1}} \approx 1. \quad (3)$$

Therefore, CM-MLT serves as simple current follower and inverter that is required by proposed application in Fig. 1. The first and adjustable part of the purple ECCII (Fig. 2) implements current gain adjustment based on EL2082 (also known as ECCII or current-mode multiplier, but having single output terminal Z) The standard terminal relations are valid for this device:  $V_Y = V_X$ ,  $I_Y = 0$ ,  $I_Z = -B I_X$  [30]. The current gain is defined approximately as  $B \approx V_{SET\_B}$  (perfectly valid from 0 up to 2). Despite obsolete status of EL2082, the alternative solution of the device having, identical principal behavior, can be found in [31].

The DDA device [2], [32] has simple principle and works as unity-gain summing/subtracting unit:  $V_{out} = V_+ - V_- + V_+$  when full negative feedback by the fourth remaining (negative) input is connected to output of the device.

The CPE device is shown in Fig. 3. Table II shows values of RC parameters (obtained by algorithm presented by Valsa et al. in [8], [9]) used in CPE that forms equivalent value  $C_\alpha = 225 \mu\text{F/sec}^{3/4}$ ,  $\alpha = 1/4$ , and operational bandwidth 100 Hz → 10 MHz with maximal phase ripple (verified by simulation)  $\Delta\phi = \pm 2^\circ$ .

### IV. EXPERIMENTAL TEST

The DUT connection to measuring system is shown in Fig. 4. We used Keysight DSOX-3022T oscilloscope having frequency response analysis (FRA) option and equipment using AD844 current feedback operational amplifier (CFOA) that allowed measurement of complex impedance in form of transfer response (Bode plot) because:

$$Z_{unknown}(s) = \frac{V_2(s)}{V_1(s)} \cdot R, \quad (4)$$

where magnitude and phase response are defined as:

$$|Z_{unknown}| = 10^{\frac{K_V[\text{dB}]}{20}} \cdot R, \quad (5)$$

$$\varphi_{Z_{unknown}} = \arg(K_V(s)). \quad (6)$$

The level of input sine waveform was set as 100 mV (amplitude). This method provides reliable results up to units of MHz, then parasitic poles of CFOA (tens of MHz) start to have significant influence on phase and magnitude response.

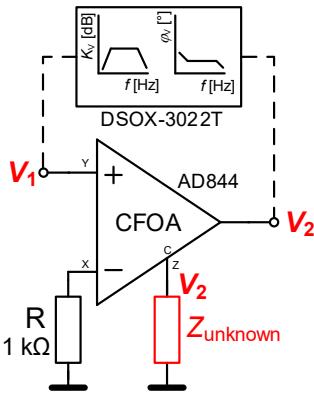


Fig. 4. Experimental arrangement of DUT ( $Z_{\text{unknown}}$ ) and measuring device.

The experimental results are performed for current gain  $B$  ( $V_{\text{SET\_B}}$  respectively) varying from 0.1 up to 2. Selected traces are shown in Fig. 5. Note that real setting of current gains (driving voltages  $V_{\text{SET\_B}}$ ) was slightly different than in ideal case (we used 0.07, 0.16, 0.42, 0.8 and 2 V actually). The uncertainty of gain value (tracking error) in the real EL2082+EL4083 cascade causes these mismatches. Nevertheless, this is not conceptual (topological) issue but it depends on specific construction of ECCII $\pm$  in Fig. 1. Figure 6 implies the dependence of input capacity on driving voltage  $V_{\text{SET\_B}}$ . The ideal equivalent capacity (so-called pseudo-capacitance) varies between 22.5 and 449  $\mu\text{F/sec}^{3/4}$  for discussed range of  $V_{\text{SET\_B}}$  adjustment. The PSpice simulation yields adjustment from 23 up to 409  $\mu\text{F/sec}^{3/4}$  and experiment from 24 up to 429  $\mu\text{F/sec}^{3/4}$ . The error in the corner values of the range reaches up to 7% for experiment and 9% for simulation. The active circuitry degrades supposed phase ripple that now reaches  $\pm 3^\circ$  in bandwidth from 200 Hz up to 40 kHz (more than 2.5 decades) in indicated range of  $B$  variation. The example of time-domain responses for sine wave (1 kHz, 100 mV amplitude) input signal of the measuring chain ( $V_{\text{SET\_B}} = 0.07$  V) in Fig. 4 is shown in Fig. 7. The total harmonic distortion (THD) of the output signal (in accordance with Fig. 7) reaches 0.53% (see Fig. 8). The simulated power consumption of whole measuring chain, including DUT, reaches 374 mW. The experiment also shown power consumption slightly below 400 mW.

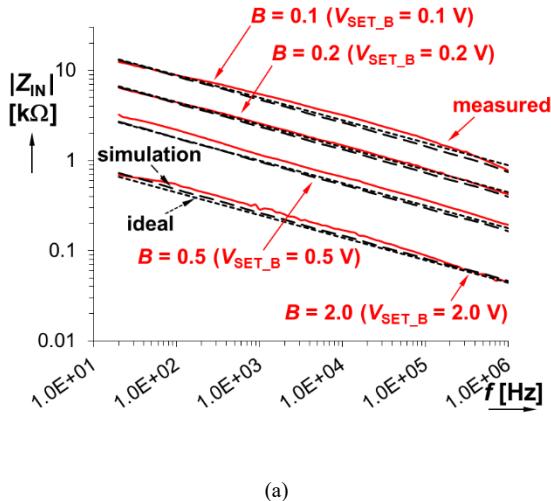


Fig. 5. Impedance characteristics of proposed CPE-MLT: a) magnitude plots, b) phase plots.

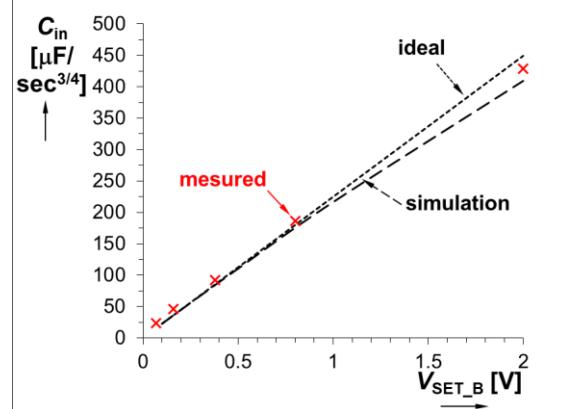


Fig. 6. Dependence of input capacity of the CPE-MLT on driving voltage.

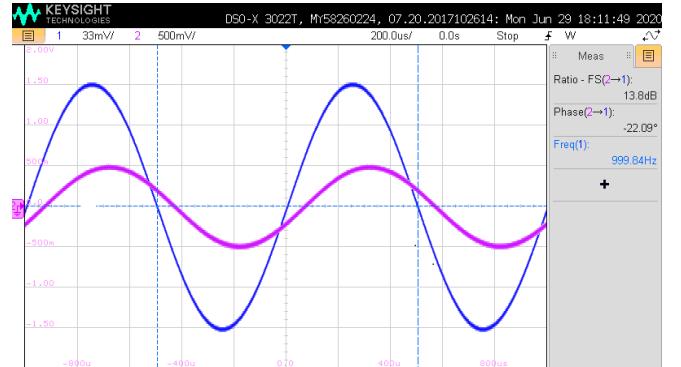


Fig. 7. Time domain response of the measuring chain (blue color – input wave, purple color – output wave).

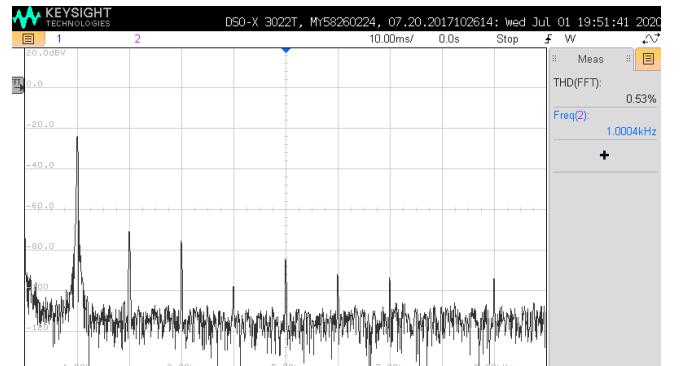


Fig. 8. FFT spectrum of the output signal at 1 kHz.

## V. CONCLUSION

We proposed CPE value converter allowing change of equivalent value of capacity (pseudo-capacitance) from 24 up to  $429 \mu\text{F/sec}^{3/4}$  (real measurement results). It is more than one decade adjustment of value that is important for final applications, especially in tunable circuits (filters and oscillators for example). The paper also shows that usage of commercially available building blocks leads to simple and compact solution (no special devices integrated on IC are required). The advantage of our solution consists also in good linearity in comparison to low-voltage low-power integrated solutions using adjustable  $g_m$  stages, etc. (ten to hundred times higher processed levels). On the other hand, additional simplification of resulting topology can be reached when integrated form is used for design of these active circuits. Real implementation of presented concept in IC form requires further precise analysis of fabrication dispersion (Monte Carlo and process, voltage, temperature + corners) especially for passive solution of CPE as well as active circuitry.

## REFERENCES

- [1] R. Senani, D. R. Bhaskar, and A. K. Singh, *Current Conveyors: Variants, Applications and Hardware Implementations*. Switzerland: Springer International Publishing, 2015.
- [2] D. Bolek, R. Senani, V. Biolkova, Z. Kolka, "Active elements for analog signal processing: Classification, Review and New Proposals," *Radioengineering*, vol. 17, no. 4, pp. 15–32, 2008.
- [3] P. Ushakov, A. Shadrin, D. Kubanek, and J. Koton, "Passive fractional-order components based on resistive-capacitive circuits with distributed parameters," in *Proceedings of 39th International Conference on Telecommunications and Signal Processing (TSP)*, Vienna, Austria, 2016, pp. 638–462.
- [4] M. Krishna, S. Das, K. Biswas, B. Goswami, "Fabrication of a fractional order capacitor with desired specifications: a study on process identification and characterization," *IEEE Transactions on Electronics Devices*, vol. 58, no. 11, pp. 4067–4073, 2011.
- [5] A. Adhikary, M. Khanra, S. Sen, K. Biswas, "Realization of carbon nanotube based electrochemical fractal," In *Proceedings of IEEE Int. symposium on Circuits and Systems (ISCAS)*, Lisbon, Portugal, pp. 2329–2332, 2015.
- [6] A. M. Elshurafa, M. N. Almadhoun, K. N. Salama, H. N. Alshareef, "Microscale electrostatic fractional capacitors using reduced graphene oxide percolated polymer composites," *Applied Physics Letters*, vol. 102, no. 102, pp. 232901, 2013.
- [7] A. Kartci, A. Agambayev, N. Herencsar, K. N. Salama, "Series-, Parallel-, and Inter-Connection of Solid-State Arbitrary Fractional-Order Capacitors: Theoretical Study and Experimental Verification," *IEEE Access*, vol. 6, no. 1, pp. 10933–10943, 2018.
- [8] J. Valsa, P. Dvorak, M. Friedel, "Network model of CPE," *Radioengineering*, vol. 20, no. 3, pp. 619–626, 2011.
- [9] J. Valsa, J. Vlach, "RC models of a constant phase element," *International Journal of Circuit Theory and Applications*, vol. 41, no. 1, pp. 59–67, 2013.
- [10] I. A. Khan and M. T. Ahmed, "OTA-based integrable voltage/current-controlled ideal C-multiplier," *Electronics Letters*, vol. 22, no. 7, pp. 365–366, 1986.
- [11] M.T. Abuelma'atti, and N.A Tasadduq, "Electronically tunable capacitance multiplier and frequency-dependent negative-resistance simulator using the current-controlled current conveyor," *Microelectronics Journal*, vol. 30, no. 9, pp. 869–873, 1999.
- [12] W. Jaikla and M. Siripruchyanan, "An Electronically Controllable Capacitance Multiplier with Temperature Compensation," In *Symp. On Communications and Information Technologies*, Bangkok, Thailand, 2006, pp. 356–359.
- [13] E. Yuce, S. Minaei, and O. Cicekoglu, "Resistorless floating immittance function simulators employing current controlled conveyors and a grounded capacitor," *Electrical Engineering*, vol. 88, pp. 519–525, 2006.
- [14] M. Siripruchyanan and W. Jaikla, "Floating capacitance multiplier using DVCC and CCCII," In *Symp. On Communications and Information Technologies*, Sydney, Australia, 2007, pp. 218–221.
- [15] P. Silapan, C. Tanaphatsiri and M. Siripruchyanan, "Current Controlled CCTA Based- Novel Grounded Capacitance Multiplier with Temperature Compensation," In *Proc. of IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Macao, China, 2008, pp. 1490–1493.
- [16] T. Kulej, "Regulated capacitance multiplier in CMOS technology," In *Proc. of Int. Conf. on Mixed Design of Integrated Circuits & Systems (MIXDES)*, Lodz, Poland, 2009, pp. 316–319.
- [17] A. De Marcellis et al., "The VCG-CCII: a novel building block and its application to capacitance multiplication," *Analog Integrated Circuits and Signal Processing*, vol. 58, pp. 55–59, 2009.
- [18] P. Prommee, and M. Somdunyakanok, "CMOS-based current-controlled DDCC and its applications to capacitance multiplier and universal filter," *AEU – Int. J. of Elect. and Commun.*, vol. 65, no. 1, pp. 1–8, 2011.
- [19] U. E. Ayten, M. Sagbas, N. Herencsar, and J. Koton "Novel Floating General Element Simulators Using CBTA," *Radioengineering*, vol. 21, no. 1, pp. 11–19, 2012.
- [20] Y.-A. Li, "A series of new circuits based on CFTAs," *AEU – Int. J. of Elect. and Commun.*, vol. 66, no. 7, pp. 587–592, 2012.
- [21] A. Kartci and et al., "Floating capacitance multiplier simulator for grounded RC colpitts oscillator design," In *Proc. of Applied Electronics (AE)*, Pilsen, Czech Republic, 2015, pp. 93–96.
- [22] A. Kartci, and et al., "Application possibilities of VDCC in general floating element simulator circuit," In *Proc. of European Conference on Circuit Theory and Design (ECCTD)*, Trondheim, Norway, 2015, pp. 1–4.
- [23] S. Unhavanich, O. Onajn, and W. Tangsrirat "Tunable Capacitance Multiplier with a Single Voltage Differencing Buffered Amplifier," In *Proc. of the International MultiConference of Engineers and Computer Scientists (IMECS)*, Hong Kong, China, 2016, pp. 1–4.
- [24] W. Tangsrirat, "Resistorless tunable capacitance multiplier using single voltage differencing inverting buffered amplifier," *Rev. Roum. Sci. Techn. – Électrotechn. et Énerg.*, vol. 62, no. 1, pp. 72–75, 2017.
- [25] W. Tangsrirat, and O. Channumsin, "Tunable Floating Capacitance Multiplier Using Single Fully Balanced Voltage Differencing Buffered Amplifier," *J. Commun. Technol. Electron.*, vol. 64, pp. 797–803, 2019.
- [26] M. A. Al-Absi and A. A. Al-Khulaifi, "A New Floating and Tunable Capacitance Multiplier with Large Multiplication Factor," *IEEE Access*, vol. 7, pp. 120076–120081, 2019.
- [27] M. A. Al-Absi and A. A. Al-Khulaifi, "Realization of a Large Values Floating and Tunable Active Inductor," *IEEE Access*, vol. 7, pp. 42609–42613, 2019.
- [28] M. A. Al-Absi and M. T. Abuelma'atti, "A Novel Tunable Grounded Positive and Negative Impedance Multiplier," *IEEE Trans. on Circs. and Syst. II: Express Briefs*, vol. 66, no. 6, pp. 924–927, 2019.
- [29] D. Bolek, V. Biolkova, "Implementation of active elements for analog signal processing by diamond transistors," In *Proc. of International Conference on Electronic Devices and Systems EDS 2009*, Brno, Czech Republic, 2009, pp. 304–309.
- [30] R. Sotner, L. Langhammer, J. Petrzela, O. Domansky and T. Dostal, "Applications of novel behavioral implementation of a controllable generalized current conveyor," In *Proc. of 2018 28th International Conference Radioelektronika (RADIOELEKTRONIKA)*, Prague, Czech Republic, 2018, pp. 1–6.
- [31] R. Sotner, J. Jerabek, L. Langhammer, J. Polak, N. Herencsar, R. Prokop, J. Petrzela, W. Jaikla, "Comparison of Two Solutions of Quadrature Oscillators With Linear Control of Frequency of Oscillation Employing Modern Commercially Available Devices," *Circuits, Systems and Signal Processing*, vol. 34, no. 11, pp. 3449–3469, 2015.
- [32] R. Sotner, N. Herencsar, V. Kledrowetz, A. Kartci and J. Jerabek, "New Low-Voltage CMOS Differential Difference Amplifier (DDA) and an Application Example," In *Proc. of 2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, Windsor, ON, Canada, 2018, pp. 133–136.