CHANNEL MERGING TECHNIQUES FOR IMPROVING DYNAMIC RANGE OF ± 10V SIGNAL CHAIN

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Abstract: This paper presents the channel merging technique that is used in the Analog Devices part AD7606C. In more detail, it describes the current dynamic range (DR) and total harmonic distortion (THD) performance that has been achieved on the first AD7606C silicon. Then, it presents options to achieve higher values of the DR and also options to mitigate the undesirable non-linear current which decreases the THD performance.

Keywords: dynamic range, signal chain, signal-to-noise ratio, channel, merging, saturation, total harmonic distortion

1 INTRODUCTION

It might be the case that there are two channels on the existing die each working separately with a certain DR performance which these channels alone can not exceed. But, if the requirement from the customer is to achieve higher values of the DR on the same die, the channel merging technique might be used. If two channels connected together on their inputs are used in order to create one signal chain and both channels are working with different input ranges, better DR performance might be achieved without a lot of changes to the original die. Such a technique was introduced in the Analog Devices part AD7606C, which is an eight-channel part with eight SAR ADCs running at 800 kHz. How this technique works in AD7606C and what performance can be achieved with such a technique is in more detail described in sections 2 and 3.

However, such a technique might be introducing some issues as well. It was discovered while measuring the AD7606C performance that the THD decreases rapidly with increasing value of the external resistor which customers usually use as a part of an anti-aliasing filter in front of the AD7606C. As this is a highly undesirable phenomenon, this paper also presents three options to mitigate this issue. These options are presented in more detail in section 5.

2 THE AD7606C CHANNEL MERGING TECHNIQUE

The AD7606C channel merging technique currently uses two of its channels, where one channel is set to ± 2.5 V range and the other one is set to ± 10 V range. As can be seen in figure 1, both channels are connected to their inputs and outputs of these channels are connected to the internal logic block which creates a new 20-bit signal based on the code values coming from the channel with the ± 10 V range. If codes represent values from -2.5 V to 2.5 V, the codes from the ± 2.5 V channel are directly transferred to the output of the internal logic block. If codes represent values lower than -2.5 V or higher than 2.5 V, the codes from the ± 10 V channel are logically shifted by 2 bits to the left and then transferred to the output of the internal logic block. Such a technique should, in theory, add 12 dB of DR performance in comparison with a case where the ± 10 V range channel works alone [1].

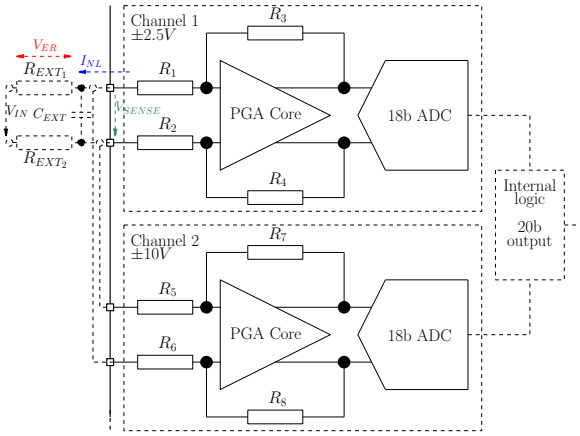

Figure 1: Block diagram of the AD7606C channel merging technique with the external filter

3 THE MEASURED PERFORMANCE

To evaluate the performance of the channel merging technique described in section 2 measurements were performed in the laboratories of the Analog Devices company. As the aim of this paper is to propose options to improve the DR and the THD performance, only the results are shown in this paper even though many others have been performed.

3.1 THE DYNAMIC RANGE PERFORMANCE

It was discovered that the presented AD7606C channel merging technique can achieve the DR of 115 dB with an oversampling ratio (OSR) equal to 256 as can be seen in figure 2. That is only an extra 5 dB in comparison with the ±10 V range channel working alone. The reason why the extra 12 dB has not been measured is the different signal-to-noise ratio of both channels.

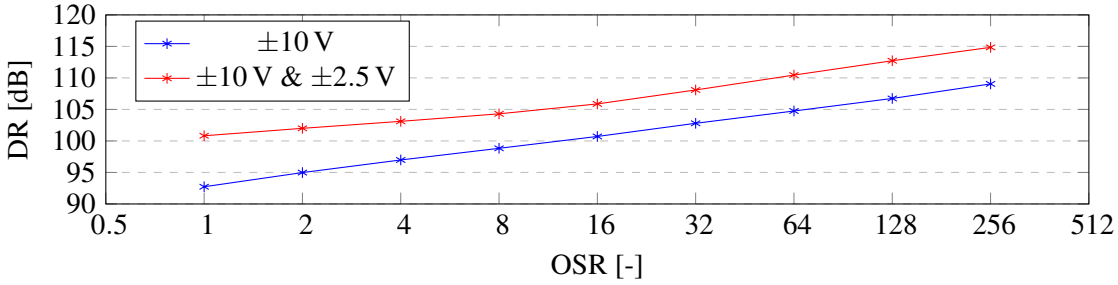

Figure 2: The measured DR performance

As the AD7606C customers were interested in higher DR performance, three options on how to obtain better results were proposed and are presented in section 4.

3.2 THE TOTAL HARMONIC DISTORTION PERFORMANCE

The AD7606C channel merging technique is sensitive to the value of the external resistor because once the input signal is higher or lower than ±2.5 V, the ±2.5 V range channel is in saturation and this results in non-linear current going out of this channel to the input of the AD7606C as is depicted in figure 1. This non-linear current than generates non-linear voltage over the external resistor and decreases the THD performance. The sensitivity to the value of the external resistor can be seen in figure 3.

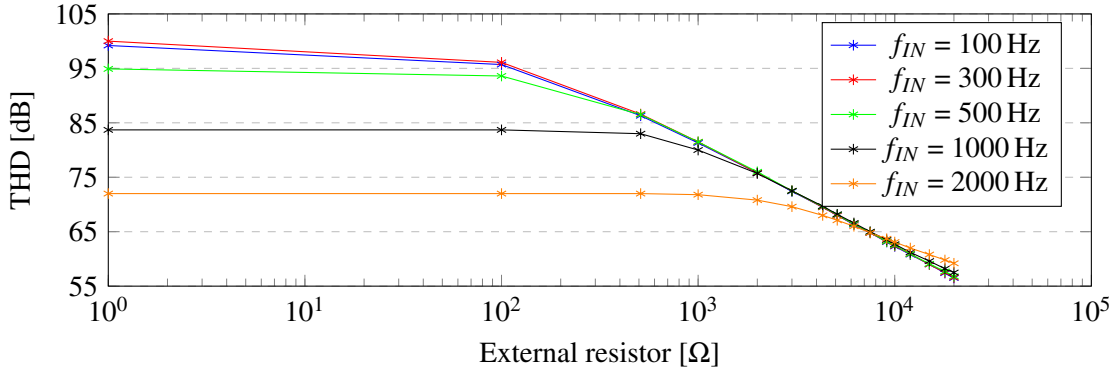

Figure 3: The measured THD performance

It was discovered that the THD decreases rapidly with the increasing value of the external resistor. Thus, techniques to mitigate this phenomenon were proposed and are presented in section 5.

4 OPTIONS TO IMPROVE THE DYNAMIC RANGE PERFORMANCE

Three options to improve the AD7606C DR performance were proposed, designed and simulated. Ideas behind all three options are summarized in the following list and the results obtained are presented in figure 4.

1. Decrease the cutoff frequency of the whole signal chain to the half. This will reduce the noise in the circuit, increase the signal-to-noise performance and thus the DR as well.
2. Decrease the range from the second channel ± 2.5 V to ± 1.25 V. This will add 1 extra bit to the final output signal and in theory should add extra 18 dB to the DR performance. The downside of this option is the necessity of reducing the input impedance to half of its original value.
3. Combination of option 1 and 2.

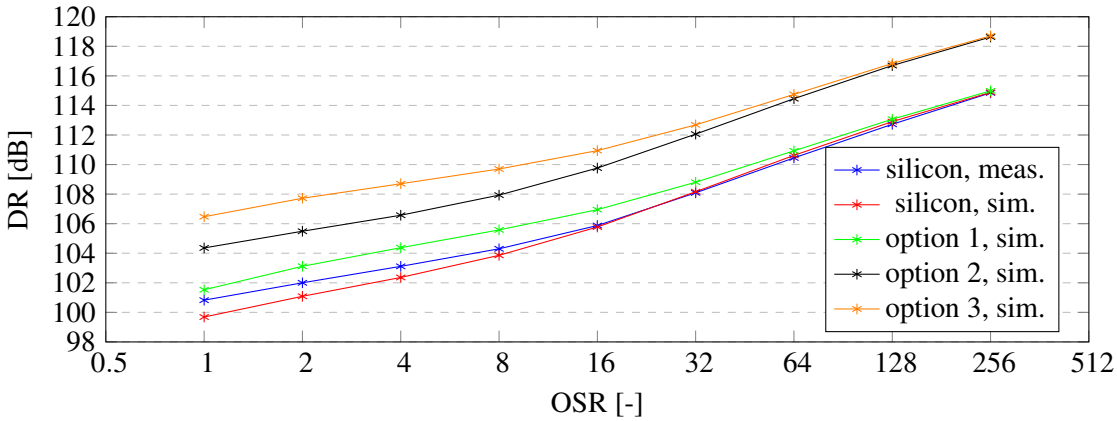

Figure 4: The DR performance of proposed options to improve current solution

5 MITIGATION OF THE NON-LINEAR CURRENT

Three options to mitigate the issue with the non-linear current, which causes the THD performance degradation, were proposed, designed and simulated and are summarized in the list below. The results

from the simulations are shown in figure 5.

1. Change the range of the lower range channel to the higher values once the input signal reaches the limits of the set range. This will prevent the lower range channel from saturation and thus no non-linear current should appear in the input of the signal chain. The downside for this technique is that it can not be used with the ± 1.25 V range which improves the DR performance.
2. Disconnect the lower range channel from the signal chain and connect it to the ground every time the input signal is outside of its range. This will prevent the non-linear current flowing through the external resistor and thus no THD degradation should appear. The downside of this technique is the slow charging of all parasitic capacitance in the input node.
3. Instead of connecting the lower range channel to the ground, connect it to the sampled value of the virtual ground at the moment when the input signal is about to leave the range of the lower range channel. This technique removes the downside of option 2, but on the other hand, the sample and hold circuit is necessary to add to the circuit, which might be area demanding.

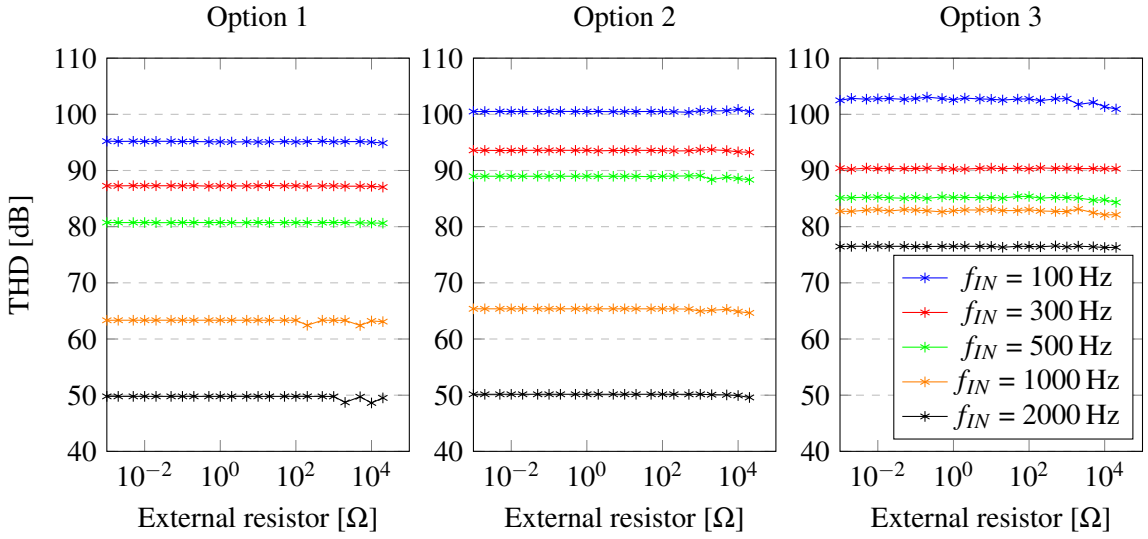

Figure 5: The THD performance of proposed options to mitigate the issue with the non-linear current

6 CONCLUSION

It was discovered that the AD7606C channel merging technique can achieve 115 dB of DR on the current silicon. But, if range ± 1.25 V will be added and the cutoff frequency of the whole signal chain will be decreased to half, the DR performance can be increased to 118.6 dB.

Also, it has been discovered during the measurements, that the AD7606C channel merging technique is highly sensitive to the external resistor as the THD performance is rapidly decreasing with the increasing value of this resistor. Thus, three options to mitigate this issue were proposed, designed and simulated. All three options were able to mitigate this issue as can be seen in figure 5. The best option to choose would probably be option 2 as it requires minimal changes to the circuitry and can be used with the newly introduced ± 1.25 V range.

REFERENCES

[1] BYRNE, E., ANALOG DEVICES, INC. *AD7606C Channel Merging*. Limerick, 2018.