Fractional-order integrator and its application in FLF fractional-order frequency filter

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Abstract—The main aim of this paper is to introduce the proposal of fractional integrator by approximation of the integer-order follow-the-leader-feedback topology (FLF). Current differencing transconductance amplifier (CDTA) is used in the integrator due to the higher versatility of this building block. The proposed integrator is also implemented to the frequency filter, creating a fractional-order frequency filter in FLF topology. The main advantage of this circuit is its electronic controllability. The resulting circuits (integrator and filter) are simulated in OrCAD using a transistor models in TSMC 0.18 µm technology.

Keywords—fractional integrator, fractional filter, active elements, CDTA, FLF topology

1. INTRODUCTION

Electronic circuits with fractional transfer are becoming more and more significant in last years in the field of analogue electronics and signal processing. Frequency-shift keying modulation technique using fractional-order structures [1][2], for example. Current research is, among others, focused on design of basic analogue building blocks with fractional transfer, such as integrators and differentiators. The main requirement is versatility of designed circuit structures. Electronic controllability of the circuit parameters significantly contributes to the required versatility. For that reason, nonconventional active elements with ability of controlling their parameters (transconductance, voltage or current gain, etc.) are often used or basic active elemets are modified to provide the additional possibility of control.

In the first part of this paper, CDTA (element allowing to control the transfer of current differencing unit (CDU) and transconductance of the second OTA (operational transconductance amplifier) stage) and adjustable current amplifier (ACA) are used for design of the fractional order integrator. Thanks to the electronic parameter control, the frequency and order of the structure can be easily tuned. In the next part of this paper, the proposed integrator is implemented into the frequency filter.

2. CDTA ACTIVE ELEMENT

Two-stage CDTA consist of the CDU stage and transconductance amplifier stage. This element is meant for using in current-mode circuit, because it has two current input \( p \) and \( n \) and one or more current outputs. The CDU is implemented by the OTA instead of the pair of current conveyors. Because the OTA has voltage input, I/U converter in the simplest variant of the parallel grounded resistors must be connected before the CDU unit. For the unit gain of the CDU unit applies \( R = g_{m,\text{CDU}}^{-1} \) [\( \Omega \)], where \( g_{m,\text{CDU}} \) is the transconductance of the OTA realized CDU unit.

In Figure 1 general schematic of the CDTA element is depicted. For marked currents and voltages applies \( U_p = U_n = 0 \), \( I_s = I_p - I_n \) and \( I_x = g_{m,\text{amp}} U_x \). The inner structure of the CDTA is depicted in the Figure 2. The TSMC 0.18 µm transistor-level model of the OTA does not allow to achieve higher values of transconductance so input parallel resistors \( R \) must be quite high. Thus input resistance of the CDTA is too high, specifically 670 \( \Omega \) (ideal value of current input resistance is zero). The higher input resistance can be reduced by a suitable implementation of the OTA in the CDU unit. For example, commercially available LT1228 allows to achieve transconductance up to 10 mS. The bandwith in which this model of the CDTA can be used is 37 MHz.

Possible advantage of this realization CDU, respectively CDTA, is possibility to modify this active element into the fully-differential form (necessary to use multi output OTAs) [3]. Another potential advantage lies in the possibility of replacement the resistors \( R \) by controllable resistance (for example...
OTA realized as a controllable resistor). This modification would make it possible to control the transfer of the CDU unit. In this particular implementation, the pair of the parallel passive resistors is sufficient (saving active elements).

3. FLF FRACTIONAL-ORDER INTEGRATOR/DIFFERENTIATOR

There is currently no available commercial element with fractional transfer. The fractional order of the element is marked by \( \alpha \). The ideal lossless integrator with fractional transfer has slope of the module \( S = -20 \alpha \, \text{dB/decade} \) and constant phase \( \varphi = (-90 \alpha)^\circ \). The realization of fractional-order integrator or differentiator lies in approximation of fractional-order behavior which is valid for a limited bandwidth. In this case, where fractional behavior is achieved by approximation of the integer-order FLF structure, validity bandwidth of the approximation is depending on integer order \( n \) of the FLF cascade.

A CFE approximation (continuous fraction expansion) was used to design fractional integrator. Because the used FLF structure is 3rd-order, the following relationships for 3rd-order approx. have been used

\[
\begin{align*}
a_0 &= \alpha^3 + 6\alpha^2 + 11\alpha + 6 \\
a_1 &= -3\alpha^3 - 6\alpha^2 + 27\alpha + 54 \\
a_2 &= 3\alpha^3 - 6\alpha^2 - 27\alpha + 54 \\
a_3 &= -\alpha^3 + 6\alpha^2 - 11\alpha + 6
\end{align*}
\]

where \( \alpha \) means fractional order and for integrator realization yields \( \alpha \in (-1; 0) \) [4]. The coefficients \( a_0 \) to \( a_3 \) have been substituted into the 3rd-order approximation of the Laplace operator \( s^\alpha \)

\[
s^\alpha \approx \left( \frac{a_0}{a_3} \right) s^3 + \left( \frac{a_1}{a_3} \right) s^2 + \left( \frac{a_2}{a_3} \right) s + 1 = \frac{a_0 s^3 + a_1 s^2 + a_2 s + a_3}{a_3 s^3 + a_2 s^2 + a_1 s + a_0}
\]

and then the values \( g_m, B \) were calculated by the comparison of eq. (1) with transfer function of the FLF structure depicted in Figure 3 expressed as

\[
K_{\text{I,FLF}}(s) = \frac{s^3C_1C_2C_3B_1 + s^2C_2C_3g_{m1}B_2 + sC_3g_{m1}g_{m2}B_3 + g_{m1}g_{m2}g_{m3}B_4}{s^3C_1C_2C_3 + s^2C_2C_3g_{m1} + sC_3g_{m1}g_{m2} + g_{m1}g_{m2}g_{m3}}
\]

which was found by symbolic analysis in Snap software. The designed integrator has center frequency \( \omega_0 = 1 \, \text{rad s}^{-1} \). It is necessary to multiply each transconductance by \( \tau^{-1} = \omega_0 = 2\pi f_0 \) to increase center frequency. Resulting values of \( g_m, B \) for different fractional order and \( f_0 = 100 \, \text{kHz} \) are listed in the Table I. Values of the capacitors have been selected \( C_1 = 100 \, \text{pF}, C_2 = 1 \, \text{nF} \) and \( C_3 = 10 \, \text{nF} \). Unfortunately, the values of the current gain are too high for fractional order \( \alpha = 0.7 \) and higher. There
Table I: Values of $g_{m_i}$ and $B_i$ for realization of fractional-order integrator, $f_0 = 100$ kHz

<table>
<thead>
<tr>
<th>$\alpha$</th>
<th>0.1</th>
<th>0.2</th>
<th>0.3</th>
<th>0.4</th>
<th>0.5</th>
<th>0.6</th>
<th>0.7</th>
<th>0.8</th>
<th>0.9</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_{m_{amp1}}$ [$\mu$S]</td>
<td>497</td>
<td>440</td>
<td>391</td>
<td>350</td>
<td>314</td>
<td>283</td>
<td>255</td>
<td>230</td>
<td>208</td>
</tr>
<tr>
<td>$g_{m_{amp2}}$ [$\mu$S]</td>
<td>568</td>
<td>514</td>
<td>464</td>
<td>419</td>
<td>377</td>
<td>338</td>
<td>303</td>
<td>269</td>
<td>238</td>
</tr>
<tr>
<td>$g_{m_{amp3}}$ [$\mu$S]</td>
<td>608</td>
<td>524</td>
<td>444</td>
<td>370</td>
<td>300</td>
<td>233</td>
<td>170</td>
<td>110</td>
<td>54</td>
</tr>
<tr>
<td>$B_1$ [-]</td>
<td>0.69</td>
<td>0.48</td>
<td>0.33</td>
<td>0.22</td>
<td>0.14</td>
<td>0.10</td>
<td>0.05</td>
<td>0.03</td>
<td>0.01</td>
</tr>
<tr>
<td>$B_2$ [-]</td>
<td>0.90</td>
<td>0.82</td>
<td>0.74</td>
<td>0.67</td>
<td>0.60</td>
<td>0.54</td>
<td>0.48</td>
<td>0.43</td>
<td>0.38</td>
</tr>
<tr>
<td>$B_3$ [-]</td>
<td>1.11</td>
<td>1.22</td>
<td>1.35</td>
<td>1.50</td>
<td>1.67</td>
<td>1.86</td>
<td>2.08</td>
<td>2.33</td>
<td>2.63</td>
</tr>
<tr>
<td>$B_4$ [-]</td>
<td>1.44</td>
<td>2.01</td>
<td>3.07</td>
<td>4.59</td>
<td>7.00</td>
<td>10.00</td>
<td>20.00</td>
<td>33.33</td>
<td>100.00</td>
</tr>
</tbody>
</table>

Figure 4: Schematic of the fractional-order controllable filter

is no commercialy available amplifier, which would provide such a high gain. The pair of the amplifiers ACA4 and ACA5 allows us to realized at least orders 0.5 and 0.6 (gain $B_4 = B_{ACA4} \cdot B_{ACA5}$).

4. FRACTIONAL-ORDER FREQUENCY FILTER

This section shows the application of the proposed fractional-order integrator in frequency filter. The filter design from [5] was used. It is a 3rd-order Butterworth filter in FLF topology too, which consists of three OTA-C integrators. The last OTA-C integrator in the cascade was replaced by the proposed fractional-order integrator. This adjustment created a frequency filter with electronically tunable order in range $\alpha = 2 \div 2.6$. The OTA-C integrators are created using multiple output OTA so there are available many outputs of both polarities. This allows both integrators to be connected (fractional order and 1st-order OTA-C) behind the second OTA-C section.

Characteristics equation of the filtering structure from Figure 4

$$CE_{FLF} = s^3 + s^2 \frac{g_{m1}}{C_1} + s \frac{g_{m1} g_{m2}}{C_1 C_2} + \frac{g_{m1} g_{m2} g_{m3}}{C_1 C_2 C_3} = s^3 b_3 + s^2 b_2 + s b_1 + b_0$$

was found by symbolic analysis in Snap software. Parameters of filter tolerance field (for the design of higher order filters) are: characteristics frequency $f_0 = 100$ kHz, maximal band-pass ripple $K_{max} = -3$ dB, band-stop frequency $f_{att} = 1$ MHz, band-stop attenuation $K_{min} = -59$ dB and Butterworth approximation. Values of the $g_m$ for 3rd-order filter are $g_{m1} = 314$ $\mu$S, $g_{m2} = 628$ $\mu$S and $g_{m3} = 1.26$ mS if all of the capacitors are $C = 1$ nF.

5. SIMULATIONS

Designed circuits (integrator and filter) were simulated in OrCAD Pspice. Transistor-level models of multiple output transconductance amplifier (MOTA), multiple output current follower (MO-CF) and adjustable current amplifier (ACA) in CMOS TSMC 0.18 $\mu$m technology were used [6].

Frequency characteristics (module and phase) of the proposed fractional-order integrator are in Figure 5a and 5b. Module characteristics of the fractional-order filter are in Figure 5c. Possibility of frequency tuning is shown on graph in Figure 5d. Dashed lines represent ideal simulation with the level 1 models of active elements and solid lines represent simulations with the transistor-level models.
6. CONCLUSION

Disadvantages of this proposed circuits are 1) impossibility to achieve orders higher than $\alpha = 0.6$ and 2) large number of active elements. The first mentioned disadvantage can be eliminated if ACA were implemented by an element capable of achieving high gains. Significant advantage is electronic controllability. It is possible to tune characteristics frequency of the filter and fractional order by a proportional change of all transconductances, current gains respectively. From the attached graphs it is obvious, that bandwidth of validity of the approximation is about 2.5 decades (approx 4 kHz ÷ 2 MHz).

REFERENCES


