A Survey of Non-conventional Techniques for Low-voltage Low-power Analog Circuit Design

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Abstract. *Designing integrated circuits able to work under low-voltage (LV) low-power (LP) condition is currently undergoing a very considerable boom. Reducing voltage supply and power consumption of integrated circuits is crucial factor since in general it ensures the device reliability, prevents overheating of the circuits and in particular prolongs the operation period for battery powered devices. Recently, non-conventional techniques i.e. bulk-driven (BD), floating-gate (FG) and quasi-floating-gate (QFG) techniques have been proposed as powerful ways to reduce the design complexity and push the voltage supply towards threshold voltage of the MOS transistors (MOST). Therefore, this paper presents the operation principle, the advantages and disadvantages of each of these techniques, enabling circuit designers to choose the proper design technique based on application requirements. As an example of application three operational transconductance amplifiers (OTA) based on these non-conventional techniques are presented, the voltage supply is only ±0.4 V and the power consumption is 23.5 μW. PSpice simulation results using the 0.18 μm CMOS technology from TSMC are included to verify the design functionality and correspondence with theory.*

Keywords

Low-voltage low-power analog circuit design, bulk-driven, floating-gate, quasi-floating-gate, OTA.

1. Introduction

Over the last decade reducing the voltage supply and minimizing the power consumption become the most important priority particularly for portable electronics and battery-powered implantable and wearable medical devices. The LV LP capability of portable electronics and battery-powered medical devices is essential demand since it enables increasing the battery lifetime and/or decreasing the size and weight of the devices by using battery with smaller size and weight which is demanded and important in modern devices [51].

Integrated circuit (IC) technologies trend toward reduction of the minimum feature size of MOS transistors, thus more electronic functions per unit area are achieved. However, increasing the device density of single IC means in its turn higher power dissipation and overheating. Hence it is very important to decrease the power dissipation of the integrated circuits to ensure device function and reliability [1].

Achievement of LV LP operation could be obtained either by technologies or by design techniques. The main advantages and disadvantages of the LV LP technologies and some of the most popular techniques are discussed in this paper; three main technologies are used for low-voltage low-power IC design:

- BiCMOS technology is advanced semiconductor technology, which integrates bipolar junction transistor and CMOS transistor in a single integrated circuit, and combines the advantages of both transistor types. This technology improves speed over purely bipolar technology, offers lower power dissipation over purely CMOS, high analog performance, smaller IC size and more reliable IC. However, this technology requires extra fabrication steps which increase the process cost [9].
- SOI (Silicon on insulator) technology: In this technology a layer of silicon dioxide is implanted below the surface by oxidation of Si or by oxygen implantation into Si. This implanted silicon dioxide is called buried oxide (BOX) which helps to reduce parasitic capacitances, and as a result improves the performances of the device. This technology offers ideal device isolation and smaller layout area, high switching speed and lower-power consumption. However, fabrication of this technology is more expensive featuring also higher self-heating because of poor thermal conductivity of the insulator [2].
- CMOS Technology: In CMOS (complementary metal oxide semiconductor) technology both kinds of transistors are used p-channel MOSFET and n-channel MOSFET in a complementary way on the same substrate. Besides, CMOS technology is used in the fabrication of conventional microchip, since it is less expensive than BiCMOS and SOI technologies and offers high performance, high density and low-power dissipation.

While the MOS transistor dimensions are shrunk, the power supply voltage is reduced to ensure the device reliability. However, the threshold voltage is not scaled down by the same ratio since devices with higher threshold voltage value have higher noise margin and smaller leakages [7]. This rather high value of the threshold voltage is the main limitation in LV LP analog circuit design. In order to overcome this restriction many techniques have been introduced based on CMOS technology. By utilizing these techniques, the threshold voltage is decreased or even removed. The most widely used techniques for LV LP analog circuits design are:

- Circuits with rail-to-rail operating range [49, 50].
- MOSTs operating in weak inversion [26].
- Level shifter techniques [7].
- Floating-gate approach [4, 7, 12, 13, 14, 15, 29, 33, 34, 35, 37, 39, 44].
- Quasi-floating-gate approach [16, 17, 18, 19, 20, 38, 41, 42, 43].
- Bulk-driven MOST [3, 5, 7, 8, 10, 11, 12, 21, 23, 24, 25, 27, 28, 31, 32, 36, 40].

However, the last three techniques are considered as non-conventional; they offer mainly design simplicity and capability to work under ultra LV LP condition with sufficient circuit's performances. Circuits based on these techniques are suitable for ultra LV LP application as battery-powered implantable and wearable medical devices.

Based on our survey a variety of recent publications describe various attractive implementations of the non-conventional techniques in LV LP applications such as operational amplifier [16, 28, 29], operational transconductance amplifier OTA [30-35], second generation current conveyor CCII [19, 36, 37, 38], class AB output stage for CMOS op-amps [39], transconductors [41-44], current differencing external transconductance amplifier (CDeTA) [40], differential-input buffered, external transconductance amplifier (DBeTA) [11], differential voltage current conveyor DVCC [27], and many others.

This paper is organized as follows. In Section 2, the non-conventional techniques based on bulk CMOS technology are presented, including principle of operation, small signal models and main advantages and disadvantages of each technique. Section 3 presents OTA design as an application example based on these techniques, simulation results and their evaluations are also included. Finally, Section 4 concludes the paper.

2. Non-conventional Techniques Based on Bulk CMOS Technology

2.1 Bulk-driven MOST (BD-MOST)

MOS transistor is a four terminals device namely: drain "D", gate "G", source "S" and bulk "B" as shown in Fig. 1(a) and in its cross section (b) which is presented with substrate terminal "Sub". Depending on the type of used technology (i.e. N-, P-well or twin-tub) the bulk terminal is normally connected either to positive/negative supply voltage for PMOS/NMOS transistor, respectively, or to the transistor source terminal. In other words, the bulk terminal is ignored and not used as a signal terminal and hence many applications are overlooked. The principle of the bulk-driven technique was firstly presented in [10].

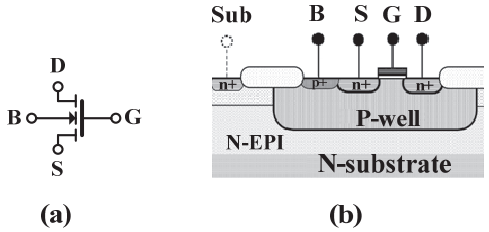

Fig. 1. Bulk-driven N-MOST: a) symbolic and b) cross-section.

To demonstrate the principle of operation of the bulk-driven technique in comparison with the conventional gate-driven MOST (GD-MOST) the common source amplifier as an example of application is shown in Fig. 2. In the bulk-driven technique the gate-source voltage must be set to a proper bias voltage V_{bias} to form an inversion layer under the gate oxide, permitting the operation in the conductance region.

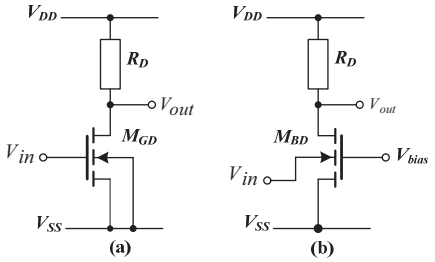

Fig. 2. Common source amplifier based on a) gate-driven NMOST and b) bulk-driven NMOST.

Unlike the conventional gate-driven technique the input signal in the bulk-driven technique is applied to the bulk terminal $V_{in} = V_{bs}$ rather than the gate terminal. The operation of the BD-MOST is much like a JFET where the channel width is constant as long as the input and bias voltages don't change.

Fig. 3 shows the drain current versus bulk-source voltage of BD-NMOST in Fig. 2(b) with three different dimensions, it is clear that by scaling up the transistor dimensions W/L the transconductance steadily increases, as it is discussed later. As well the relationship between drain current and gate-source voltage of the gate-driven NMOST in Fig. 2(a) is shown in Fig. 3. The simulation has been done with the following characteristics: V_{DD} = 0.8 V, V_{ss} = 0 V, V_{bias} = 0.5 V, R_D = 15 kΩ, W/L = (5µ/0.5µ, 10µ/0.5µ and 20µ/0.5µ) for BD-NMOST and W/L = 5µ/0.5µ for GD-NMOST, 0.18 µm CMOS process. It is evident from Fig. 3 that the drain current of the GD-NMOST appears when the input voltage exceeds the

threshold voltage value ($V_T \approx 400$ mV); while in BD-NMOST the threshold voltage has been removed. Furthermore, the BD-NMOST operates under negative input voltage and has a wide operating range stretches to slightly positive input voltage. Conversely, the BD-PMOST operates under positive, zero and slightly negative input voltage. Hence BD-MOST is a very attractive technique in rail-to-rail applications [21], [11].

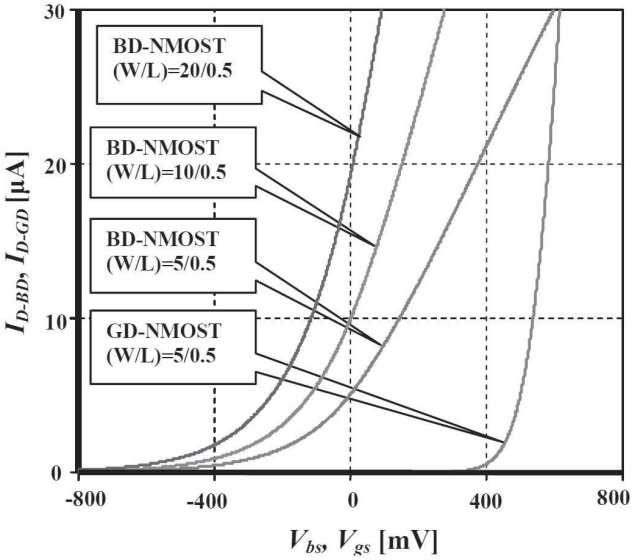

Fig. 3. Drain currents versus gate-source voltage of GD-MOST and bulk-source voltage of BD-MOST with various *W/L* ratios.

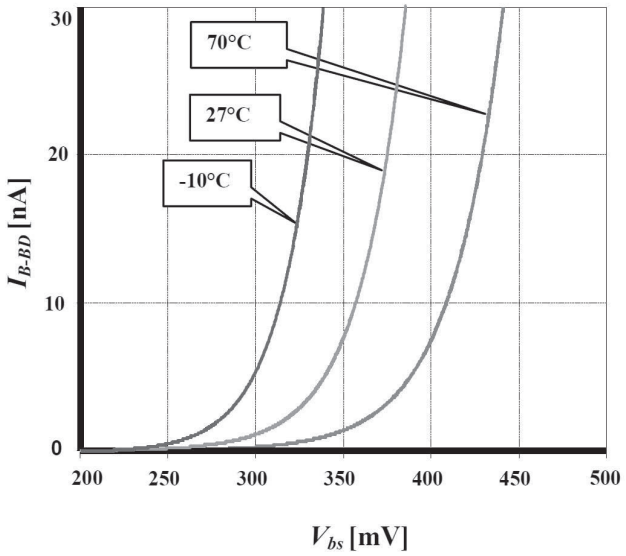

Fig. 4. Bulk current versus bulk-source voltage of the BD-NMOST for temperatures of -10, 27 and 70°C.

However, the operating range of the BD-MOST must be limited to avoid latch up problem, since the bulk-source voltage must be smaller than the turn-on voltage of the bulk-source PN junction diode [11], which causes a remarkable current through the bulk terminal and the transistor is latch up. It is relatively safe to use BD-MOST at low-voltage applications more than other applications. Fig. 4 shows the current through bulk terminal versus the bulk-source voltage for various temperatures of -10, 27 and 70°C.

The cross section of BD-NMOST is shown in Fig. 1(b) in the aim to ease understanding the small signal model of the common source BD amplifier and the influence of the parasitic capacitances on BD-MOST's parameters, as it is discussed below.

Fig. 5(a) and (b) show the small signal equivalent circuit at high frequencies of the common source amplifier based on GD-NMOST and BD-NMOST, respectively. The capacitances C_{bd}, C_{bs}, C_{bsub} are bulk-drain, bulk-source and bulk-substrate parasitic capacitance, respectively. These parasitic capacitances are a result of well and substrate structure of the transistor.

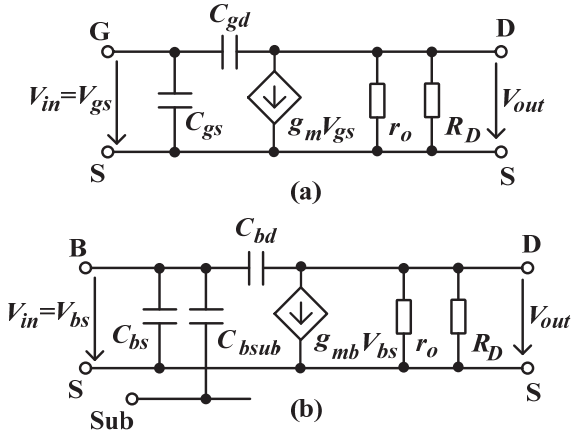

Fig. 5. Small signal equivalent circuit of the common source amplifier based on: a) Gate-driven NMOST, b) Bulk-driven NMOST.

The transconductance of GD-MOST which operates in strong inversion is given by:

$$g_m = K\frac{W}{L}(v_{gs} - V_T) \tag{1}$$

where *W, L* are channel width and channel length, respectively. V_{gs} is gate-source voltage, V_T is the threshold voltage, K is the current gain factor of the used process. Nevertheless the transconductance of BD- MOST is [11]:

$$g_{mb} = \frac{\gamma}{2\sqrt{|2\varphi_F - \mathbf{V}_{BS}|}} g_m = \frac{C_{BC}}{C_{GC}} g_m \approx (0.2 \to 0.4) g_m \tag{2}$$

where C_{BC} is the total bulk-channel capacitance, C_{GC} is the total gate channel capacitance, γ is the body effect coefficient, and φ_F the Fermi potential, V_{BS} is the quiescent bulk-source voltage. From previous equation it is clear that g_{mb} is smaller than g_m, the same result understandable from Fig. 3. The relatively small transconductance of the BD-MOST is considered as one of its drawbacks in comparison with GD-MOST, since high value of transconductance is widely desired in analog circuit design. However, smaller transconductance is attractive in several applications such as biomedical applications. A practical example is the G_m-C filter [22, 33, 34, 48], where the positions of poles are determined by the ratio g_m/C, because biological signals

frequencies are substantially small, the poles must be at very low values and this can be achieved either by increasing the capacitance value or decreasing the transconductance. Factually decreasing transconductance is more practical; smaller transconductance was introduced in a lot of works such as in [45, 46]. Nevertheless the BD-MOST's transconductance can be increased by increasing the W\L ratio as it was discussed previously.

To determine the frequency performance of a BD-MOST, transition frequency f_T must be calculated. This frequency is defined as the frequency where the magnitude of the short circuit, common-source current gain falls to unity [47]. To calculate the transition frequency, consider the ac circuit of Fig. 6(a) and the small signal equivalent of Fig. 6(b), whereas the parasitic capacitances have been described in Fig. 5.

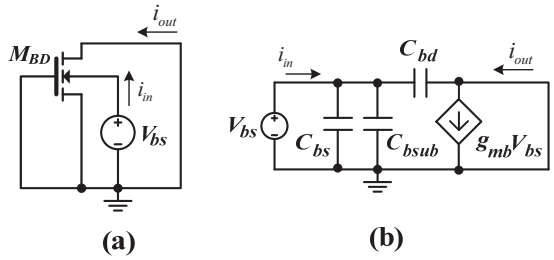

Fig. 6. Circuits for calculating transition frequency of BD-MOST: a) ac schematic, b) small signal equivalent circuit.

The small signal input current i_{in} :

$$i_{in} = s(C_{bs} + C_{bsub} + C_{bd})v_{bs} . \tag{3}$$

If the current through C_{bd} is neglected then i_{out}:

$$i_{out} \approx g_{mb}v_{bs} . \tag{4}$$

From (3) and (4) we can find the current gain:

$$\frac{i_{out}}{i_{in}} \approx \frac{g_{mb}}{s(C_{bs} + C_{bsub} + C_{bd})} . \tag{5}$$

Put $s = j\omega$ to find the frequency response, then:

$$\frac{i_{out}}{i_{in}} \approx \frac{g_{mb}}{j\omega(C_{bs} + C_{bsub} + C_{bd})} . \tag{6}$$

The magnitude of the small signal current gain is unity when:

$$\omega = \omega_T = \frac{g_{mb}}{C_{bs} + C_{bsub} + C_{bd}} . \tag{7}$$

Then the transition frequency of the BD-MOST is:

$$f_{T_b} = \frac{1}{2\pi}\omega_T = \frac{1}{2\pi}\frac{g_{mb}}{C_{bs} + C_{bsub} + C_{bd}} . \tag{8}$$

Assume that $(C_{bs} + C_{bsub})$ is much greater than C_{bd}, that gives:

$$f_{T_b} = \frac{g_{mb}}{2\pi(C_{bs} + C_{bsub})} \approx (0.3 \to 0.5)f_T \tag{9}$$

whereas f_T is transition frequency of GD-MOST which can be calculated by the same steps:

$$f_T = \frac{g_m}{2\pi C_{gs}} . \tag{10}$$

From (9) it is obvious that the transition frequency of BD-MOST is smaller than the transition frequency of GD-MOST, since the transition frequency is proportional to the transconductance, as well as the effect of the parasitic capacitances.

The input referred noise power spectral density of GD-MOST is expressed by:

$$v^2_{noise,GD} = \frac{i^2_{ni}}{g^2_m} \tag{11}$$

where i^2_{ni} is the total drain current generated by noise sources and its unit is A^2. The input referred noise power spectral density of BD-MOST can be expressed by [11]:

$$v^2_{noise,BD} = \left(\frac{g_m}{g_{mb}}\right)^2 v^2_{noise,GD} . \tag{12}$$

BD-MOST suffer from higher referred noise as it is clear from (12), since g_{mb} inherently smaller than g_m.

BD-MOST and GD-MOST have identical output resistance r_o Fig. 5:

$$r_o = \frac{1}{g_o} = \frac{1}{\lambda I_{DSsat}} . \tag{13}$$

Many advantages can be obtained by using the BD-MOST in analog circuit design:

- The threshold voltage requirements are removed.
- A wider input common mode range under negative, zero and slightly positive input voltage (BD-NMOST).
- Suitable for rail-to-rail applications.
- Can be modeled using the conventional MOS transistor.
- Can process DC and AC over the FG-MOST and QFG-MOST which process AC only, as it is discussed below.

In the other hand some drawbacks come with the BD-MOST technique:

- Smaller transconductance and transition frequency in comparison with GD-MOST.
- Higher input referred noise than conventional GD-MOST.
- In the applications where both PMOS and NMOS are needed to use as bulk-driven transistors, twin well process is needed, that can be achieved at the expense of higher cost process and larger chip area.
- Analog circuits with tight matching between BD-MOSTs are difficult to be fabricated, since BD-

MOSTs are fabricated in differential wells to have isolated bulk.

- Latch-up maybe occurs.

2.2 Floating-gate MOST (FG-MOST)

The first well-known application of the FG-MOST was to store data in digital EEPROMs, EPROMs and flash memories [37]. Recently, many new and important LV LP applications were designed using the floating gate technique [13, 14, 15, 29, 33, 34, 35, 37, 39, 44], since the threshold voltage is tunable as it is discussed below. The symbol of the FG-MOST with two control gates is shown in Fig. 7(a), its equivalent circuit in (b), its layout in (c) and the cross-sectional views in (d). The gate in FG-MOST is fabricated using the poly1 layer and is left floating, since it is surrounded by insulator layers (SiO_2). Two or more control gates (G_{in}, G_{bias}) are formed using the second poly layer and capacitively coupled to the floating gate.

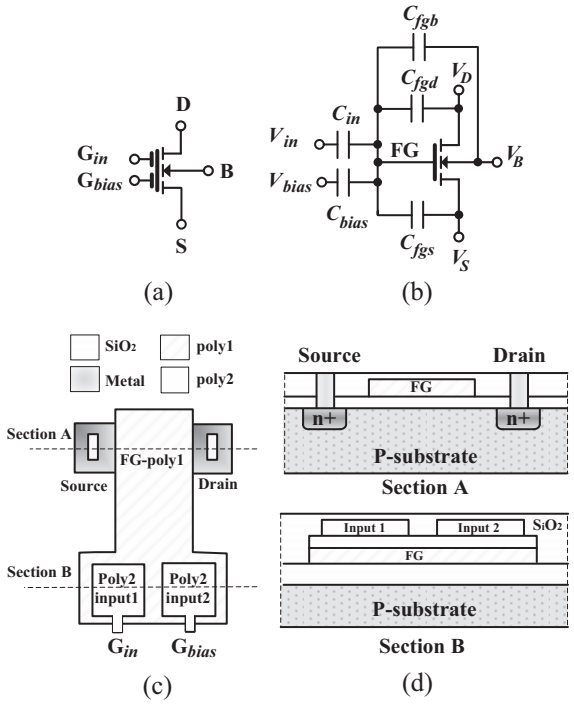

Fig. 7. Two-input floating gate NMOST: a) symbolic, b) equivalent circuit, c) layout and d) cross-sectional views.

The floating gate voltage is given by:

$$V_{FG} = \frac{C_{in}V_{in} + C_{bias}V_{bias} + C_{fgd}V_D + C_{fgs}V_S + C_{fgb}V_B + Q_{FG}}{C_{Total}} \quad (14)$$

where the capacitances C_{in} and C_{bias} are the control gates capacitances at which the input signal V_{in} and the bias voltage V_{bias} is applied, respectively. $C_{fgb,}$ C_{fgd} and C_{fgs} denote the floating gate-bulk, -drain and -source capacitances. C_{Total} is the sum of these capacitances:

$$C_{Total} = C_{in} + C_{bias} + C_{fgd} + C_{fgs} + C_{fgb} \quad (15)$$

and Q_{FG} is the initial charge trapped at the floating gate during fabrication; Since floating gate is surrounded by high-quality isolation any electrical charge injected onto this gate is retained for several years, causing DC offsets. However, this charge can be eliminated by several ways such as cleaning with ultraviolet (UV) light, hot electron injection [4, 7, 12], Fowler-Nordheim (FN) tunneling [4, 12], forcing an initial condition with a switch [4] or by fabrication process solution which is based on a novel layout technique that takes advantage of the fabrication process itself [56].

To demonstrate the operation principle of the FG-MOST, a common source amplifier based on the FG-NMOST with two control gates is shown in Fig. 8(a), its small signal equivalent circuit is depicted in Fig. 8(b). As it is clarified in Fig. 8, a proper bias voltage V_{bias} is applied at one of the control gates G_{bias} through large value capacitance, which is able to shift the threshold voltage. The input signal is applied at the second control gate G_{in} and modulates the inversion layer, thus controls the drain current. The threshold voltage of the FG-MOST is expressed by:

$$V_{T_{FG}} = \frac{V_T - V_{bias}K_2}{K_1} \quad (16)$$

where V_T is the threshold voltage of a conventional GD-MOST, K_1 and K_2 are given by:

$$K_1 = \frac{C_{in}}{C_{Total}}, \qquad K_2 = \frac{C_{bias}}{C_{Total}}. \quad (17)$$

It is obvious from (16) that the threshold voltage of FG-MOST is smaller than the threshold voltage of conventional GD-MOST; it can be even removed with proper values of the bias voltage, K_1 and K_2.

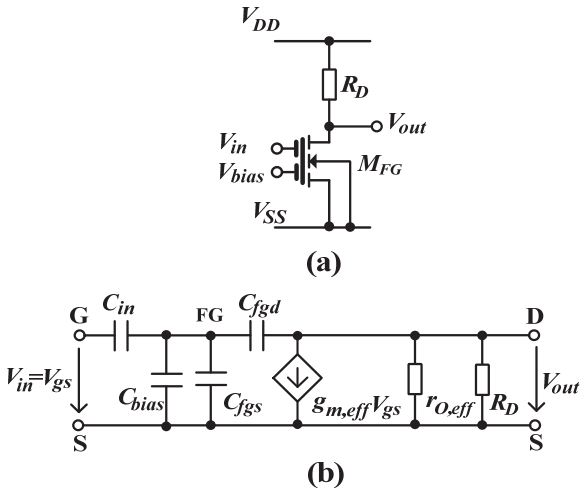

Fig. 8. Floating-gate MOST: a) common source amplifier and b) small signal model equivalent circuit.

For example, assume the common source amplifier in Fig. 8(a) with a FG-NMOST has $W/L = 10/0.5\mu m/\mu m$, $R_D = 15\ k\Omega$, $C_{in} = C_{bias} = 0.1$ pF, $C_{fgs} = C_{fgd} = 0.8$ fF, thus $K_1 = K_2 \approx 0.5$ and the threshold voltage is removed for $V_{bias} = 0.7$ V. The same result is illustrated in Fig. 9 where

the drain current of the previous FG-NMOST is compared with the drain current of the GD-NMOST in Fig. 2(a). Whereas the GD-NMOST has $W/L = 10/0.5\mu m/\mu m$ and $R_D = 15\ k\Omega$. From Fig. 9 it is obvious that the threshold voltage requirement is removed from the signal path using FG-MOST.

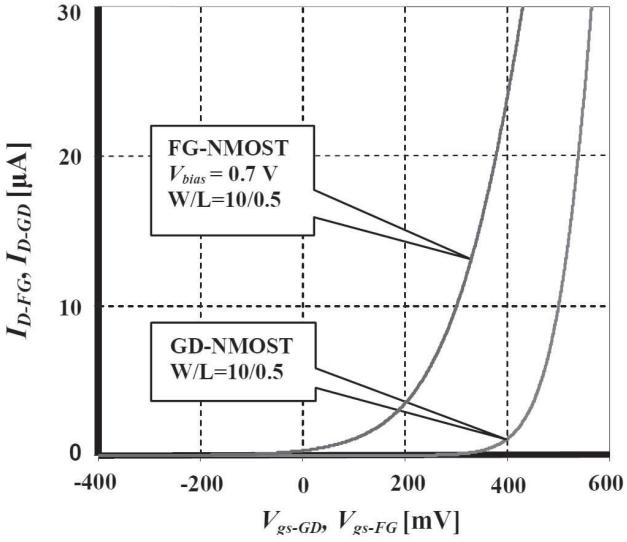

Fig. 9. Drain currents versus gate-source voltages of FG-MOST and GD-MOST.

Actually, the designers face a problem with simulation of the FG-MOST, because the simulators don't accept a floating node. Many solutions have been proposed to overcome the simulation problem and are presented in [4], [52-55]. The most popular solution is to connect extremely high resistor in parallel with the floating gate input capacitors [53]; this method was used to simulate FG-MOST in this paper.

The effective transconductance of combined structure of the FG-MOST is given by:

$$g_{m,eff} = K_1 g_m = \frac{C_{in}}{C_{Total}} g_m \ . \tag{18}$$

It's clear from this equation that the effective transconductance $g_{m,eff}$ is smaller than the gate transconductance g_m. The effective transconductance can be increased proportionally with g_m and C_{in}/C_{Total} ratio. That can be done at the expense of increasing the power consumption and the occupied chip area.

To calculate transition frequency, let's consider the ac circuit and its small signal equivalent circuit in Fig. 10:

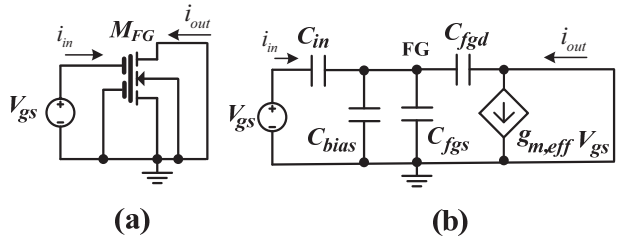

Fig. 10. Circuit for calculating transition frequency of FG-MOST: a) ac schematic, b) small signal equivalent circuit.

The small signal input current is:

$$i_{in} = s\left[\frac{C_{in}(C_{bias} + C_{fgs} + C_{fgd})}{C_{Total}}\right] v_{gs} \ . \tag{19}$$

If the current through C_{fgd} is neglected then:

$$i_{out} \approx g_{m,eff} v_{gs} \ . \tag{20}$$

From (19) and (20), the current gain can be written:

$$\frac{i_{out}}{i_{in}} = \frac{g_{m,eff}}{s\left[\frac{C_{in}(C_{bias} + C_{fgs} + C_{fgd})}{C_{Total}}\right]} \ . \tag{21}$$

By following the same steps that were done to find transition frequency of BD-MOST at the previous subsection, the transition frequency equation of FG-MOST will be given by:

$$f_{T_{FG}} = \frac{g_{m.eff}}{2\pi\left[\frac{C_{in}(C_{bias} + C_{fgs} + C_{fgd})}{C_{Total}}\right]} \ . \tag{22}$$

Assuming C_{fgs} is much greater than C_{fgd} and substituting the effective transconductance value from (18), then:

$$f_{T_{FG}} = \frac{g_m}{2\pi(C_{bias} + C_{fgs})} \ . \tag{23}$$

It is clear that the transition frequency of FG-MOST is smaller than the transition frequency of GD-MOST; hence FG-MOST has smaller bandwidth than GD-MOST.

The relationship between the input referred noise power spectral density of FG-MOST and GD-MOST is given by [4]:

$$v^2_{noise,FG} = \left(\frac{C_{Total}}{C_{in}}\right)^2 v^2_{noise,GD} \ . \tag{24}$$

It is evident that the input referred noise increases at the effective input of the FG-MOST.

The effective output conductance of the FG-MOST is larger than the output conductance of the GD-MOST, because of DC and AC feedback from drain to floating gate through C_{fgd} [7]. The output conductance of FG-MOST is given by [4]:

$$g_{ds.eff} = \frac{1}{r_{o,eff}} = \frac{C_{fgd}}{C_{Total}} g_m + g_{ds} \tag{25}$$

where g_{ds} is output conductance of GD-MOST transistor operates at the same biasing conditions.

Many advantages can be obtained using FG-MOST technique, such as:

- Possibility of multi-input terminals.
- Threshold voltage can be shifted according to the application's requirements.
- Can be used in ultra-low power ultra-low voltage applications.

- Can be fabricated in any MOS technology, although for better performance double poly technology is recommended.

There are some disadvantages coming with this technique:

- Larger area is occupied on the chip over the conventional GD-MOST, since the bias and input capacitances have relatively high values [42, 19].
- Uncertain amount of cumulative initial charge in the floating gate.
- Reduction of the effective transconductance and output impedance in comparison with the conventional GD-MOST.
- Smaller transition frequency, hence smaller bandwidth than the GD-MOST.
- Shortage of simulation models, as well the simulators don't accept the floating node.

2.3 Quasi-Floating-gate MOST (QFG-MOST)

Many recent publications describe interesting and important implementations of the QFG-MOST in LV LP applications [16, 17, 18, 19, 20, 38, 41, 42, 43]. The QFG-MOST appears as a developed version of the FG-MOST to overcome some of its drawbacks. It has been discussed previously that the relatively high bias capacitance value of the FG-MOST leads to an increase in the silicon area and a reduction of the effective transconductance and GBW. Besides, FG-MOST has uncertain residual charge trapped at the floating gate. Using the QFG-MOST, the occupied chip area is minimized and the initial charge is no longer an issue [4]. Since the floating gate is tied through a large value resistor to a proper bias voltage, depending on the transistor type. Practically, a leakage resistance R_{lkg} of a reverse biased P-N junction of a diode connected MOS transistor M_R is implemented rather than a typical resistor, as it is obvious in Fig. 11 which shows the symbolic of the QFG-MOST (a), its equivalent circuit (b) and layout (c) with single input terminal.

QFG-MOST may have a multiple input terminals like the FG-MOST. Besides, it can be fabricated in any MOS technology, nevertheless, the double poly technology is recommended to obtain better results. As it is shown in Fig. 11 the input terminal is capacitively connected to the floating gate as FG-MOST case. The quasi-floating gate DC voltage value is set to V_{bias} independently of the DC component of the input voltage while the quasi-floating gate AC voltage can be expressed by [19]:

$$V_{QFG} = \frac{sR_{lkg}}{1+sR_{lkg}C_{Total}}(C_{in}V_{in} + C_{fgd}V_D + C_{fgs}V_S + C_{fgb}V_B) \quad (26)$$

where C_{Total} is:

$$C_{Total} = C_{in} + C_{fgs} + C_{fgd} + C_{fgb} + C_{gd} \ . \quad (27)$$

The capacitors C_{in}, C_{fgs} , C_{fgb} and C_{fgd} are input, floating gate-source, -bulk and -drain capacitor, respectively. C_{gd} is the gate-drain capacitor of the diode connected transistor M_R. Fig. 12 shows the common source amplifier based on QFG-MOST in (a) and its small signal equivalent circuit in (b), where the previous capacitors are shown, however the floating gate-bulk capacitance is ignored, because it has no influence on signal path. The operation principle of the QFG-MOST is similar to the FG-MOST.

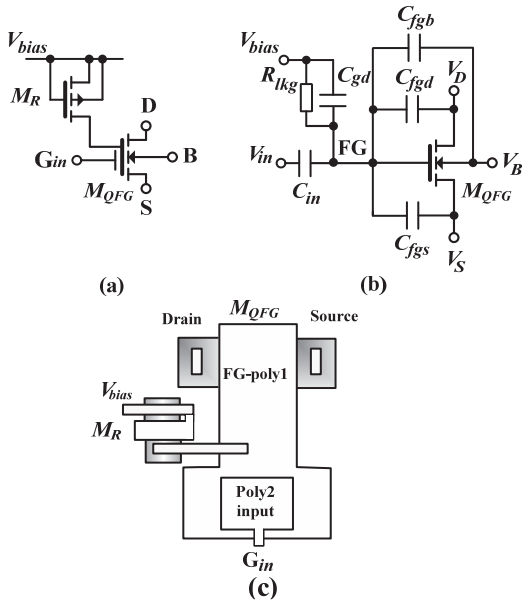

Fig. 11. One-input Quasi-Floating gate NMOST: a) symbolic, b) its equivalent circuit and c) layout.

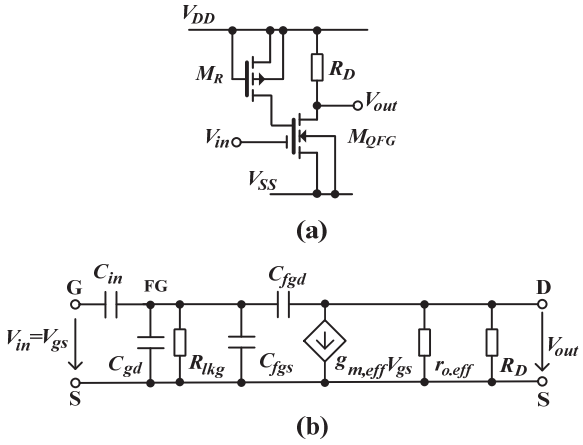

Fig. 12. Quasi-Floating gate MOST: a) common source amplifier with single input terminal, b) small signal model equivalent of (a).

The drain current of the common source amplifier in Fig. 12 versus its gate-source voltage, in comparison with the drain current of the common source amplifier in Fig. 2(a) is shown in Fig. 13. It is notable that the threshold voltage requirements have been removed from the signal way using the QFG-MOST.

Attention must be attracted to the floating gate voltage V_{QFG} level; this voltage should be at the range where the p-n junction of the diode connected transistor M_R is still reverse biased [4].

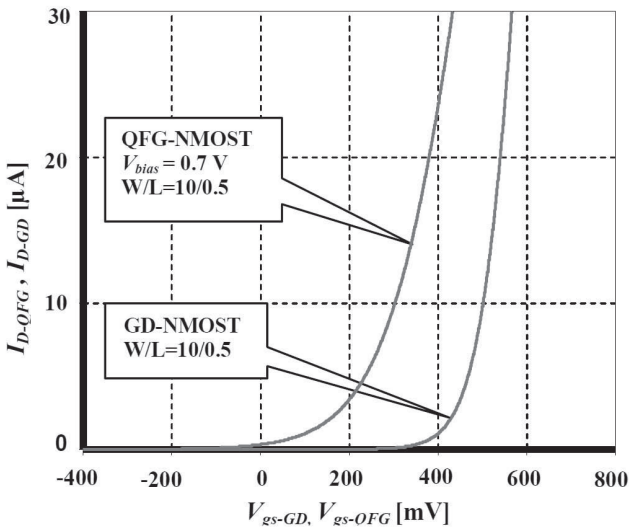

Fig. 13. Drain currents versus gate-source voltages of QFG-MOST and GD-MOST.

The effective transconductance of the QFG-MOST is given by:

$$g_{m,eff} = \frac{C_{in}}{C_{Total}} g_m \tag{28}$$

where g_m is the transconductance seen from the floating gate. The effective transconductance of QFG-MOST is larger than the effective transconductance of FG-MOST, however still smaller than the transconductance of conventional GD-MOST as it is obvious from Fig. 13.

It is notable from Fig. 12(b) that the input is high pass filter; its cut-off frequency is given by:

$$f_{cut,off} = \frac{1}{2\pi R_{lkg} C_{Total}} . \tag{29}$$

The cut-off frequency should be extremely small for properly operation at the applications where the low frequencies are needed. Hence the value of R_{lkg} must be large enough in the order of Giga ohms.

To calculate transition frequency of QFG-MOST, let's consider the ac circuit and its small signal equivalent circuit in Fig. 14:

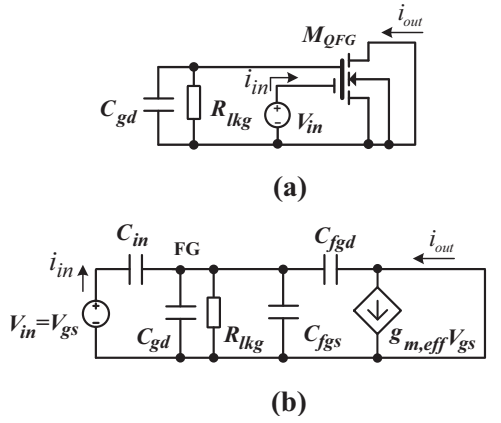

Fig. 14. Circuit to calculate transition frequency of QFG-MOST: a) ac schematic, b) small signal equivalent circuit.

Assuming that R_{lkg} is extremely large, then the small signal input current is:

$$i_{in} = s\left[\frac{C_{in}(C_{gd} + C_{fgs} + C_{fgd})}{C_{Total}}\right] v_{gs} . \tag{30}$$

If the current through C_{fgd} is neglected then:

$$i_{out} \approx g_{m,eff} v_{gs} . \tag{31}$$

From (30) and (31) the current gain can be found:

$$\frac{i_{out}}{i_{in}} = \frac{g_{m,eff}}{s\left[\frac{C_{in}(C_{gd} + C_{fgs} + C_{fgd})}{C_{Total}}\right]} . \tag{32}$$

By following the same steps that were done previously, then the transition frequency equation of QFG-MOST is:

$$f_{T_{QFG}} = \frac{g_{m.eff}}{2\pi\left[\frac{C_{in}(C_{gd} + C_{fgs} + C_{fgd})}{C_{Total}}\right]} . \tag{33}$$

Assume that C_{fgs} is much greater than C_{fgd} and compensate the effective transconductance from (28), then the transition frequency can be expressed by:

$$f_{T_{QFG}} = \frac{g_m}{2\pi(C_{fgs} + C_{gd})} . \tag{34}$$

The input referred noise of the QFG-MOST is similar in form to that of FG-MOST, since the input signal path in both MOSTs is the same, then:

$$v^2_{noise,QFG} = \left(\frac{C_{Total}}{C_{in}}\right)^2 v^2_{noise,GD} . \tag{35}$$

As it is clear QFG-MOST suffer from higher input referred noise than GD-MOST, however, the input referred noise of QFG-MOST is smaller than it of FG-MOST, since $C_{Total,QFG} < C_{Total,FG}$.

The effective output conductance of QFG-MOST is greater than the effective output conductance of FG-MOST, and it is given by the same form of the FG-MOST conductance:

$$g_{ds.eff} = \frac{C_{fgd}}{C_{Total}} g_m + g_{ds} . \tag{36}$$

The QFG-MOST has almost the same advantages as the FG-MOST, besides:

- There is no initial charge trapped at the floating gate.
- Smaller occupied chip area than FG-MOST.
- The effective transconductance and transition frequency are relatively higher than the effective transconductance and transition frequency of FG-MOST, but they are still smaller than the transconductance and transition frequency of the conventional GD-MOST.

Some drawbacks come with QFG-MOST techniques, such as:

- Greater effective output conductance than the effective output conductance of FG-MOST and the output conductance of GD-MOST.
- Floating gate voltage must not exceed the cut-in voltage of the p-n junction of the diode connected transistor M_R.

3. Example of Application (Operational Transconductance Amplifier OTA)

To illustrate the implementation principle of non-conventional techniques in analog circuit design, these techniques are used in this section to build three LV LP Miller OTAs with the same voltage supply, power consumption and transistors aspect ratios. However, the differential pair transistors are different i.e. BD-PMOST, FG-PMOST and QFG-PMOST to clarify the performances of each technique. A comparison study between the most important characteristics of the three OTAs is presented as well.

Since operational transconductance amplifier is an important block used in many applications and structures, it has been chosen as an example of non-conventional techniques application. Actually, Miller OTA composite of cascade of two stages, first stage is a differential amplifier with PMOS input transistors (M_1, M_2), see Fig. 15, and the current mirror (M_3, M_4) acting as an active load. The second stage is a simple common source amplifier with transistor M_6 acting as driver and M_7 as an active load, its output connected to its input through the compensation capacitor C_c and resistor R_c, this capacitor acting as Miller capacitance, without it the circuit is not stable [6]. The bias current I_b and transistors M_8, M_5, M_7 provide the bias currents needed for the first and second stage of OTAs. Utilizing the non-conventional techniques as input devices of the differential amplifier at the first stage, LV LP OTAs can be achieved.

Three Miller OTAs based on non-conventional techniques are depicted in Fig. 15, bulk-driven OTA in (a), floating-gate OTA in (b) and quasi-floating-gate OTA in (c). In the bulk-driven OTA, the gate terminals of BD-PMOSTs (M_1, M_2) are tied to V_{ss} to provide sufficient bias voltage, the input signals are applied at bulk terminals Fig. 15(a). Floating-gate OTA is designed by implementation of two FG-PMOSTs (M_1, M_2) with two control gates. The bias voltage V_{ss} is applied at one of control gates of each transistor. The input signals are applied at the second control gate as it is shown in Fig. 15(b). The third OTA has two QFG-PMOSTs with single input terminal as input devices; the floating gates of the QFG-PMOSTs are tied through reversed-biased diode connected transistors (M_9 and M_{10}) to V_{ss}, while input signals applied to the input terminals as shown in Fig. 15(c).

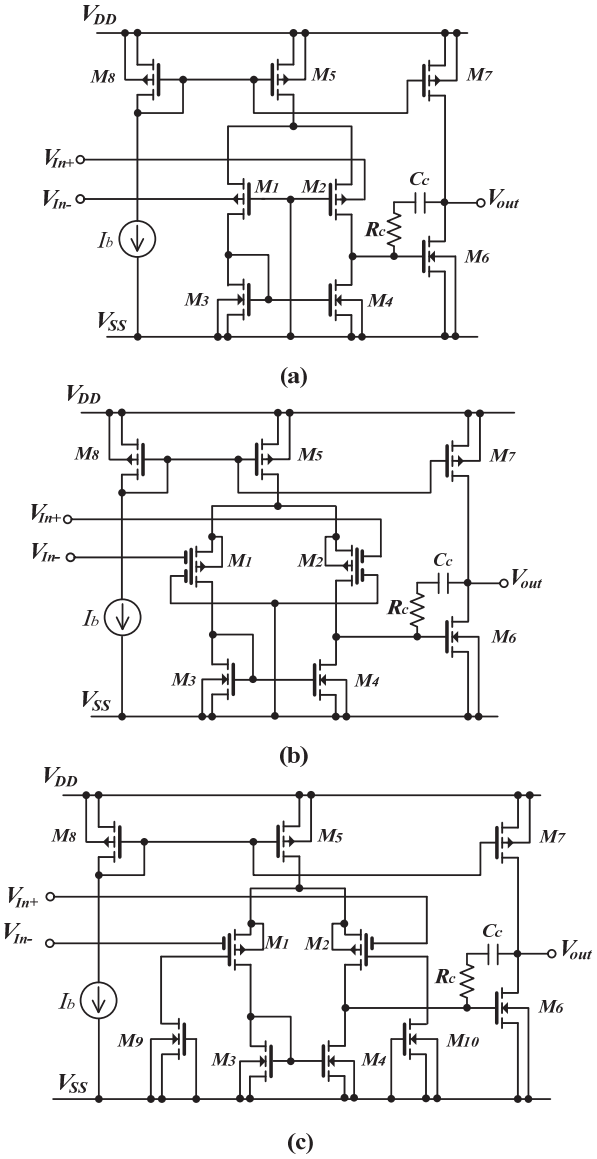

Fig. 15. LV LP Miller OTA based on: a) BD-MOST, b) FG-MOST and c) QFG-MOST.

The simulation results of the described OTAs are summarized in Tab. 1, and the transistors aspect ratios are listed in Tab. 2. It is notable that the proposed OTAs offer high performance LP LV operation, where the power consumption is reduced to about 23.5 μW and the power supply is ± 0.4 V. Besides relatively high output impedance, wide input voltage range and phase margin higher than 60º are obtained, hence the proposed OTAs ensure stability. In Fig. 16 the frequency responses for each OTA are depicted; as well the GBW, the gain and the phase values at the unity gain frequency are shown. The output signals of a voltage follower connected OTA are shown in Fig. 17, the input sine wave has 100 mV amplitude and 10 kHz frequency. By comparing the basic parameters from Tab. 1, it is evident that the best performances are offered by QFG-OTA then FG-OTA. However, due to the input and bias capacitances the chip area of the FG and QFG-OTAs is larger than the BD-OTA.

Characteristics	Bulk-driven OTA	Floating-gate OTA	Quasi-floating-gate OTA
Power consumption [µW]	23.5	23.5	23.5
Phase margin [º]	93	87	84
Output impedance [kΩ]	255.9	255.7	255.7
Offset voltage [mV]	0.7	0.44	0.92
Dynamic range [mV]	-100 to 400	-300 to 395	-237 to 400
CMRR [dB]	42.4	50.29	49.8
GBW [MHz]	1.5	3.84	7.47
Gain [dB]	24	35.94	41.5
Slew rate [V/µs]	0.28	0.54	0.76
Measurement conditions: V_{DD}= 0.4V, V_{SS}= -0.4V, C_c=C_L=1 pF, C_{in}=C_{bias}=1 pF, R_c=7kΩ, I_b=6 µA			

Tab. 1. The simulation results of three LV LP Miller OTAs.

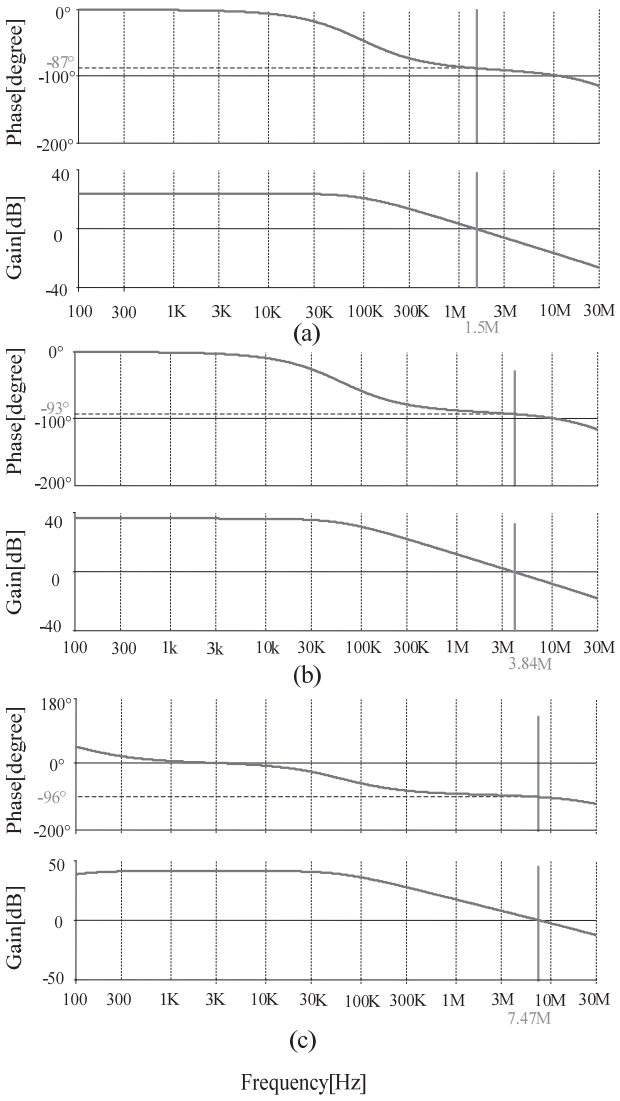

Fig. 16. Frequency response of the OTA based on: a) Bulk-driven transistor, b) floating-gate transistor, c) quasi-floating gate transistor.

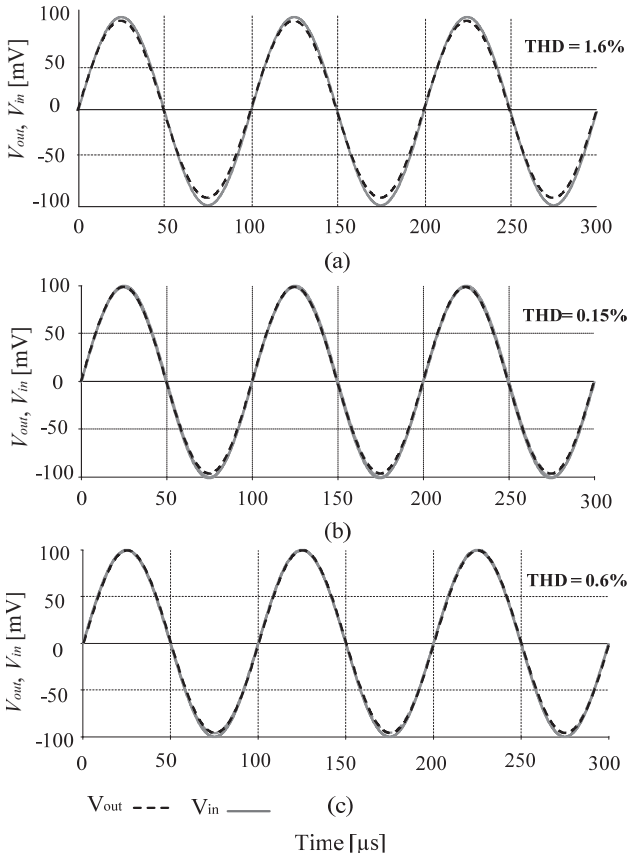

Fig. 17. Output voltage and input voltage of the OTA based on: a) Bulk-driven transistor, b) floating-gate transistor, and c) quasi-floating gate transistor.

Transistor	W/L [µm/µm]
M_1, M_2	**12/0.6**
M_3, M_4	**12/0.6**
M_5, M_7	**8/0.6**
M_6	**24.9/0.6**
M_8	**4/0.6**
M_9, M_{10}	**4/1**

Tab. 2. The transistors aspect ratios of the OTAs in Fig. 15.

	Threshold voltage	Transconductance	Transition frequency	Output conductance	Input referred noise
GD-MOST	$V_T = V_{T0} \pm \gamma\left(\sqrt{\lvert 2\phi_F - v_{bs}\rvert} - \sqrt{\lvert 2\phi_F\rvert}\right)$	$g_m = K\frac{W}{L}(v_{gs} - V_T)$	$f_T = \frac{g_m}{2\pi C_{gs}}$	$g_{ds} = \lambda I_{ds}$	$v^2_{noise,GD} = \frac{i^2_{ni}}{g^2_m}$
BD-MOST	removed	$g_{mb} = \frac{C_{bs}}{C_{ox}} g_m$ $g_{mb} \approx (0.2 \to 0.4) g_m$	$f_{Tb} = \frac{g_{mb}}{2\pi(C_{bs} + C_{bsub})}$	$g_{ds} = \lambda I_{ds}$	$v^2_{noise,BD} = \left(\frac{g_m}{g_{mb}}\right)^2 v^2_{noise,GD}$ $v^2_{noise,BD} \approx (6 \to 25) v^2_{noise,GD}$
FG-MOST	$V_{T,FG} = \frac{V_T - V_{bias} k_2}{k_1}$ reduced or removed	$g_{m,eff} = \frac{C_{in}}{C_{Total}} g_m$ $g_{m,eff} \approx (0.5 \to 0.6) g_m$	$f_{T_{FG}} = \frac{g_m}{2\pi(C_{bias} + C_{fgs})}$	$g_{ds,eff} = \frac{C_{gd}}{C_{Total}} g_m + g_{ds}$	$v^2_{noise,FG} = \left(\frac{C_{Total}}{C_{in}}\right)^2 v^2_{noise,GD}$ $v^2_{noise,FG} \approx (2.7 \to 4) v^2_{noise,GD}$
QFG-MOST	$V_{T,FG} = \frac{V_T - V_{bias} k_2}{k_1}$ reduced or removed	$g_{m,eff} = \frac{C_{in}}{C_{Total}} g_m$ $g_{m,eff} \approx (0.7 \to 0.9) g_m$	$f_{T_{QFG}} = \frac{g_m}{2\pi(C_{fgs} + C_{gd})}$	$g_{ds,eff} = \frac{C_{gd}}{C_{Total}} g_m + g_{ds}$	$v^2_{noise,QFG} = \left(\frac{C_{Total}}{C_{in}}\right)^2 v^2_{noise,GD}$ $v^2_{noise,QFG} \approx (1.2 \to 2)\, v^2_{noise,GD}$

Tab. 3. Main parameters summary of non-conventional techniques.

4. Conclusions

This paper presents the principle of non-conventional techniques for LV LP analog circuit design; the main parameters of non-conventional techniques were clarified and also summarized in Tab. 3 to make them reachable. Furthermore, their advantages and disadvantages were listed, thus one can use appropriate technique for intended analog circuit design. In spite of that the non-conventional techniques offer design simplicity with high performance, low voltage and low power operation, some drawbacks come with these techniques, mainly, the reduction of the gain bandwidth, transconductance and the output impedance (in FG-MOST and QFG-MOST case).

Finally, to demonstrate the implementation way, OTAs based on non-conventional techniques are presented. The simulation results of LV LP OTAs in Fig. 15 show attractive results such as: low supply voltage ± 0.4 V; low power consumption close to 23.5 μW, good stability, and high dynamic voltage range. Thus the non-conventional techniques are utilized successfully in LV LP applications.

Acknowledgements

The described research was performed in laboratories supported by the SIX project; the registration number CZ.1.05/2.1.00/03.0072, the operational program Research and Development for Innovation and has been supported by the Czech Science Foundation as project No. GA102/11/1379, and by the Ministry of Industry and Commerce under the contract FR-TI3/485.

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