

Realization of Resistorless Lossless Positive and Negative Grounded Inductor Simulators Using Single ZC-CCCITA

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Abstract. *This paper is in continuation with the very recent work of Prasad et al. [14], wherein new realizations of grounded and floating positive inductor simulator using current differencing transconductance amplifier (CDTA) are reported. The focus of the paper is to provide alternate realizations of lossless, both positive and negative inductor simulators (PIS and NIS) in grounded form using z-copy current-controlled current inverting transconductance amplifier (ZC-CCCITA), which can be considered as a derivative of CDTA, wherein the current differencing unit (CDU) is reduced to a current-controlled current inverting unit. We demonstrate that only a single ZC-CCCITA and one grounded capacitor are sufficient to realize grounded lossless PIS or NIS. The proposed circuits are resistorless whose parameters can be controlled through the bias currents. The workability of the proposed PIS is validated by SPICE simulations on three RLC prototypes.*

Keywords

Positive inductor simulator (PIS), negative inductor simulator (NIS), grounded lossless inductor, z-copy current-controlled current inverting transconductance amplifier (ZC-CCCITA).

1. Introduction

An inductor is a required element in circuit design and can be used in many blocks such as filters, oscillators, phase shifters and impedance matching circuitry. Conventional spiral inductors directly made on chip occupy significant chip area and therefore are too costly and suffer from substrate resistive losses and capacitive couplings. In addition, process tolerances lead to component variations, which cannot easily be tuned in the passive case [1]. Due to these disadvantages, active element-based inductor design has been very desirable to designers. During the last few years, various grounded inductors have been created using different high-performance active building blocks (ABBs), such as minus-type modified inverting first- and second-

generation current conveyor (MICCI-/MICCII-) [2], [3], gain-variable third-generation current conveyor (GVCCIII) [4], dual-X second-generation current conveyor (DXCCII) [5]–[7], differential voltage current conveyor (DVCC) [8], current-feedback operational amplifier (CFOA) [9], [10], positive four-terminal-floating-nullor (PFTFN) [11], differential difference operational mirrored amplifier (DDOMA) [12], and modified dual-output differential difference current conveyor (MDO-DDCC) [13]. A literature survey shows that a large number of grounded inductor realizations based on current conveyors have been proposed, and in general, possess some weaknesses. Although the circuits reported in [2], [3], and [4] realize pure inductance with only one MICCI-, MICCII-, or GVCCIII, respectively, in addition to a grounded resistor all of the circuits employ a floating resistor and a floating capacitor. Similarly, the DXCCII-based inductor simulators in [5]–[7] also consist of floating capacitor and one or two floating resistors. In [8] proposed circuits employing single DVCC, grounded capacitor, and both floating and grounded resistor can simulate grounded, both series and parallel R-L immittances. However, in some applications the lossy term of circuits can be disadvantageous. Similar lossy inductors are presented in [9]. None of circuits can realize positive one, moreover, in circuit Fig. 2(d) of [9] critical capacitance matching is required. In another CFOA-based grounded inductor simulator [10] the intrinsic capacitance of the Analog Devices AD844 IC is used instead of external capacitor. The PFTFN-based inductor [11] requires component matching constraint. The grounded inductor in [12] consists of three DDOMAs, one NMOS, and only grounded passive elements. In recently published paper [13] authors present a lossless grounded inductor using single MDO-DDCC, two resistors, and one grounded capacitor. Since the MDO-DDCC is a non-tunable active element, the proposed circuit can be considered as a minimal configuration in terms of number of active and passive elements used. Although this circuit seems to be very attractive inductance simulator, the floating resistor brings a drawback to it.

Our short study showed that none of the above listed literature present resistorless lossless grounded inductor simulator. In [14], which is one of the most recent reports on current differencing transconductance amplifier (CDTA)

[15]–[22], authors propose resistorless simulators, both in grounded and floating form. The circuit in Fig. 2 of [14] describes nearly the same floating lossless inductor simulator as the topology in Fig. 2(b) of [16], only the input and output terminals of active elements were suitably changed. The grounded simulator in Fig. 1 of [14] is based on the grounded lossless inductor already presented in [17] (see the passive prototype in Fig. 3 and its active equivalent in Fig. 4). The modifications proposed in [14] consist in adding feedforward and feedback paths that, however compared to the solution presented in [17], reduce the final value of the equivalent inductor by four. The proposed grounded inductor simulators in [14] and [17] employ grounded capacitor, which is very desirable for monolithic integration. However, the use of two active elements increases the chip area of the circuit and is not that economical. Therefore, the motivation of this paper is to reduce the number of ABBs in inductor simulators. In particular, we restrict the current paper to the realization of resistorless lossless grounded inductors, but unlike in [14] and [17] we provide realizations for both positive and negative inductor simulator (PIS and NIS). For this purpose a new active building block called the z-copy current-controlled current inverting transconductance amplifier (ZC-CCCITA) is used, which is a derivative of the conventional ZC-CITA [23] and additionally enables to change the intrinsic resistance of the active element by means of external current leading to control the value of the equivalent inductor. In the proposed circuits of PIS and NIS one ZC-CCCITA and one grounded capacitor are only required. The workability of the proposed PIS was verified by SPICE simulations using Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μm level-3 CMOS process parameters [24].

2. Circuit Description

The ZC-CCCITA essentially consists of an input negative current-controlled current follower (i.e. current-controlled current inverter) stage that transfers the input current to the z and zc terminals and a transconductance amplifier stage, which converts the voltage at the z terminal to output current at the x terminal. The intention of using this ABB is that in several cases the CDU of the CDTA is just reduced to either current following or current inverting unit, since in many applications both p and n terminals of CDTA are not used or required simultaneously. Even in the floating inductor proposed in [14] n terminals of CDTA1 and CDTA2 are not used. The circuit symbol and behavioral model of ZC-CCCITA are shown in Fig. 1 and the characterizing equations are as follows:

$$v_f = R_f i_f, \quad i_z = i_{zc} = -i_f, \quad i_{x+} = g_m v_z, \quad i_{x-} = -g_m v_z. \quad (1)$$

In (1), the R_f and g_m represent the intrinsic resistance of f terminal and transconductance from the z terminal to $x+$ and $x-$ terminals, respectively. For CMOS implementation of ZC-CCCITA (Fig. 8), the intrinsic resistance is given as:

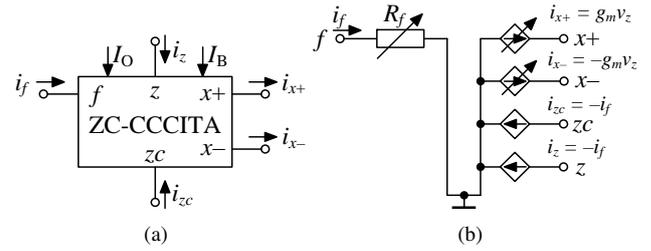


Fig. 1. (a) Circuit symbol and (b) behavioral model of ZC-CCCITA.

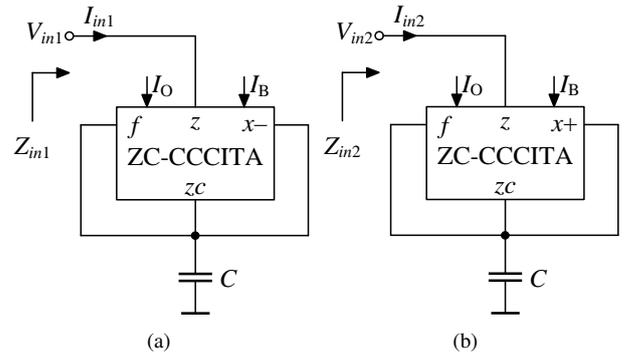


Fig. 2. Proposed grounded lossless (a) positive and (b) negative inductance simulators.

$$R_f = \sqrt{\frac{1}{8k_1 I_O}}, \quad \text{where } k_1 = \mu_p C_{ox} \left(\frac{W}{L}\right)_{3,4} = \mu_n C_{ox} \left(\frac{W}{L}\right)_{1,2} \quad (2)$$

and the transconductance is given as:

$$g_m = \sqrt{k_2 I_B} \quad \text{where } k_2 = \mu_n C_{ox} \left(\frac{W}{L}\right)_{20,21}. \quad (3)$$

Here the $k_i = \mu_{p,n} C_{ox} (W/L)_j$ for $i = 1, 2$ is the physical parameter of the corresponding MOS transistor j (C_{ox} is the gate oxide capacitance per unit area, $\mu_{p,n}$ is the electron mobility in the channel, W and L are the channel width and length), the I_O is the bias current to control the intrinsic resistance of the input terminal f , and the I_B is the control current adjusting the transconductance g_m of the ZC-CCCITA. It should be also noted that the signs of the currents for the current inverter stage are in accordance with the generalized current follower (GCF) stage in [25], [26] (the currents are flowing into the terminals) and is opposite to the convention followed by Bielek *et al.* in [23].

The proposed realizations of grounded lossless PIS and NIS are shown in Fig. 2(a) and Fig. 2(b), respectively. Using (1), routine circuit analysis yields the following input impedances for both circuits:

$$Z_{in1} = -Z_{in2} = sL_{eq} = \frac{sCR_f}{g_m} = \frac{sC}{\sqrt{8k_1 k_2 I_O I_B}}. \quad (4)$$

From (4) it is obvious that circuits in Fig. 2 represent lossless positive and negative inductor simulators, respectively. In both circuits it can be also clearly seen that the inductance value L_{eq} can be adjusted electronically by either I_O and/or I_B currents.

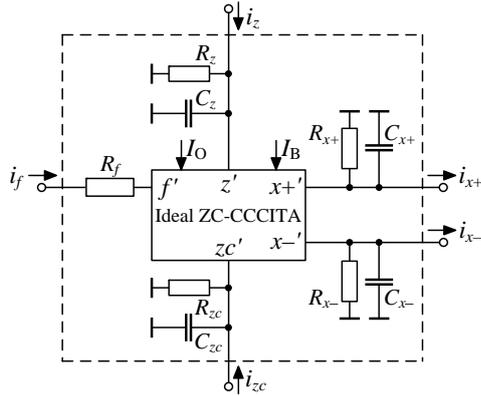


Fig. 3. Model of the ZC-CCCITA including parasitic elements and intrinsic resistance R_f .

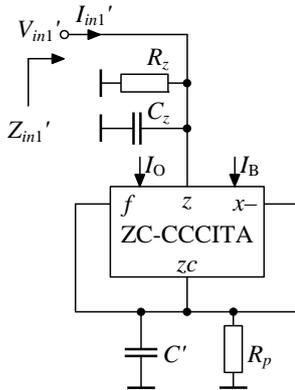


Fig. 4. Proposed grounded lossless PIS in Fig. 2(a) including dominant parasitics.

3. Non-Ideal Analysis

For a complete analysis, it is important to take into account parasitics of the active element (Fig. 3). Except of the intrinsic resistance R_f appearing at the terminal f , which is controllable through the bias current I_O of the current inverting stage and in our case is requested, following non-idealities of the ZC-CCCITA can be considered:

- $i_z = -\beta_1 i_f$ and $i_{zc} = -\beta_2 i_f$, where β_1 and β_2 represent current gains that differ from their ideally unity values by current tracking errors ϵ_i ($|\epsilon_i| \ll 1$), where $i = 1, 2$.
- The parasitic resistances R_z , R_{zc} and parasitic capacitances C_z , C_{zc} appearing between the high-impedance z and zc terminals and ground, respectively.
- The parasitic resistance $R_{x\pm}$ and parasitic capacitance $C_{x\pm}$ appearing between the high-impedance $x\pm$ terminals of the transconductance amplifier and ground.

Here, the following non-ideal analysis will only focus on the grounded lossless PIS circuit, i.e. Fig. 4. We believe that it is sufficient since in case of the NIS it involves only sign change. It is also worth mentioning that the effects of the parasitic resistances R_z , R_x and capacitances C_z and C_x are not considered in [14] within deriving the non-ideal values of the simulated inductance. But, here we consider them,

as they will eventually lead to realization of lossy inductor rather than lossless inductor as indicated in [14]. Moreover, important results to improve the quality factor Q of the simulated lossy inductor are found.

Taking into account the aforementioned non-idealities, except for the parasitics R_z and C_z , the input impedance of the circuit from Fig. 4 is given as:

$$Z_{in1}' = R_{lossy} + sL_{eq} = \frac{1 - \beta_2}{\beta_1 g_m} + \frac{R_f}{\beta_1 R_p g_m} + \frac{sC'R_f}{\beta_1 g_m} = \frac{1 - \beta_2}{\beta_1 \sqrt{k_2 I_B}} + \frac{1}{\beta_1 R_p \sqrt{8k_1 k_2 I_O I_B}} + \frac{sC'}{\beta_1 \sqrt{8k_1 k_2 I_O I_B}} \quad (5)$$

where $R_p = R_{zc} || R_{x-}$ and $C' = C + C_{zc} + C_{x-}$, respectively. Equation (5) clearly indicates that there is a lossy term (resistance) in the simulated impedance and thus the quality factor of the inductor is not infinite, but found to be:

$$Q_L = \frac{\omega L_{eq}}{R_{lossy}} = \frac{\omega C' R_p R_f}{R_p (1 - \beta_2) + R_f} = \frac{\omega C' R_p}{[R_p \sqrt{8k_1 k_2 I_O} (1 - \beta_2)] + 1} \quad (6)$$

To increase the quality factor of the simulated inductor, the lossy term needs to be minimized and this can be achieved by:

- making the β_2 very close to unity (by using high-output resistance current mirrors) and,
- choosing $R_f \ll R_p$, i.e. $\sqrt{\frac{1}{8k_1 I_O}} \ll R_p$.

Assuming now the lossy term being minimized, the input impedance Z_{in1}' approximates to the inductance of value $L_{eq} = \frac{C'R_f}{\beta_1 g_m} = \frac{C'}{\beta_1 \sqrt{8k_1 k_2 I_O I_B}}$. In practice, the external capacitor is chosen such that $C \gg C_{zc} + C_{x-}$.

Till now, we have neglected the effects of parasitics R_z and C_z . Taking them into account we get the input admittance as:

$$Y_{in1} = \frac{1}{R_z} + sC_z + \frac{1}{sL_{eq}} = \frac{1}{R_z} + sC_z + \frac{\beta_1 \sqrt{8k_1 k_2 I_O I_B}}{sC'} \quad (7)$$

Assuming the operating frequency $f \ll 1/2\pi \times \min \left\{ \frac{\beta_1 (8k_1 k_2 I_O I_B)^{1/2}}{C'}, \left[\frac{\beta_1 (8k_1 k_2 I_O I_B)^{1/2}}{C' C_z} \right]^{1/2} \right\}$, the upper frequency potential of the circuit is limited. However, the effects of the parasitics on the simulated inductance can be sufficiently reduced by techniques proposed in [27].

4. Application Examples

4.1 Fourth-Order High-Pass Filter Design

To illustrate an application of the proposed grounded lossless PIS, it is used in an fourth-order high-pass filter (HPF) realization [11]. The passive RLC prototype is shown in Fig. 5(a) and its transfer function is given by:

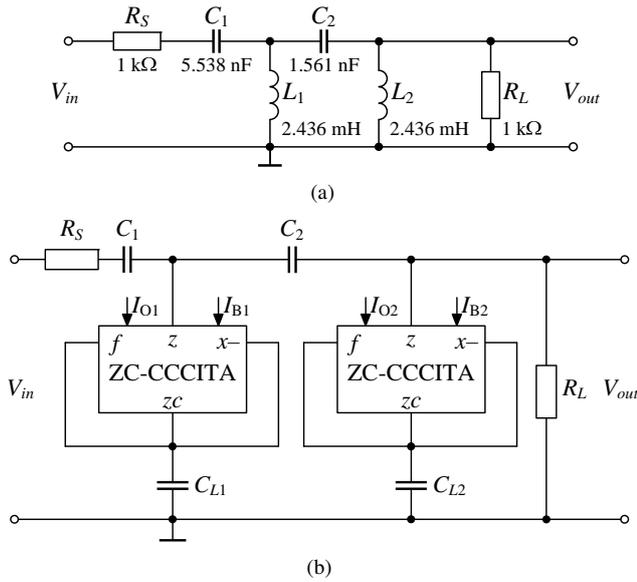


Fig. 5. (a) Fourth-order high-pass filter prototype with Butterworth response and (b) the transformed equivalent circuit diagram.

$$K_{HPF}(s) = \frac{V_{out}}{V_{in}} = \frac{s^4}{a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0} \quad (8)$$

where

$$\begin{aligned} a_4 &= 1 + \frac{R_S}{R_L}, \\ a_3 &= \frac{R_S}{L_1} + \frac{R_S}{L_2} + \frac{1}{C_1R_L} + \frac{1}{C_2R_L}, \\ a_2 &= \frac{1}{L_1C_1} + \frac{1}{L_2C_1} + \frac{1}{L_2C_2}, \\ a_1 &= \frac{1}{L_1C_1R_LC_2} + \frac{R_S}{L_1L_2C_2}, \\ a_0 &= \frac{1}{L_1L_2C_1C_2}. \end{aligned} \quad (9)$$

The transformed equivalent active circuit using the proposed grounded lossless PIS is shown in Fig. 5(b). Here the \$L_1\$ and \$L_2\$ are \$\frac{C_{L1}}{\sqrt{8k_1k_2I_{O1}I_{B1}}}\$ and \$\frac{C_{L2}}{\sqrt{8k_1k_2I_{O2}I_{B2}}}\$, respectively.

4.2 Second-Order Band-Pass Filter Design

The workability of the proposed grounded lossless PIS has also been verified by designing second-order band-pass filter (BPF) [14]. The passive RLC BPF is shown in Fig. 6(a) and the appropriate active circuit using the proposed grounded lossless PIS is shown in Fig. 6(b). Routine circuit analysis yields the following voltage transfer function of the BPF:

$$K_{BPF}(s) = \frac{V_{out}}{V_{in}} = \frac{s \frac{1}{CR}}{s^2 + s \frac{1}{CR} + \frac{1}{LC}} = \frac{s \frac{1}{CR}}{s^2 + s \frac{1}{CR} + \frac{\sqrt{8k_1k_2I_{O}I_{B}}}{C_L C}}. \quad (10)$$

The natural angular frequency \$\omega_0\$, the quality factor \$Q\$, and the bandwidth \$BW\$ (\$\omega_0/Q\$) of the BPF can be found as:

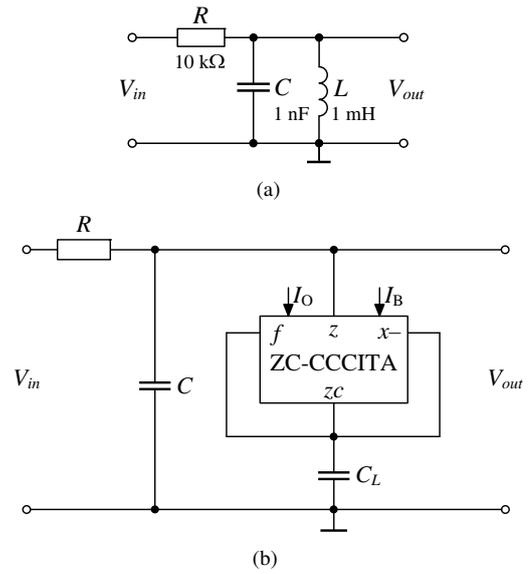


Fig. 6. (a) Second-order band-pass filter prototype and (b) the transformed equivalent circuit diagram.

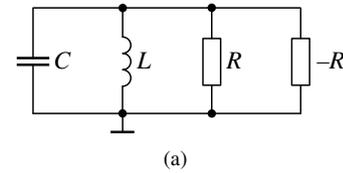


Fig. 7. (a) Quadrature oscillator prototype and (b) the transformed equivalent circuit diagram.

$$\omega_0 = \sqrt{\frac{1}{LC}} = \frac{(8k_1k_2I_{O}I_{B})^{1/4}}{(C_L C)^{1/2}}, \quad (11)$$

$$Q = R\sqrt{\frac{C}{L}} = R \left[\frac{C(8k_1k_2I_{O}I_{B})^{1/2}}{C_L} \right]^{1/2}, \quad (12)$$

$$BW = \frac{1}{CR}. \quad (13)$$

The active and passive sensitivities of the filter parameters are following:

$$S_{k_1, k_2, I_{O}, I_{B}}^{\omega_0} = \frac{1}{4}, S_{C_L, C}^{\omega_0} = -\frac{1}{2}, S_R^{\omega_0} = 0, \quad (14)$$

$$S_{k_1, k_2, I_{O}, I_{B}}^Q = \frac{1}{4}, S_C^Q = -S_{C_L}^Q = \frac{1}{2}, S_R^Q = 1, \quad (15)$$

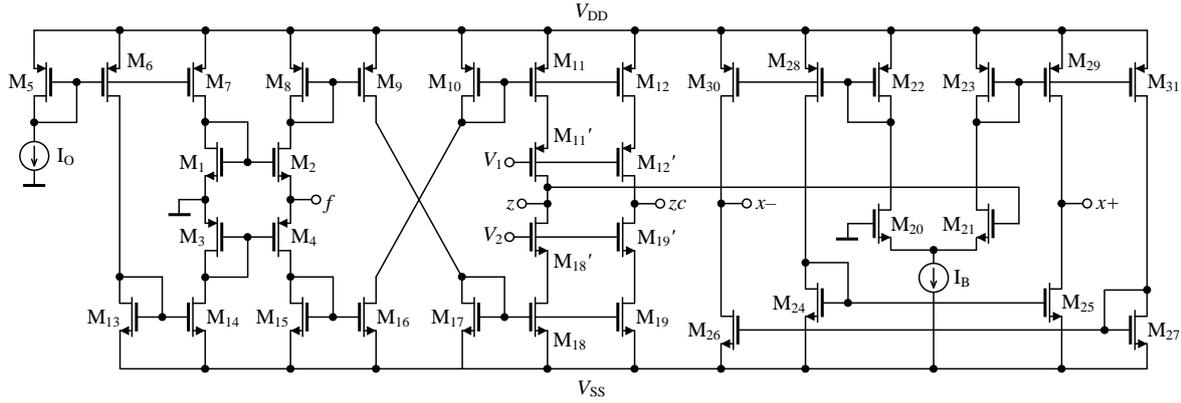


Fig. 8. CMOS internal structure of ZC-CCCITA.

$$S_{C,R}^{BW} = -1, S_{k_1, k_2, I_{O1}, I_{B1}, C_L}^{BW} = 0. \tag{16}$$

Equations (14)–(16) indicate that all the passive and active sensitivities are not more than unity in absolute value, and hence, the proposed circuit exhibits an attractive sensitivity performance.

4.3 Quadrature Oscillator Design

The third application of proposed grounded lossless PIS is quadrature oscillator (QO). Quadrature sinusoidal oscillators are important circuits for various communication applications, wherein there is a requirement of multiple sinusoids that are 90° phase shifted, e.g. in quadrature mixers and single-sideband modulators, or for measurement purposes in the vector generator or selective voltmeters [28]. Therefore, QOs are widely used in many communication, signal processing, and instrumentation systems [29]–[31]. Fig. 7(a) shows the realization of the oscillator, which is a parallel connection of a capacitor, positive inductor, positive resistor and negative resistor, respectively. The appropriate active QO using the proposed grounded lossless PIS and ZC-CCCITA-based negative resistor is shown in Fig. 7(b). Routine circuit analysis yields the following characteristic equation (CE):

$$CE: s^2 C_L C_R R_{f1} + R_{f1} s C_L (1 - g_{m2} R) + g_{m1} R = 0. \tag{17}$$

From (17) the condition of oscillation (CO) and the frequency of oscillation (FO) can be evaluated as:

$$CO: g_{m2} R \geq 1 \text{ or } R \sqrt{k_2 I_{B2}} \geq 1, \tag{18}$$

$$FO: \omega_0 = \sqrt{\frac{g_{m1}}{C_L C_R R_{f1}}} = \frac{(8k_1 k_2 I_{O1} I_{B1})^{1/4}}{(C_L C)^{1/2}}. \tag{19}$$

From (18) and (19) it is clear that the CO can be controlled independently of FO by means of varying the control current I_{B2} and the FO can be controlled via the bias current I_{O1} and/or by adjusting the control current I_{B1} , respectively.

Thus, the proposed oscillator provides independent control of the CO and the FO. The relationship between the output voltages can be given as:

$$V_{out2} = -jk' V_{out1} \tag{20}$$

where

$$k' = \frac{g_{m1}}{\omega_0 C_L} = \frac{\sqrt{k_2 I_{B1}}}{\omega_0 C_L}, \tag{21}$$

ensuring the output voltages V_{out1} and V_{out2} to be quadrature (the phase difference $\phi = 90^\circ$) and have equal amplitudes if $k' = 1$.

5. Simulation Results

To verify the theoretical analyses, the proposed grounded lossless PIS in Fig. 2(a), filter, and oscillator examples in Figs. 5(b), 6(b), and 7(b) have been simulated using SPICE software. The CMOS implementation of the ZC-CCCITA is shown in Fig. 8. In the design, transistors are modeled by the TSMC 0.35 μm level-3 CMOS process parameters [24]. Dimensions of transistors are listed in Tab. 1. The DC power supply voltages are equal to $+V_{DD} = -V_{SS} = 1.5$ V and $V_1 = V_2 = 0$ V. Simulated intrinsic resistance at input terminal R_f and transconductance value g_m relative to I_{O1} and I_{B1} , respectively, are shown in Fig. 9.

PMOS transistors	W(μm)/L(μm)
M ₃ , M ₄	60/0.35
M ₅ –M ₇	30/2
M ₈ –M ₁₂ , M ₁₁ ' , M ₁₂ '	30/1
M ₂₂ , M ₂₃	2/0.5
M ₂₈ –M ₃₁	8/0.5
NMOS transistors	W(μm)/L(μm)
M ₁ , M ₂	20/0.35
M ₁₃ –M ₁₉ , M ₁₈ ' , M ₁₉ '	10/1
M ₂₀ , M ₂₁	5/0.5
M ₂₄ –M ₂₇	2/0.5

Tab. 1. Transistor dimensions of the ZC-CCCITA.

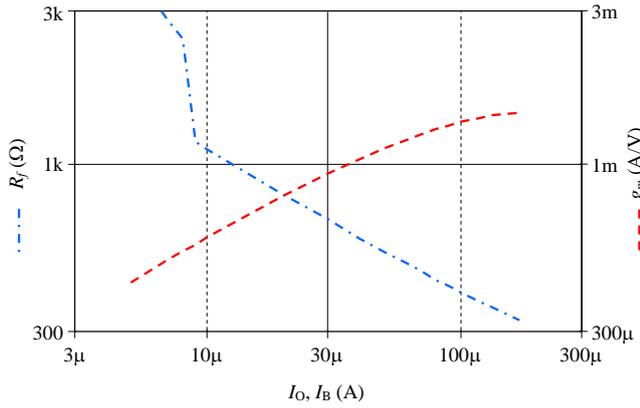


Fig. 9. Intrinsic resistance at input terminal R_f relative to I_O and transconductance value g_m relative to I_B .

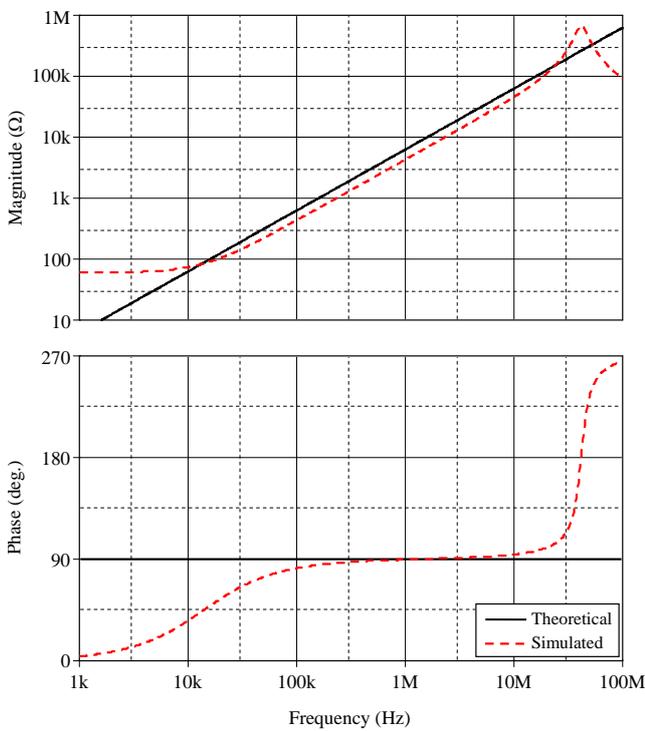


Fig. 10. Theoretical and simulated magnitude and phase responses of the impedance of the proposed grounded lossless PIS relative to frequency for $L_{eq} = 1$ mH.

The proposed grounded lossless PIS shown in Fig. 2(a) is simulated with the following active parameters and passive element values: $I_O = 12.5 \mu A$, $I_B = 36 \mu A$, and $C = 1$ nF which results in $L_{eq} = 1$ mH. The theoretical and simulated magnitude and phase responses are shown in Fig. 10. As it can be seen from Fig. 10, the magnitude of impedance increases with the frequency. Due to parasitic elements restricting the performance of the proposed PIS the useful frequency ranges is about 14 kHz up to 21 MHz. Wider operating frequency ranges can be achieved using parasitic impedance reduction techniques proposed in [27]. Fig. 11 shows impedance values relative to frequency of the PIS with different I_B . It confirms that the simulated inductance can be adjusted by control the I_B current of the ZC-CCCITA.

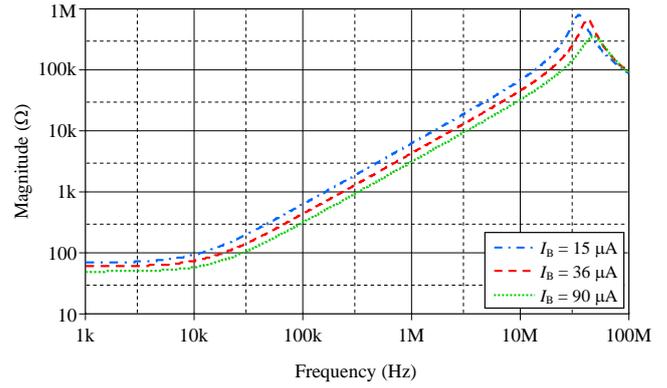


Fig. 11. Simulated magnitude responses of the impedance of the grounded lossless PIS relative to frequency for different I_B .

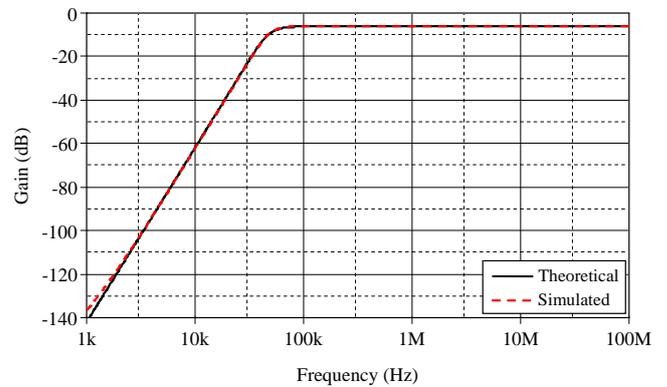


Fig. 12. Theoretical and simulated magnitude responses of the fourth-order HPF.

To design the fourth-order high-pass filter for a cut-off frequency of $f_0 = 50$ kHz with the Butterworth approximation, the normalized design ($f_0 = 1$ Hz) was obtained with the following component values: $R_S = R_L = 1 \Omega$, $L_1 = L_2 = 0.1217$ H, $C_1 = 0.2768$ F, and $C_2 = 0.0780$ F. To get the required cut-off frequency, appropriate frequency scaling has been performed. The resulting values of the components have been found to be as shown in Fig. 5(a) [11]. The derived equivalent filter in Fig. 5(b) has been designed by using two simulated inductors with values $L_1 = L_2 = 2.436$ mH ($I_{O1} = I_{O2} = 12.5 \mu A$, $I_{B1} = I_{B2} = 36 \mu A$, and $C_{L1} = C_{L2} = 2.436$ nF). Fig. 12 compares the magnitude response of the simulated high-pass filter with passive inductor and simulated inductor.

The second-order band-pass filter from Fig. 6(b) has been simulated for the characteristic frequency $f_0 = \omega_0/2\pi \cong 159.15$ kHz and the quality factor $Q = 10$. The passive component values are shown in Fig. 6(a). The inductor simulator is realized with the following active parameters and passive element values: $I_O = 12.5 \mu A$, $I_B = 36 \mu A$, and $C_L = 1$ nF to obtain the required $L = 1$ mH. Ideal and simulated magnitude responses of the second-order BPF are shown in Fig. 13(a). Additionally, the transient simulation result of the filter with $Q = 1$ (in Fig. 6 the $R = 1$ k Ω) is shown in Fig. 13(b) in which a sinusoidal input voltage signal with 100 mV peak value at 159.15 kHz is applied to the

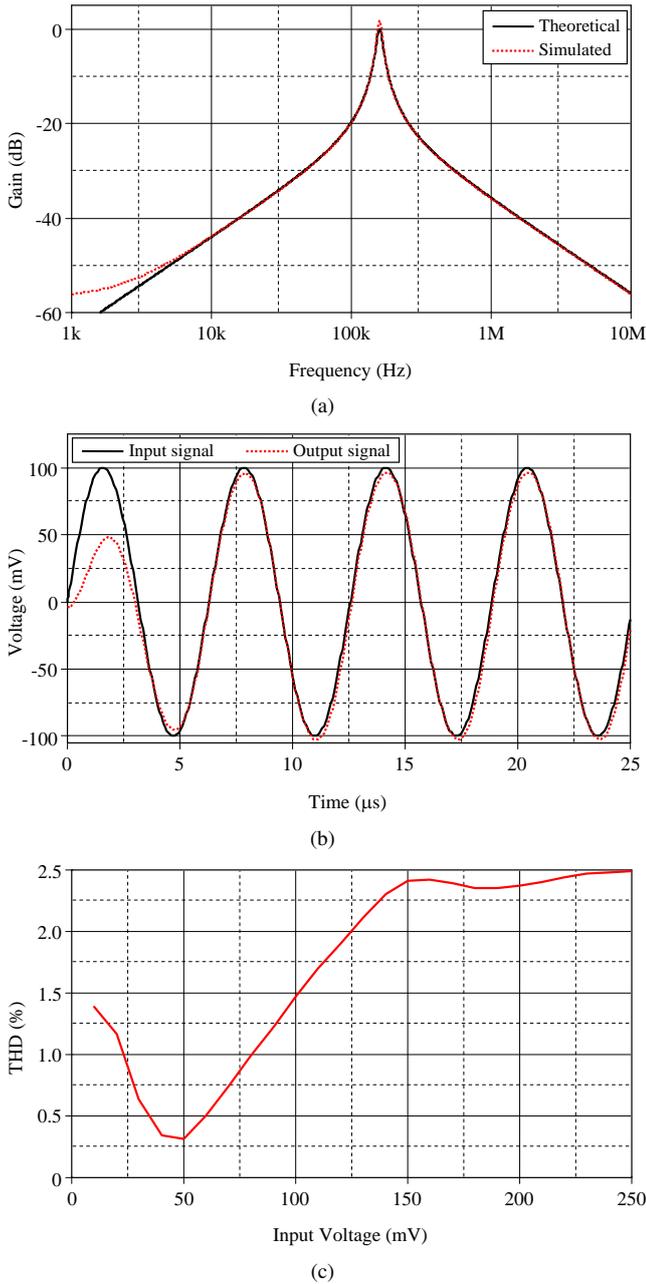


Fig. 13. (a) Theoretical and simulated magnitude responses, (b) time-domain responses and (c) THD of the proposed second-order BPF at 159.15 kHz.

filter. In order to investigate distortion of the proposed BPF, the total harmonic distortion (THD) at 159.15 kHz has been simulated and the results are shown in Fig. 13(c).

The proposed quadrature oscillator is shown in Fig. 7(b). To obtain the sinusoidal output waveforms with the oscillation frequency of $f_0 = \omega_0/2\pi \cong 159.15$ kHz, the following active parameters and the passive element values have been chosen: $I_{O1} = 12.5 \mu\text{A}$, $I_{B1} = 36 \mu\text{A}$, $C_L = 1$ nF (to obtain the required $L = 1$ mH), $C = 1$ nF, $R = 1$ k Ω , $I_{O2} = 12.5 \mu\text{A}$, and $I_{B2} = 36 \mu\text{A}$, respectively. In practice, to ensure the startup (build-up) of oscillations and subsequently to satisfy the CO in (18) the value of R is chosen as 1.1 k Ω .

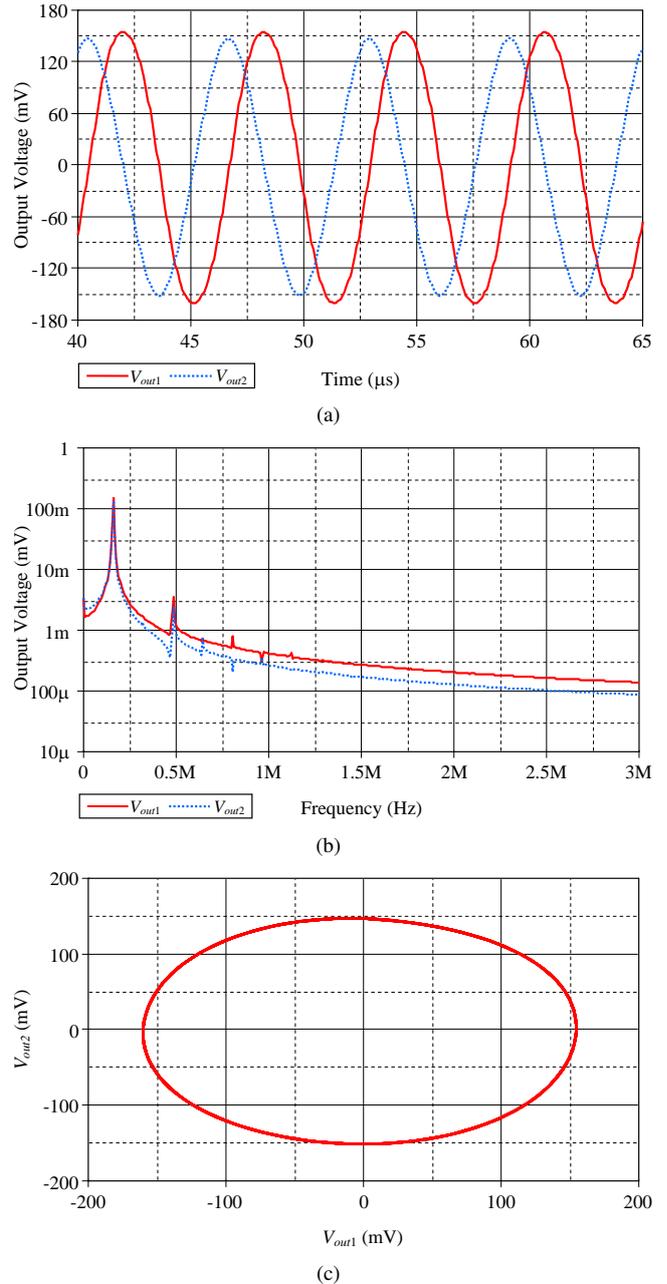


Fig. 14. (a) Steady state oscillation waveforms of the quadrature outputs, (b) frequency spectrums, (c) Lissajous figure.

The steady state waveforms of the quadrature voltages are shown in Fig. 14(a). The generated frequency is 159.05 kHz, which is in close correspondence with the theoretical value. Fig. 14(b) shows the simulated frequency spectrums of both outputs V_{out1} and V_{out2} with THD values 2.93 % and 2.48 %, respectively. The quadrature relationship between the generated waveforms has been verified using Lissajous figure shown in Fig. 14(c).

The SPICE simulations confirm the feasibility of the proposed grounded lossless PIS and the results are satisfactory. The small deviations from the theoretical characteristics are mainly caused by the non-ideal behavior of the proposed inductance simulator discussed in Section 3.

6. Conclusion

The group of CDTA-based inductor simulators in [14] and [17] are supplemented by new realizations of lossless grounded positive (PIS) and negative (NIS) inductor simulators. The proposed circuits are resistorless and minimal in configuration in terms of the number of employed ABBs and employ only grounded capacitor. The workability of the proposed grounded lossless PIS has been verified by its use in three RLC passive prototypes. Although the possibility of alternate realizations are not ruled out, it is believed that the proposed circuits here and those in [14] and [17] cover the most important grounded inductor simulators created using CDTA or its derivative elements.

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