High-Input Impedance Voltage-Mode Multifunction Filter Using a Single DDCCTA and Grounded Passive Elements

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Abstract. *In this paper, a novel single-input three-output (SITO) second-order multifunction active voltage filter with high-input impedance is proposed. The proposed circuit is based on using the recently reported active building block, namely differential difference current conveyor transconductance amplifier (DDCCTA). It employs one DDCCTA as active element together with one grounded resistor and two grounded capacitors as passive elements. The circuit still maintains the following advantageous features : (i) the simultaneous realization of lowpass, bandpass and highpass responses from the same topology, (ii) no requirements for component matching conditions, (iii) electronic controllability of important filter parameters, (iv) simpler structure due to contains only one DDCCTA and three passive elements, and (v) low sensitivity performance. The non-ideal gain effects of the developed filter are examined and PSPICE simulation results are included using 0.5 μm MIETEC CMOS technology parameters.*

Keywords

Differential Difference Current Conveyor Transconductance Amplifier (DDCCTA), multifunction filter, voltage-mode circuit.

1. Introduction

The applications and advantages in the simultaneous realization of filter transfer functions have widely found in many engineering areas, such as the phase-lock-loop FM stereo demodulator, the touch-tone telephone tone decoder and the crossover network used in a three-way high-fidelity loudspeaker [1]. From the point view of the advantages of simplicity, cost reduction, power consumption and space saving, it is important to implement active voltage biquad filters using a minimum number of active and passive elements [2]. Therefore, numerous voltage-mode filter configurations using single active element and minimum number of passive elements have received significant attention in technical literature [3]-[10]. However, all of them employ floating passive elements for their realization. Note that the employment of only grounded capacitors and resistors is advantageous in the reduction of parasitic impedance effects as well as in easy integrated circuit implementation [11]-[12]. The biquads presented in [4], [6], [9] require resistive/capacitive component matching conditions, whereas the circuit of [3] requires changes in the passive components to realize different filter functions. Moreover, the structure in [10] needs input signals V_{in}, $-V_{in}$ and $-2V_{in}$; thus, there is a requirement of additional circuits.

Recently, a relatively new active building block, the so-called differential voltage current conveyor transconductance amplifier (DVCCTA), was introduced [13]. The DVCCTA device is obtained by cascading of the differential voltage current conveyor (DVCC) with the operational transconductance amplifier (OTA) in monolithic chip for compact implementation of analog function circuits [13]-[15]. Thereafter several different applications of the DVCCTA have been presented in the technical literature, particularly from the area of frequency filters [15]-[17]. Among these, the authors in [15] proposed the voltage-mode biquadratic filter configuration with high-input impedance using one DVCCTA and two grounded capacitors. However, only two standard filter functions (i.e. LP and BP) can be obtained simultaneously. All the recently published multifunction voltage-mode filters in [16]-[17] employ two floating capacitors, and require critical matching component constraints for each filter response. With three-input two-output structure, the circuits also require an additional hardware for selecting the relevant input and output terminals in each filter response realization. In addition, these two proposed configurations also do not posses high input impedance. Second-order active voltage filters with high-input impedance are great of interest, since several cells of this kind can be directly connected in cascade to realize high-order filters [18].

In this paper, a voltage-mode biquadraric multifunction filter with one high input impedance and three output terminals based on the differential difference current conveyor transconductance amplifier (DDCCTA) is presented. The DDCCTA can easily be implemented from a DVCCTA by adding the Y3 terminal. Contrary to the

previously reported single active element-based voltage-mode filters [3]-[10], [15]-[17], the proposed circuit offers the following advantageous features :

(i) It uses a single DDCCTA, one grounded resistor and two grounded capacitors, which are the minimum components necessary for realizing a biquadratic filtering function from the same topology.

(ii) All passive elements are grounded.

(iii) It can simultaneously realize LP, BP and HP responses from the same topology.

(iv) It does not require component matching conditions.

(v) It has high-input impedance.

(vi) The natural angular frequency (ω_0) and the quality factor (Q) are electronically controllable through the transconductance parameter (g_m) of the DDCCTA.

(vii) It has low sensitivity performance.

The proposed circuit has been implemented using 0.5 μm MIETEC CMOS technology, and is simulated with PSPICE to confirm the theory.

2. Description of the DDCCTA

The DDCCTA element is based on the use of the DDCC as an input stage and the OTA as an output stage. As shown in Fig. 1, the port characteristics of the DDCCTA can be described by the following expressions:

$$i_{Y1} = i_{Y2} = i_{Y3} = 0 \ , \ \ v_X = v_{Y1} - v_{Y2} + v_{Y3} \ ,$$
$$i_Z = i_X \ , \ \ i_O = g_m v_Z \qquad (1)$$

where g_m is the transconductance parameter of the DDCCTA.

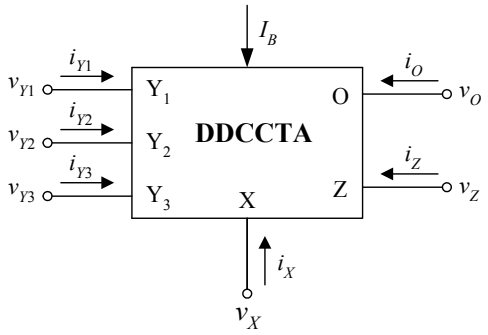

Fig. 1. Circuit symbol of the DDCCTA.

The internal structure of the DDCCTA in CMOS technology is shown in Fig. 2. The scheme is based on the internal circuit of the DDCC [19], which is followed by a TA [20]. In this case, the transconductance gain (g_m) of the DDCCTA can be given by:

$$g_m = \sqrt{\mu C_{ox} \frac{W}{L} I_B} \qquad (2)$$

where I_B is an external DC bias current, μ is the effective channel mobility, C_{ox} is the gate-oxide capacitance per unit area, W and L are channel width and length, respectively. It should be noted that the g_m-value of the DDCCTA can be adjustable electronically by I_B.

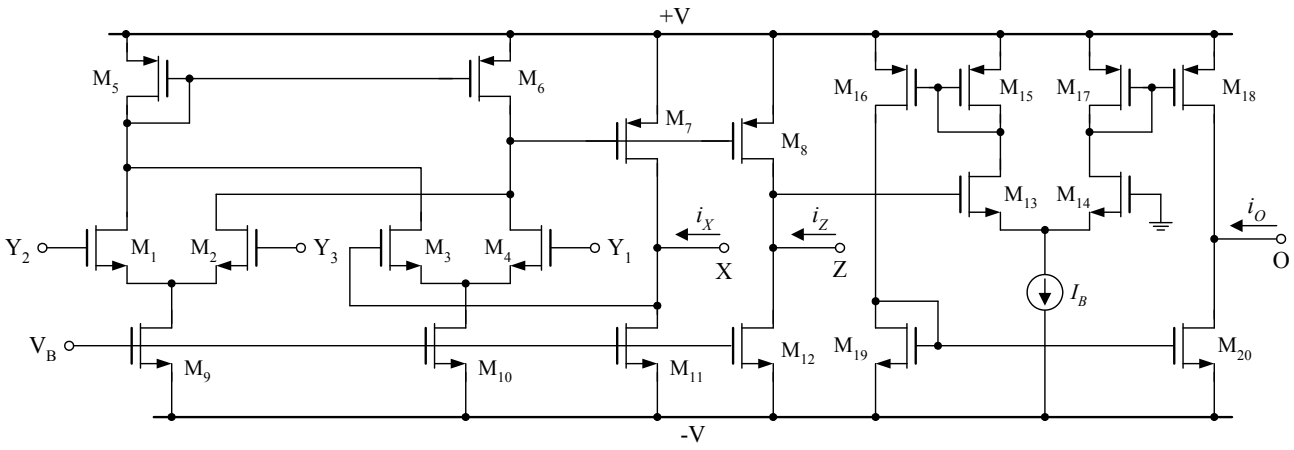

Fig. 2. CMOS internal structure of the DDCCTA.

3. Proposed Filter Configuration

Using a single DDCCTA and a canonical number of passive elements (one resistor and two capacitors), the voltage-mode multifunction filter with one input terminal and three output terminals can be obtained as shown in Fig. 3. It can be seen that the input of the proposed filter is applied to the Y_1 terminal of the DDCCTA. Therefore, the circuit has the advantage of high-input impedance. Since all the passive components are grounded, it is therefore suitable for integrated circuit implementation point of view. By routine circuit analysis using (1), the voltage

transfer functions of the proposed filter in Fig. 3 can be given by :

$$HP(s) = \frac{V_{o1}(s)}{V_{in}(s)} = \frac{s^2}{D(s)} \quad , \tag{3}$$

$$LP(s) = \frac{V_{o2}(s)}{V_{in}(s)} = \frac{\left(-\frac{g_m}{R_1C_1C_2}\right)}{D(s)} \quad , \tag{4}$$

and

$$BP(s) = \frac{V_{o3}(s)}{V_{in}(s)} = \frac{\left(\frac{s}{R_1C_1}\right)}{D(s)} \tag{5}$$

where denominator $D(s)$ is found as :

$$D(s) = s^2 + \left(\frac{s}{R_1C_1}\right) + \left(\frac{g_m}{R_1C_1C_2}\right) \quad . \tag{6}$$

It can be seen from (3)-(6) that the HP, LP and BP responses are available at the node voltages v_{o1}, v_{o2} and v_{o3}, respectively. Also note that there is no need of any component-matching constraints for all filter response realizations.

From (3)-(6), the filter responses are characterized by the important parameters (i.e., natural angular frequency (ω_0), bandwidth (BW) and quality factor (Q)) as follows :

$$\omega_0 = \sqrt{\frac{g_m}{R_1C_1C_2}} \quad , \tag{7}$$

$$BW = \frac{1}{R_1C_1} \quad , \tag{8}$$

and

$$Q = \sqrt{\frac{g_mR_1C_1}{C_2}} \quad . \tag{9}$$

Equations (7)-(9) show that the important filter parameters can electronically be tuned by varying g_m. Moreover, equations (7) and (9) also show that the parameters ω_0 and Q for all the filter responses are interactive. However, the technique to obtain the non-interactive filter parameter control can be suggested as follows. For the fix-valued capacitors, the ω_0 can be adjusted arbitrarily without disturbing Q by simultaneously changing g_m and R_1 and keeping the product g_mR_1 constant. On the other hand, the parameter Q can be tuned without disturbing ω_0 by simultaneously increasing g_m and R_1 and keeping g_m/R_1 constant.

It should be mentioned here that the proposed circuit configuration in Fig. 3 does not provide the low-output impedance. This is due to the fact that the major goal of this work is to design a compact filter configuration with the distinct advantage of using a single active element along with three grounded passive elements, fulfilling this requirement is not expected. In addition, the grounded resistor R_1 in the proposed filter may easily be realized as a variable resistance using two MOSs to obtain electronic tunability [21].

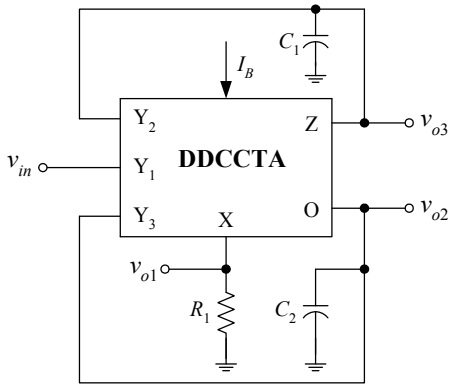

Fig. 3. Proposed filter configuration.

4. Non-Ideal Analysis and Sensitivity Performance

Taking into consideration the DDCCTA non-idealities, the port characteristics in (1) can be rewritten as:

$$i_{Y1} = i_{Y2} = i_{Y3} = 0 \quad , \quad v_X = \beta_1 v_{Y1} - \beta_2 v_{Y2} + \beta_3 v_{Y3} \, ,$$
$$i_Z = \alpha i_X \quad , \quad i_O = g_m v_Z \tag{10}$$

where and $\beta_k = 1 - \varepsilon_{vk}$ for k =1, 2, 3 and $\alpha = 1 - \varepsilon_i$. Here, ε_{vk} ($|\varepsilon_{vk}| << 1$) and ε_i ($|\varepsilon_i| << 1$) represent the voltage and current tracking errors of the DDCCTA, respectively. Thus, re-analysis of the proposed circuit in Fig. 3 yields the denominator of non-ideal voltage transfer functions as follows:

$$D(s) = s^2 + \left(\frac{\beta_2\alpha}{R_1C_1}\right)s + \left(\frac{\beta_3\alpha g_m}{R_1C_1C_2}\right) \quad . \tag{11}$$

The filter parameters for the non-ideal case are obtained as :

$$\omega_0 = \sqrt{\frac{\beta_3\alpha g_m}{R_1C_1C_2}} \quad , \tag{12}$$

$$BW = \frac{\beta_2\alpha}{R_1C_1} \quad , \tag{13}$$

and

$$Q = \frac{1}{\beta_2}\sqrt{\frac{\beta_3 g_m R_1C_1}{\alpha C_2}} \quad . \tag{14}$$

The active and passive sensitivities of the proposed circuit are shown as:

$$S_{g_m}^{\omega_0} = S_{\beta_3}^{\omega_0} = S_{\alpha}^{\omega_0} = -S_{R_1}^{\omega_0} = -S_{C_1}^{\omega_0} = -S_{C_2}^{\omega_0} = \frac{1}{2} \quad , \tag{15}$$

$$S_{\beta_2}^{BW} = S_{\alpha}^{BW} = -S_{R_1}^{BW} = -S_{C_1}^{BW} = -S_{\beta_2}^{Q} = 1 \quad , \tag{16}$$

$$S_{g_m}^{Q} = S_{\beta_3}^{Q} = -S_{\alpha}^{Q} = S_{R_1}^{Q} = S_{C_1}^{Q} = -S_{C_2}^{Q} = \frac{1}{2} \quad , \tag{17}$$

and $S_{\beta_1}^{\omega_0} = S_{\beta_2}^{\omega_0} = S_{g_m}^{BW} = S_{\beta_1}^{BW} = S_{\beta_3}^{BW} = S_{C_2}^{BW} = S_{\beta_1}^{Q} = 0$. (18)

From the above calculations, it is clearly observed that all of the parameter sensitivities are within unity in magnitude.

5. Effect of DDCCTA Parasitic Impedances

In this section, the parasitic impedance effect of the DDCCTA is to be considered. Analogous to DVCC and OTA active elements, the practical DDCCTA with its various parasitics is represented in Fig. 4. It is shown that the DDCCTA has a low-value parasitic serial resistance at port X (R_x), and high input impedances at ports Y_1, Y_2 and Y_3 ($R_{y1}//C_{y1}$, $R_{y2}//C_{y2}$ and $R_{y3}//C_{y3}$), respectively. Also, the output ports Z and O exhibit high output impedances $R_z//C_z$ and $R_o//C_o$, respectively. Since the X terminal of the DDCCTA in the proposed circuit of Fig. 3 is connected to a resistor R_1, the parasitic resistance R_x does not affect the circuit performance as it merges with the resistor [22]. It is further noted that the proposed circuit employs capacitors C_1 and C_2 at the terminals Z and O, respectively. Hence, to reduce the parasitic impedance effects of Z and O terminals, the following conditions must be satisfied:

$$\frac{1}{sC_1} << (R_Z // R_{y2}) \tag{19}$$

and

$$\frac{1}{sC_2} << (R_o // R_{y3}) \tag{20}$$

where $C_1 >> C_{y2} + C_z$ and $C_2 >> C_{y3} + C_o$. It is apparent that (19) and (20) are easily achievable in practice.

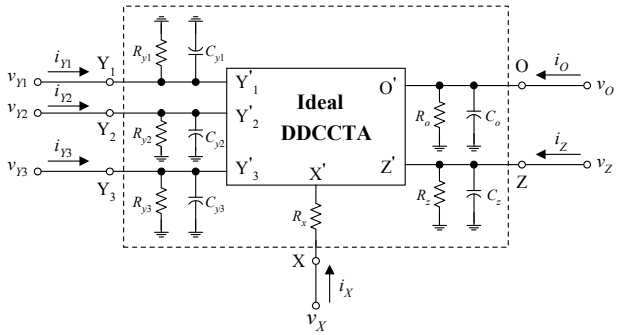

Fig. 4. Real DDCCTA with its parasitic elements.

6. Computer Simulation Results

To verify theoretical analysis, the proposed single DDCCTA-based voltage-mode multifunction filter of Fig. 3 has been simulated with PSPICE program using MIETEC 0.5 µm CMOS technology process parameters. The DDCCTA was performed by the CMOS structure given in Fig. 2 with supply voltages of +V = -V = 3 V, and V_B = -1.22 V. The aspect ratios of CMOS transistors are given in Tab. 1. Fig. 5 shows the characteristic of the g_m-value of the DDCCTA as a function of the external DC bias current I_B.

The filter is designed to realize LP, BP and HP responses with $f_0 \cong \omega_0/2\pi$ = 1.6 MHz and Q = 1. For this purpose, the active and passive components are chosen as: $g_m \cong 101.44$ µA/V (I_B = 16.5 μA), R_1 = 10 kΩ and $C_1 = C_2$ = 10 pF. The simulated responses comparing with the theoretical values are shown in Fig. 6. From the results, it can be observed that the simulation results agree very well with theoretical predictions.

Transistors	W (µm)	L (µm)
M_1 - M_4	1.8	0.7
M_5 - M_6	5.2	0.7
M_7 – M_{10}	20	0.7
M_{11} – M_{12}	58	0.7
M_{13} – M_{20}	4	1.0

Tab. 1. Transistor aspect ratios of the DDCCTA circuit shown in Fig. 2.

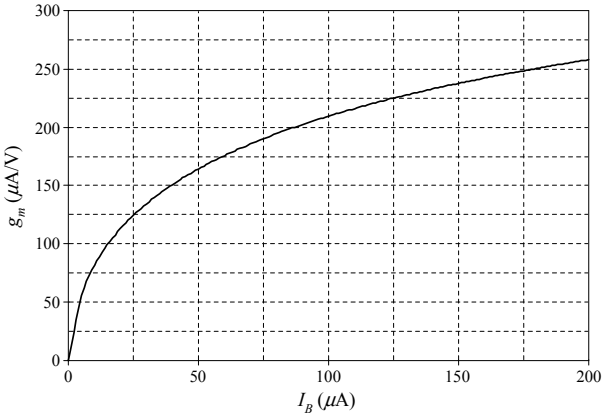

Fig. 5. Variation of g_m as a function of I_B.

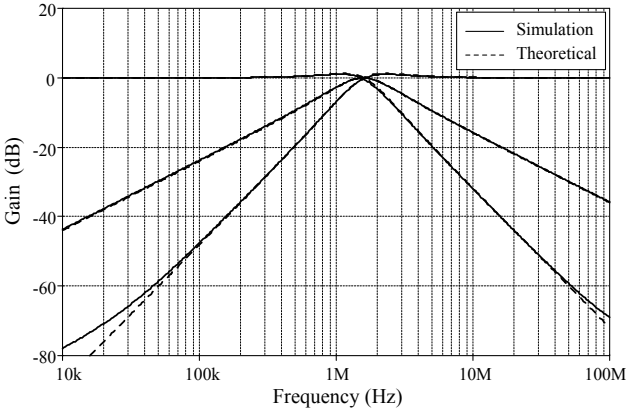

Fig. 6. Frequency responses of LP, BP and HP for the proposed biquad in Fig. 3.

In order to investigate a time-domain response of the proposed voltage-mode multifunction filter, a 1.6-MHz sinusoidal input voltage with 200 mV peak is applied to the filter. The results obtained are shown in Fig. 7, where the dotted and solid lines denote the ideal and simulated responses, respectively. It can be measured from simulations that in case of BP response the total harmonic distortion (THD) of about 0.38% and the total power consumption of about 0.83 mW are obtained. Similarly, the variation of the THD versus the applied sinusoidal input voltage for the BP response at f_0 = 1.6 MHz and f_0 = 3.18 MHz are also shown in Fig. 8. The THD values of the circuit remain below 1.5% for sinusoidal input signals up to 1 V peak.

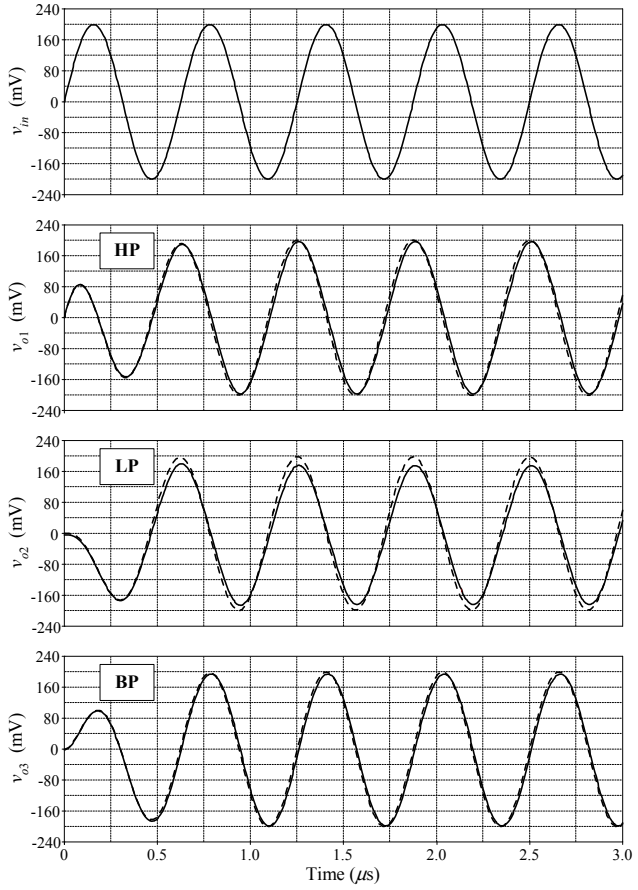

Fig. 7. Input and output waveforms of the HP, LP and BP responses for a 1.6-MHz sinusoidal input voltage of 200 mV (peak).

To evaluate the voltage swing capability of the proposed circuit, the DC analysis is performed. Fig. 9 reports the voltage transfer characteristics from a given input voltage (v_{in}) to the output voltage of the LP filter (v_{o2}), when v_{in} is swept from -1.0 V to 1.0 V. It is evident that the dynamic range for the circuit is reduced to about 85% at high input signal of ±1 V.

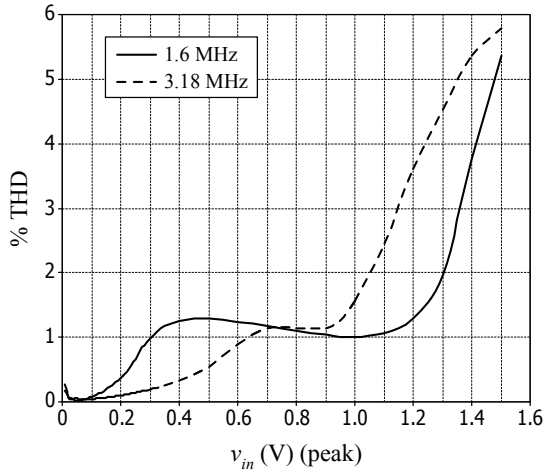

Fig. 8. THD variation of the BP response against an applied input voltage amplitude.

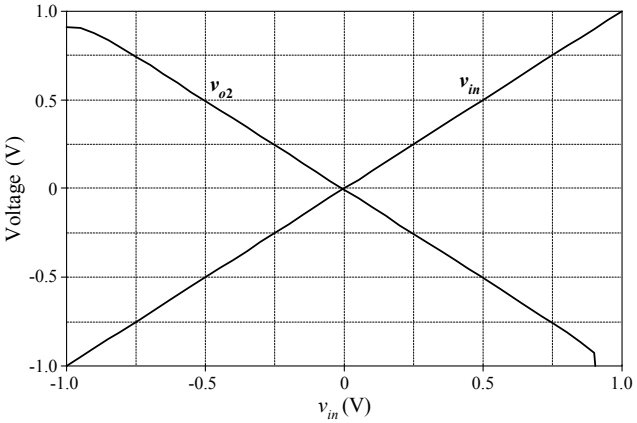

Fig. 9. Simulated DC voltage transfer characteristics of the LP filter.

7. Integration Aspect

In practice, an important aspect to be considered is the feasibility of integrating the proposed circuit given in Fig. 3. Since the DDCCTA active element is implemented in CMOS technology, the passive elements in form of resistor and capacitor should also be compatible in CMOS technology. For this purpose, the grounded resistor can be easily replaced by the simple realization of the active-MOS electronic resistor [21]. Also note that the circuit has the major advantage of using grounded capacitors, which can easily be implemented by using advanced integrated circuit technologies [11]. Therefore, by using grounded resistor and capacitors, the proposed circuit configuration is quite suitable for integration in CMOS technology.

8. Conclusion

In this paper, a single-input three-output voltage-mode multifunction filter for simultaneously realized LP, BP and HP responses without changing the configuration and requiring extra active component has been presented. The presented circuit uses one DDCCTA, one grounded resistor and two grounded capacitors, which is a canonical structure and suitable for integration. It has high-input impedance, and exhibits electronic controllability of both ω_0 and Q through the bias current of the DDCCTA. Also, no critical component matching conditions are required. Both its active and passive sensitivities are low.

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