DRM Transmitter with FPGA Device

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Abstract. *This paper presents the design and analysis of the OFDM modulator for Digital Radio Mondiale (DRM) standard. Attention is paid to the digital signal processing in FPGA devices. The system performs carrier modulation of the complex envelope of the DRM signal. It generates a phase modulated carrier and a magnitude signal that are used with a Pulse Step Modulation (PSM) transmitter. The system has been implemented by using VHDL language. Altera FPGA development kit with an additional board is used and functional tests and measurements are presented. Simulations evaluating the quality of the output signal were done.*

Keywords

OFDM, FPGA, modulator, DRM, digital signal processing.

1. Introduction

The goal of this project is the design of the DRM system [1] modulator. DRM is standard for digital radio broadcasting at frequencies below 30 MHz and is based on the OFDM modulation. The modulator uses a conventional medium-waves AM transmitter for RF generation. Modern high-power AM transmitters have switching amplifiers where the carrier is generated by an oscillator and is modulated by a signal from a modulation input. This means the designed modulator has to generate two signals: One is the magnitude signal that is connected to the modulation input of the transmitter. The other is the phase modulated carrier that replaces the original oscillator of the transmitter. Multiplication of these signals is performed by the AM transmitter. The system can now work with PSM transmitters and the functionality can be extended to other types in the future.

The paper is organized as follows. The principle of the signal generation is shown in Sec. 2.1. Sec. 2.2 and Sec. 2.3 describe the signal processing performed in the system. Hardware platform is described in Sec. 2.4 and 3. Sec. 3 presents also the measurement of the system at work.

2. Modulator Design

2.1 Basic Principles

This section shows the operations of the modulator. First, each OFDM symbol is set up in the frequency domain. The cells (OFDM sub-carriers) are modulated according to the DRM specification [1]. The discrete signal in the time domain is computed by IDFT and can be expressed as

$$\tilde{s} = \sum_{l} \sum_{k=0}^{N_u-1} x_{l,k} e^{j\frac{2\pi}{N_u}k\left(n-N_g-lN_s\right)} \upsilon_{rec1}\left(n-lN_s\right) \tag{1}$$

where υ_{rec1} means the rectangular pulse, $x_{l,k}$ is a data symbol of the l^{th} OFDM symbol and the k^{th} sub-carrier and N_u, N_s and N_g presents the number of samples per useful part, per symbol and per guard interval. The length of IDFT has to be chosen so that the sampling frequency of the signal was 12 kHz (the elementary period defined by the DRM specification is 83 $^1/_3$ μs). This corresponds to the IDFT lengths of 288, 256, 176 and 112 for DRM modes A, B, C and D respectively. Then it is necessary to insert the cyclic prefix for each symbol. If the length of IDFT is multiplied by 2 or 4, the sampling frequency changes to 24 or 48 kHz, respectively. This can be useful when considering an interpolation that follows. It is also necessary to use the sampling frequency of 24 or 48 kHz if we want to use the DRM signals with double channel bandwidth (18 or 20 kHz).

The next task is to convert the complex envelope of the signal into RF. It is important to keep in mind the usage of classical AM transmitter with inputs of carrier wave and modulating signal. Transmitted signal can be expressed as follows:

$$\begin{aligned} s(t) &= \Re\left[\tilde{s}(t)e^{j\omega_c t}\right] = \Re\left[A(t)e^{j\varphi(t)}e^{j\omega_c t}\right] = \\ &= A(t)\Re\left[e^{j(\omega_c t+\varphi(t))}\right] = A(t)\cos\left(\omega_c t+\varphi(t)\right) \end{aligned} \tag{2}$$

where $s(t)$ is the output RF signal, $\tilde{s}(t) = A(t)e^{j\varphi(t)}$ is the complex envelope of the OFDM signal and $\omega_c = 2\pi f_c$ is the frequency of the carrier. As you can see from the right side of the expression (2), the phase modulated carrier

$\cos(\omega_c t+\varphi(t))$ is amplitude-modulated by the shifted signal $A(t)$. Therefore phase modulated carrier $\cos(\omega_c t+\varphi(t))$ and magnitude signal $A(t)$ serve as a source for AM transmitter. This means, it is necessary to compute the complex envelope of the OFDM signal in polar coordinates (signals $A(t)$ and $\varphi(t)$).

The expression (2) is written for the continuous time and shows only the principle of the function. For the discrete time domain the expression (2) changes to

$$s(n) = A(n)\cos\left(2\pi\frac{f_c}{f_s}n + \varphi(n)\right) \tag{3}$$

where f_s is the output sampling frequency of the system. Frequency f_s has to be high enough for carrier generation, therefore the signal $\varphi(t)$ should be interpolated from 12 kHz to this frequency. The interpolation has to be carried out with the signal in rectangular coordinates, and the conversion to polar coordinates has to be done at the output sampling frequency. It is not possible to do this in the reverse order because the obtained signal would not be correct.

The important operations of the DRM transmitter can be summarized as follows:

- Set up an OFDM symbol according to the DRM specification.
- Calculate IDFT for each symbol in order to obtain a complex envelope signal in the time domain.
- Insert the cyclic prefix according to the DRM specification.
- Interpolate the signal in order to achieve the sampling frequency of the modulator.
- Convert the signal from rectangular to polar coordinates.
- Generate a phase-modulated carrier.
- If PSM is used, encode the magnitude signal into amplifier switching signals (will be explained in Sec. 2.4).

It was decided to implement steps 1-3 in a processor and steps 4-7 in FPGA. The reason for this decision is that step 2 - computation of IDFT – would be too difficult to implement in FPGA because of the variable length of IDFT (288, 256, 176 and 112 points). In contrast, steps 4-7 can be easily made in a low cost FPGA, but are too complex for a processor because of a high sampling frequency. For steps 1-3 a personal computer is used. It enables us to generate and save signals with all types of modulation and to use very fast FFT library FFTW [3] for the IDFT computation. A block diagram of the proposed system can be seen in Fig. 1. The system consists of three parts. The generation of the DRM signal is described in Sec. 2.2. Modulation process in FPGA is shown in Sec. 2.3. Finally Sec. 2.4 describes PSM transmitter.

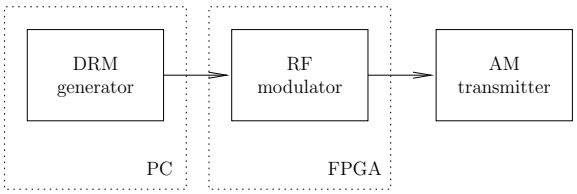

Fig.1. Block diagram of the system.

2.2 Signal Processing in PC

This section focuses on the generation of the DRM signal. Computer based on x86 processor running GNU/Linux OS was used for this. The reasons for the choice of this architecture were:

- easy and fast development in the C language,
- usage of FFTW library [3],
- multitasking environment and easy inter-process communication,
- easy and fast error debugging,
- possibility of loading signals into MATLAB and trying the signal reception in a software DRM receiver.

The DRM signal consists of three logical channels: the Main Service Channel (MSC), the Fast Access Channel (FAC) and the Service Description Channel (SDC). Each channel transfers different types of data, occupies predefined cells in OFDM symbol and uses different mappings (4-QAM, 16-QAM or 64-QAM). The work has focused on implementing the mapping of the pilot signals and the coding and mapping of FAC and SDC channels, which is sufficient for performing system tests.

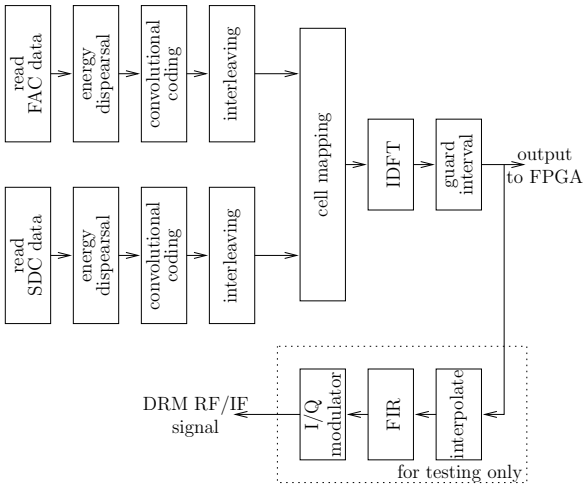

Fig. 2. Blocks of transmission system implemented in the C language.

Fig. 2 shows the block scheme of implemented parts. The blocks have been fully programmed in the C language with a floating-point arithmetic. Each block runs as a separate process with the inter-process communication implemented using UNIX half-duplex pipes, which is convenient for testing and debugging purposes.

The description of particular blocks follows. Block named “read FAC/SDC data” reads the FAC/SDC data from a file stored on disk, adds CRC checksum and periodically sends the constructed message to the output. Block “energy dispersal” generates a pseudo-random binary sequence and computes modulo-2 addition with input data. Blocks “convolutional coding” and “interleaving” continue with channel coding as described in the DRM system specification. The most important thing about OFDM symbol creation is done by the “cell mapping” block. It generates pilot signals and places them to appropriate cells. Data cells - FAC, SDC and MSC - are also mapped in this block. MSC cells are mapped randomly, which is sufficient for measuring parameters such as MER and BER. The array containing all cells is sent to the block “IDFT” where inverse discrete Fourier transform is calculated. The symbol is converted to the time domain in this way. Finally, OFDM symbol is obtained by inserting a guard interval as a cyclic repetition of a portion of the signal.

The first test focuses on verifying the correctness of the generated signal. The generated signal was successfully decoded by a software DRM receiver. For this test, additional blocks were used in order to modulate complex envelope on carrier. The modulation was carried out by direct I/Q modulator, the signal was saved into a file and fetched directly to the DReaM software [4] (an open source implementation of DRM receiver).

2.3 Modulator in FPGA

In Sec. 2.1 the modulation processes provided by FPGA were described. The complex envelope of the DRM signal is generated by PC as described in Sec. 2.2. This signal is fed into FPGA by using USB and is converted and phase-modulated as described in Sec. 2.1. The block diagram of the modulator can be seen in Fig. 3.

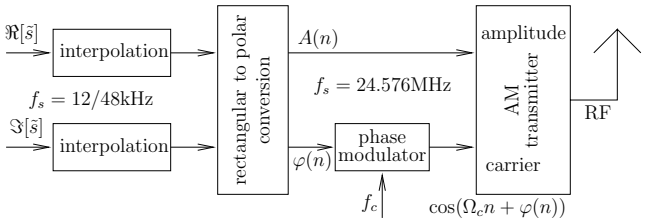

Fig. 3. Block diagram of the modulator.

First, the input signal is interpolated. It is necessary since the input signal has sampling frequency of 12, 24 or 48 kHz and is used for modulation of a carrier with DDS running on 24.576 MHz. Sampling frequency of the DDS was chosen as the power-of-two-multiple of the input sampling frequency. The interpolation structure can be seen in Fig. 4.

In order to achieve such a high interpolating rate CIC filters are used. CIC filters have very simple structure and high efficiency but also quite large band-pass droop [5]. To minimize the band-pass droop of CIC filters the FIR filter with interpolating rate of 4 is inserted. It uses a raised cosine pulse.

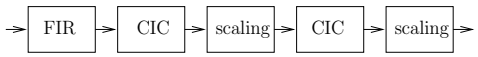

Fig. 4. Interpolation structure.

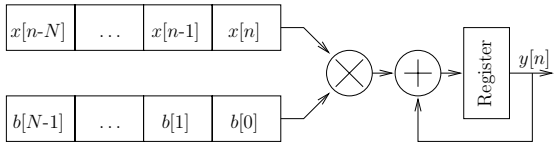

Fig. 5. Serial FIR filter.

Fully serial structure of the FIR filter was chosen, as seen in Fig. 5, because the sampling frequency of the filter is quite low. Multiplier and adder of this structure have to work at *N*-times higher frequency than the input sampling frequency is (*N* is a number of taps of the FIR filter). This is very efficient for filters with low sampling frequency, because we need only one multiplier and one adder and thus efficiently share the computational time of these blocks.

It is important for hardware implementation of the CIC filters to consider their gain. It can be written as

$$G = (RM)^N \tag{4}$$

where *R* is an interpolation rate of the filter, *N* is the filters order and *M* is a parameter called differential delay [5].

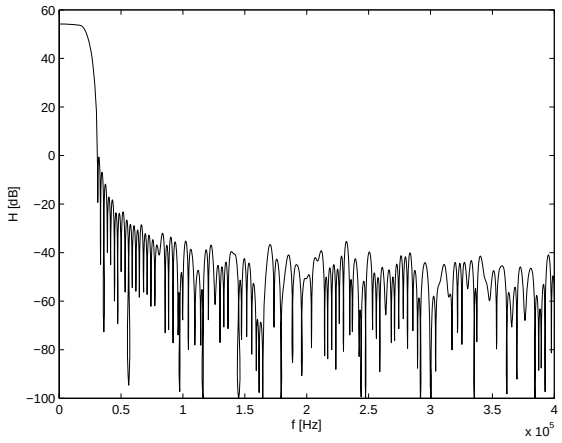

Fig. 6. Frequency response of the whole interpolation structure in the frequency range to 400 kHz (f_s = 24.576 MHz).

Because of this gain, additional guard bits in comb and integrator stages are added and each CIC filter is followed by a scaling block. It has to be kept in mind that the gain is a function of rate change *R*. Interpolation rates of both of the stages can be easily changed when changing the input sampling frequency between 12, 24 or 48 kHz. Fig. 6 illustrates the frequency response of the whole interpolation structure in the frequency range to 400 kHz (f_s=24.576 MHz).

Next, the interpolated signal is converted from rectangular to polar coordinates. It is performed by CORDIC algorithm working in vectoring mode [6]. Two basic structures are used to implement CORDIC architecture: state machine with iterative computation or a fully pipelined

processor. The fully pipelined structure has been used to fulfill the real-time requirements of the DRM modulator.

The DDS generates a phase modulated carrier for a transmitter. When we consider DDS where the angle 2π corresponds to the maximum value of the phase accumulator 2^{N_p} (the accumulator uses unsigned N_p-bit integer), the input value of DDS's sine generator Θ can be written as

$$\Theta(n) = \left(2^{N_p} \frac{f_c}{f_s} n + 2^{N_p} \frac{\varphi(n)}{2\pi} \right) \bmod 2^{N_p} \tag{5}$$

where $2^{N_p} \frac{f_c}{f_s}$ is the frequency tuning number of the DDS. Transmitters usually use binary logic gate input for a carrier, therefore DDS need not generate harmonic signal and it is not necessary to implement sine/cosine function of the phase accumulator. DDS consists of the phase accumulator where 2^{N_p} represents 2π and output is the most significant bit. When the phase is in the interval from zero to π, MSB has the value of logic zero and when the phase is in the interval from π to 2π, MSB has the value of logic 1. In the case of such a simple DDS the low sampling frequency causes high error in the phase of the carrier signal.

2.4 PSM Transmitter

The system is designed to work with all types of AM transmitters, but special attention is paid to the usage of the PSM technique (sometimes called Digital Amplitude Modulator). Its structure can be seen in Fig. 7. In the PSM transmitter, several amplifiers are used. The number of switched-on amplifiers specifies the level of the output signal. In this case, 2^N amplifiers would be needed to achieve *N*-bit resolution. Therefore amplifiers with unit gain (1×) and also amplifiers with fractional gains (½×, ¼×, ⅛ × etc) are used. Bit resolution of such a system is

$$N_{total} = \log_2 (N_{unit} + 1) + N_{frac} \tag{6}$$

where N_{unit} is the number of unit gain amplifiers and N_{frac} is the number of fractional gain amplifiers. Amplifiers are followed by a low-pass filter to remove high order harmonic waves. The structure brings high efficiency and the advantage of digital-only signal processing in the system. Digital to analog conversion is made at the latest point possible - by the summation of amplifier outputs. The system works as a power DAC. More information about the design of the PSM transmitter and about the used one can be found in [7].

Another block, that is implemented in FPGA, but is not shown in the block diagram in Fig. 3, is an encoder for the PSM transmitter. Magnitude signal expressed in binary form has to be converted into the code that controls particular amplifier stages of the PSM transmitter. It is convenient to rotate amplifiers to assure uniform usage of the unit gain stages. Gain stages should be switched only once per carrier period.

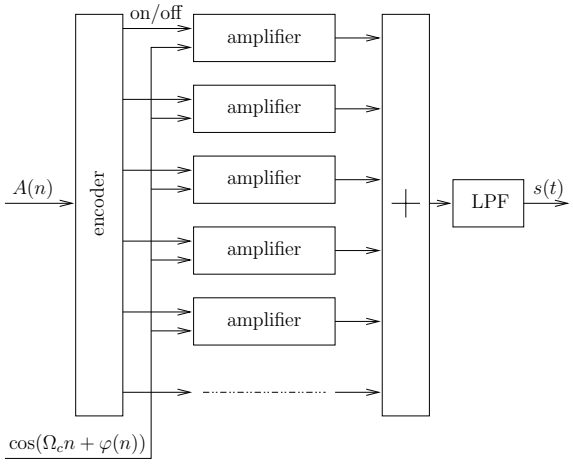

Fig. 7. Block diagram of the PSM transmitter.

3. Simulations and Implementation

Several simulations were done using MATLAB before the implementation. The signal, that was generated as described in Sec. 2.2, was loaded to MATLAB and the function of the modulator in FPGA was simulated. Output RF signal, generated by the simulation, was numerically down-converted and received by a software receiver. Signal processing in a fixed-point arithmetic was simulated and the quality of the output signal was evaluated. The quality of the signal was evaluated by MER (Modulation Error Ratio) parameter and it was observed, if the signal spectrum fulfills the frequency mask defined by [2]. The MER parameter is defined as

$$MER = 10 \log_{10} \frac{\sum_{j=1}^{N} \left(I_j^2 + Q_j^2 \right)}{\sum_{j=1}^{N} \left(\delta I_j^2 + \delta Q_j^2 \right)} \tag{7}$$

where δI_j and δQ_j represent the error vector and *I* and *Q* are the corresponding positions of the received symbol in the constellation diagram. The minimum value of MER parameter for DRM signal is 30 dB, as defined in [2].

Simulations evaluating the impact of the number of bits expressing particular signal paths were shown in [8] and [9]. Simulation showed that 8 bits are sufficient for the magnitude signal and 9 bits for the phase signal. The output spectrum was also analyzed and MER was evaluated as the function of the sampling frequency of rectangular to polar conversion. It was found that the sampling frequency of the conversion has to be at least 350 kHz [10]. It was verified during all the simulations that the output signal is a valid DRM signal and can be received by a DRM receiver.

The blocks of the modulator were written in VHDL. No FPGA IP (Intellectual Property) core is used, the program consists of author's handwritten VHDL only. The function of the whole modulator was verified in a VHDL simulator in the same manner as in MATLAB, as described above.

The hardware is based on Altera FPGA development kit with APEX 20KE200 device. An additional expansion board has been designed and constructed for the kit. It includes a USB/FIFO converter for transferring signal from PC, an oscillator with frequency 24.576 MHz, an interface for connecting to experimental PSM MW transmitter [7] and an audio codec. The frequency of the on-board oscillator was chosen as the power-of-two-multiple of the input sampling frequency. The audio codec can be used for future experiments with receiving DRM or as a magnitude signal output for other types of transmitters. The development kit with the additional board can be seen in Fig. 8.

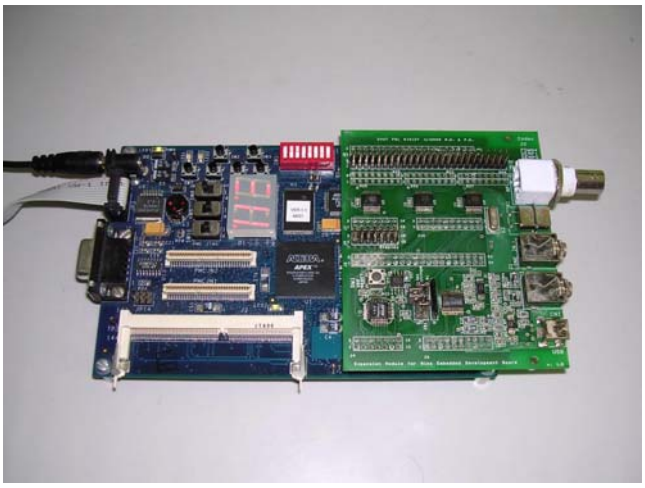

Fig. 8. FPGA development kit with the additional board.

The VHDL code used for the simulation was compiled and loaded to the FPGA device, including additional block functioning as a driver for USB/FIFO converter. Sampling frequency of DDS and CORDIC is equal to the oscillator frequency and is as high as possible for the design in this FPGA device. In the future, the design will be optimized and tested in a faster device, in order to increase the sampling frequency of DDS and to improve the quality of the output signal.

Measurements of the system were performed. Fig. 9 shows the output RF spectrum displayed by a spectrum analyzer. Fig. 10 shows the constellation diagram of the DRM signal displayed by the DReaM software [4]. MER of the received signal was 31 dB (measured by the DReaM software). Measurement is described in detail in [11].

4. Conclusions

The proposed system was able to perform the modulation of the complex envelope of the DRM signal and to generate the signals for the use with a PSM transmitter. Algorithms suitable for FPGA were used and implemented in the VHDL language. The system was constructed and tested with experimental PSM MW transmitter. Evaluated MER in the receiver was 31 dB which satisfies the DRM specifications [2].

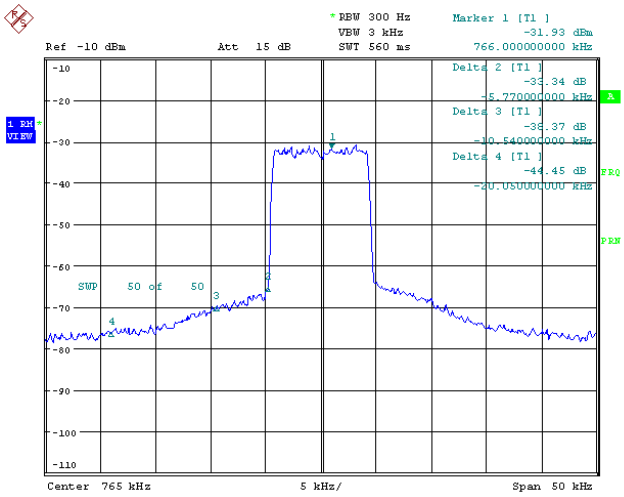

Fig. 9. Output spectrum.

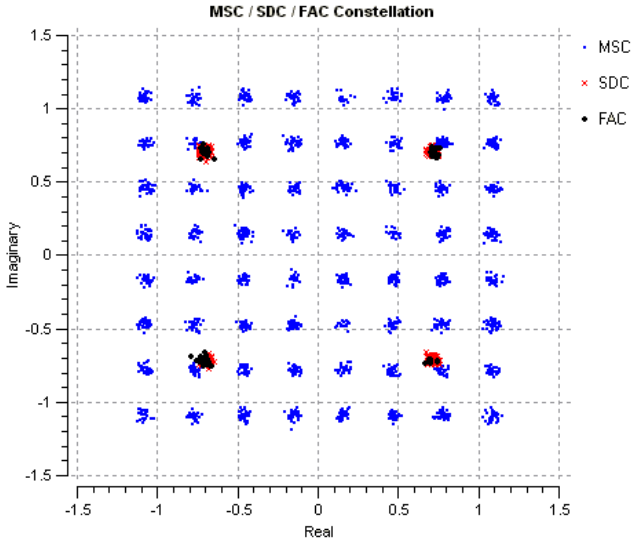

Fig. 10. Constellation diagram received by the DReaM software.

Acknowledgements

This research work has been supported by the research grant GACR (Grant Agency of the Czech Republic) No. 102/03/0451 “Radio and television systems using modulation OFDM”.

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