TCAD - A PROGRESSIVE TOOL FOR ENGINEERS

J. Vobecký, J. Voves, P. Hazdra
and I. Adamčík
Department of Microelectronics
Faculty of Electrical Engineering,
Czech Technical University in Prague

Abstract

The semiconductor industry is continuously striving to improve the performance of electron devices and circuits. It implies the need for better understanding of their basic behaviour. However, the miniaturization and complexity of devices led to a breakdown of the analytical models. As a consequence numerical analysis and simulation based on fundamental differential equations has become necessary.

1. Introduction

Contemporary simulation of semiconductor devices has attained such a high level of sophistication that numerical analysis of semiconductor devices became a basic methodology of research and development engineers. Nevertheless, one must not expect that people using computer programs as numerical analysis tool are specialists considering the complexity of assumptions, algorithms and implementation details of the programs they use. At present, one can utilize the support of software firms, like Technology Modeling Assoc. or Silvaco, both from USA, in order to purchase outstanding and users-friendly simulation tools that are being continually updated and enhanced.

The aim of this paper is to present both the principle and capabilities of Technology Computer Aided Design tools to be widely used in practice up to this time. Because there are so many options to choose from, the paper respects the present disposal of the Department of Microelectronics. Consequently, various ways, in which physically-based simulation can assist a wide range of engineering tasks, will be illustrated on the basis of products from SILVACO International.

2. Technology CAD

Technology Computer Aided Design (TCAD) comprises tools for predicting the performance of electronic devices and circuits. TCAD encompasses activities such as process, device and circuit simulation, parameter extraction, device modeling, etc.. They reduce new product development costs, shorten development times, and help maintain process control in production environments. Simply said, TCAD makes it easier for engineers to do their job. It is estimated that process and device simulation can reduce the number of developmental engineering runs from an average twelve to three, thereby reducing costs four times, while time can be reduced two or three times. This is the reason why a term "virtual wafer fab" is being used to briefly characterize the present TCAD capabilities.

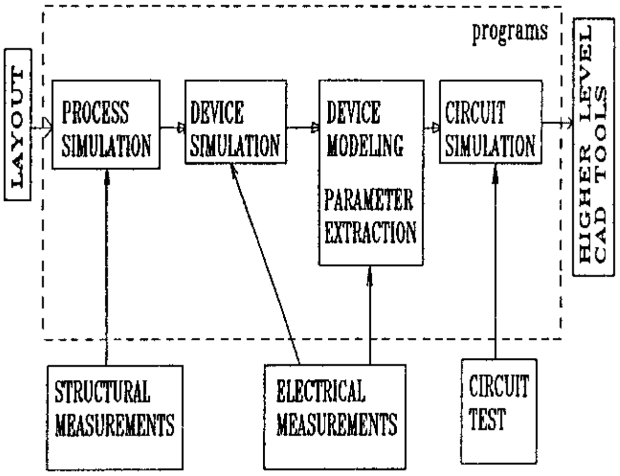

Fig. 1
TCAD flow-chart.

Fig.1 shows how TCAD tools form an integrated link as well as the feed-forward information flow between TCAD activities [3]. The link begins at the unprocessed silicon level. Process simulation predicts the physical structure that results from a sequence of processing steps applied to an initial structure. Subsequent device simulation predicts the electrical characteristics of a specified structure that was formed during process simulation such as I-V curve, output characteristics, transient behaviour, etc.. Circuit simulation that might be combined with device simulation in so called mixed-mode, predicts the electrical characteristics associated with combinations of connected devices. Another way how to couple device and circuit simulation exists through the parameter extraction which determines the coefficients required for a device model to be applicable to a particular device. In other words, the parameter extractor compiles the results of device simulator and creates a model for subsequent use by the circuit simulator. Other way leading to the parameter extraction process is via electrical measurements which enables us accurate statistical modeling if a collecting of significant amount of device model data preceeded. The goal of the following paragraphs is to illustrate the above mentioned steps.

It is worth concluding this paragraph by mentioning that, nowadays, the best TCAD systems comprise powerful environment that design simulation based experiments, generate input decks, submit runs, store and analyze results. These capabilities make it extremely easy for engineers to perform large simulation-based experiments that mirrors existing experimental procedures.

2.1. Process Simulation

Process simulation predicts the stucture of devices, that result from defined sequences of processing steps. It is performed by solving equations that represent the physics and chemistry of the situation. The most versatile and accurate semiconductor process simulator available today is SUPREM-4. This is because there are implemented sophisticated physical models for ion implantation, oxidation and diffusion, which has been carried out by leading development group worldwide. SUPREM-4 can simulate a structure consisting of any number of non-planar layers, each of which is composed of one material [1]. Seven materials are defined by default, i.e. silicon, polysilicon, SiO_2, Si_3N_4, oxinitride, aluminium and photoresist. The following elements are default when implanted, diffused or deposited: boron, phosphorus, arsenic and antimony. A structure may be doped with up to 30 impurities. The program also models the generation, diffusion and recombination of point defects (interstitials and vacancies) in silicon layers, as well as the diffusion in oxides. Finally, numerical diffusion and oxidation models enable us to accurately simulate arbitrary device structures under most processing conditions.

Fig.2 shows the application of SUPREM-4 on PC platform. The process (as well as device) simulator calculate values of solution variables at discrete points. These points form the nodes of a mesh. Fig.2 illustrates such mesh for a power diode which serves as the testing structure for investigation of high- energy low-dose ion irradiation on electron devices. One can see that the method of final elements is applied as the most powerful one. Beside the mesh specification the input deck of SUPREM-4 contains technology description. In the example presented it comprises processing steps roughly described as follows: wet oxidation (1080 °C, 3.5 hours), local oxide etching, phosphorus (10^{16}/ 150keV from the back side) and boron (10^{16}/ 100keV) implantations, furnace annealing (800 °C, 2 hours). Fig.3 shows the resulting doping profile (both the donors and acceptors in logarithmic scale) of the device which corresponds to the mesh from Fig.2. On the left side the doping of the p^+-anode is interrupted ($x = 0 - 5\,\mu m$, $y = 0\,\mu m$). This is because the real test structure is a 3 inch wafer with the matrix of individual diodes. Because of symmetry one half of the individual diode is enough to simulate (see Fig. 2). On the right side of the figure, the n^+-cathode is located as a part of all the wafer contact. The doping profile shown provides the data for input deck of the device simulator PISCES-2B which is described in the following paragraph.

2.2. Device Simulation

Device simulation predicts the electrical behaviour of semiconductor structures by solving coupled, nonlinear, partial differential equations that describe the physics of device performance. The fundamental equations are Poisson equation solving the relationship between electrostatic potential and charge density, and charge carrier continuity equation reflecting the fact that sources and sinks of the conduction current are fully compensated by the time variation of the mobile charge. If we desire an account for the temperature changes and its distribution in the interior of a device, the heat-flow equation comes into account. Auxiliary equations relate the carrier velocities to the electric field vector and to the carrier concentration. They can vary considerably, depending on the features that is the simulator equipped by. The equations are solved for DC, time-domain transient or small-signal conditions. A number of spatial coordinates determine whether a simulator is one- two- or three-dimensional. Two-dimensional simulators are most popular ones because of good compromise between time consumption and applicability/validity of results.

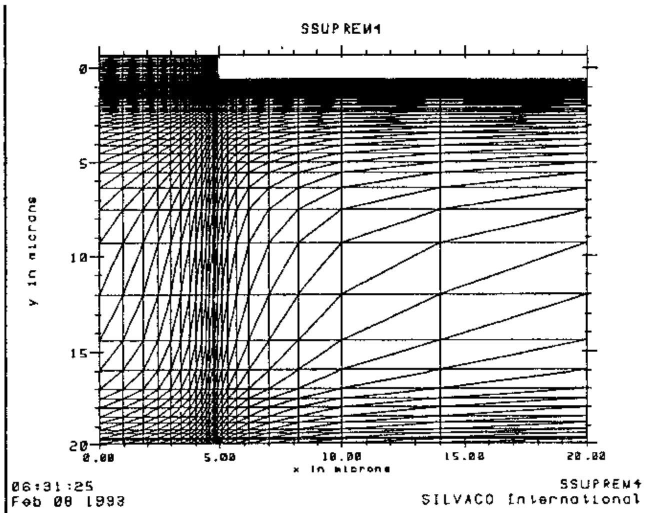

Fig. 2
2-D mesh for the diode test structure

Herein is presented the application of the 2-D device simulator PISCES-2B, to be utilized in PC platform, that has worldwide been proved to be most useful. PISCES-2B solves basic semiconductor equations on non-uniform triangular grids [2]. The structure of the simulated device may be completely arbitrary [2]. Doping profiles within the device may be obtained from either analytical functions, experimentally measured data, or process modelling programs SUPREM-3 and SUPREM-4. State-of-the- art physical models are used for accurate simulations (SRH and Auger recombination, impact ionization, mobility models, etc.). The simulator allows to: - investigate MOS and SOI devices (bipolar effects, latch-up phenomena, modeling of gate and substrate currents, parasitic capacitances, hot electron and punch-through effects, etc...), - design and analyze CCDs, photodetectors, and solar cells (multilayer reflections, quantum efficiency for conversion of absorbed photons, spectrum vs. wavelength relations, complex refractive index, dc or transient illumination of chosen intensity from the top or bottom of the device through a variable window may be taken into account), - simulate submicron devices using sophisticated mobility models - predict breakdown in various devices, analyze impact ionization effects and avalanche breakdown, - evaluate the behaviour of bipolar-MOS devices

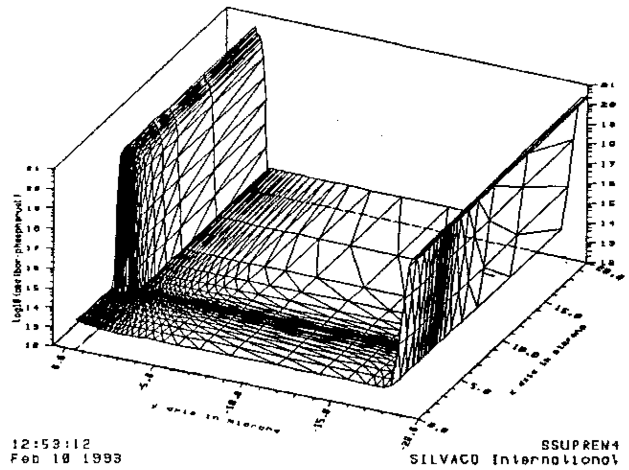

Fig. 3
The doping profile of the diode test structure provided by technological simulator SUPREM-4 for the device simulator PISCES-2B.

(IGBT, smart power circuits), - analyze switching of high-speed and/or high-power thyristors and diodes, etc.. The above described linking between process and device simulator (see Fig.1) is illustrated by means of the link between SUPREM-4 and PISCES-2B. The doping profile and mesh specification of the diode structure to be created by SUPREM-4 (see Fig.3) enters PISCES-2B input deck. Beside the doping and mesh, there are specified electrical contacts, material parameters, physical models, boundary conditions and methods for solving the differential equations, and finally, magnitudes of voltage or currents on electrodes for dc, transient or ac analysis. Fig.4 shows the result of dc analysis for the diode structure with geometry and doping according Fig.2 and 3. The diode is forward biased (1.05V) and the spatial distribution of recombination rate is plotted as an example. This parameter is interesting because, as was mentioned above, the diode is subjected to low-does high- energy ion irradiation. The ions are stopped within the silicon at the depth determined by their energy. They create most of the lattice damage towards the end of their range, enabling localization of the region with high defect concentration, i.e. with greatly lowered minority carrier lifetime, while most of the silicon is left relatively unaffected. The area of greatly reduced lifetime is that one with high recombination rate ($10\,\mu m > y > 4\,\mu m$) on the Fig.4. The influence of its location within the n-base and the geometry of the p$^+$-anode on the recombination rate distribution is clearly visualized.

2.3. Circuit simulator

Circuit simulators such as fairly well known SPICE solve systems of equations that describe the behaviour of electrical circuits. Terminal characteristics of the devices that are of interest are approximated with good accuracy in so called compact models. These models have been developed with the aid of device characterization and parameter extraction (see Fig.1). Circuit simulation is very popular because it provides good accuracy with minimum complexity and reasonable CPU time. However, for many purposes it has some limitations. Typical applications not satisfactorily covered by compact models include high frequency, high power and optoelectronic devices, thin film transistors, etc.. These limitations may be overcome by using mixed device and circuit simulators, i.e. the above mentioned mixed-mode [3]. In the mixed-mode, an inaccurate compact model of some device contained in a circuit may be replaced by the device simulation to predict the device behaviour. The rest of the circuit is treated using usual circuit simulation. It means that some circuit elements are described by compact models, and some by models based on device simulator. Consequently, the approximation errors introduced by compact models can be avoided. The cost is increased CPU time and necessity to use a workstation platform. This is the reason why any demonstration is not presented here.

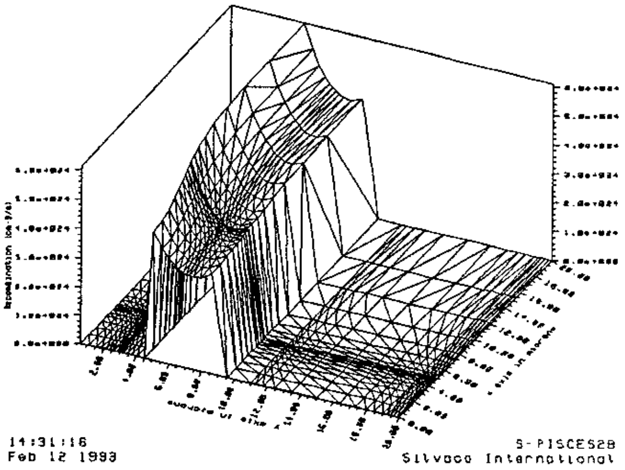

Fig. 4
Spatial distribution of the recombination rate of the diode test structure under high-injection conditions (provided by PISCES-2B.

3. Conclusions

Technology Computer Aided Design (TCAD) helps solve development problems while minimizing the need for trial-and- error experimentation. TCAD helps the engineer make decisions before structures are even built. Finally, TCAD allows engineers to investigate internal device behaviour that otherwise may not be possible, while providing a simulation link between the circuit layout representation and circuit simulation. TCAD software has become a worldwide technological standard. Majority of renowned universities have accepted TCAD into their educational plans. Department of Microelectronics, Czech Technical University of Prague, is the first body within the Czech Republic, that has purchased and utilized TCAD tools for both the scientific and pedagogic purpose. Consequently, the undergraduate students as well as postgraduate students entering the Department have opportunity to reach practical skills in the application of TCAD. It is expected that due to the attractive subject some new scientific collaborations will be established. We all approach the TCAD tools with high expectations.

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About authors:

Jan Vobecký was born in Prague in 1957. He graduated in Electrotechnology from the Faculty of Electrical Engineering, CTU in Prague, in 1981. He received PhD. degree in 1988 and Associate Professor degree in 1992. He is the author of more than 20 technical papers and 4 printed lectures for students. Nowadays, he is the manager of research groups at the Dept. of Microelectronics, CTU in Prague. His research activities are oriented towards diagnostics and simulation of power devices and ICs. He is a member of IEEE.

Jan Voves was born in Prague in 1960. He received the MSc.and RNDr. degree in physical electronics and optics from the Faculty of Mathematics and Physics, Charles' University of Prague in 1984. From 1984 he was a research fellow in the Department of Microelectronics, Faculty of Electrical Engineering, CTU of Prague, working on the electrical characterization of ion implanted doping profiles in semiconductors. From 1987 he is an Assistant Professor at CTU in Prague. His research interests are in the area of device simulation, especially on application of the Monte Carlo Method.

Pavel Hazdra was born in Prague in 1960. He received MSc. and PhD. in microelectronics from CTU in Prague. In 1987 he joined the staff of the Department of Microelectronics, CTU Prague, as an Assistant Professor. His research has focusedon semiconductor defect investigation and their characterisation by means of electrical methods (DLTS). Since 1992 he has managed the project in defect engineering and the Electron Device Group. He is the author of over 20 scientific and technical papers.

Ivan Adamčík was born in 1937. He graduated from the Faculty of Electrical Engineering, STU Bratislava. He received PhD. degree in 1973. From 1961 to 1990 he was working in TESLA Research Institute in Prague, in the field of IC design and testing. In 1990 he became the Head of Dept. of Microelectronics, CTU in Prague. As an Associate Professor he is teaching microelectronics & IC design. He is the author of about 50 technical papers, 12 patents and two printed lectures for students.

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