

Performance Analysis of 8-bit ODACs for VLC Applications

Ales DOBESCH¹, Mónica FIGUEIREDO^{2,3}, Luis Nero ALVES^{2,4}, Otakar WILFERT¹

¹ Dept. of Radio Electronics, Brno University of Technology, Technicka 3082/12, 616 00 Brno, Czech Republic

² Instituto de Telecomunicações, Campus Universitário de Santiago, 3810-193, Aveiro, Portugal

³ Instituto Politécnico de Leiria, Rua General Norton de Matos, 2411-901 Leiria, Portugal

⁴ Universidade de Aveiro, Campus Universitário de Santiago, 3810-193, Aveiro, Portugal

dobesch.ales@phd.feec.vutbr.cz, monica.figueiredo@ipleiria.pt, nero@ua.pt, wilfert@feec.vutbr.cz

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Abstract. *A discrete optical power level stepping technique in visible light communication (VLC), also known, as an optical digital to analog conversion (ODAC) has been proposed. This is an alternative concept for VLC front-end design, able to mitigate the LED intrinsic non-linearity. Additionally, it removes the need of an electrical digital to analog conversion (EDAC) in the driver stage. This paper provides an experimental evaluation of two different ODAC front-ends. The results investigate the spatial relation between the optical front-end and the optical receiver. In addition, the performance evaluation employs dynamic test metrics rather than conventional static metrics previously reported in the literature.*

Keywords

LED, VLC, Li-Fi, ODAC

1. Introduction

With the advent of solid-state lighting (SSL), visible light communication (VLC) has become a promising communication technology in the framework of 5G and beyond 5G technologies [1], [2]. The exploitation of light emitting diode's (LED) capability to support fast switching is advancing novel means for combined lighting and communications. LEDs with bandwidths in the range of tenths of MHz are currently able to support communication in the order of Gbit/s [3]. The early VLC IEEE standard in IEEE 802.15.7 [4] is currently under revision with the aim of extending communication means to the so called light-fidelity (Li-Fi) [5].

The optical digital to analog conversion (ODAC) technique was proposed as a suitable alternative of an optical front-end architecture able to mitigate driving impairments of conventional VLC emitters affecting the communication system. Specifically, ODAC-based devices offer better linearity, full LED dynamic range and no need of EDAC in the driver stage [6], [7]. Moreover, large amount

of LEDs inside each ODAC emitter complies with recent trends in general lighting, i.e. multiple LED array design ensuring higher luminous output [8]. An ODAC concept was firstly introduced in [6] employed in infra-red (IR) wireless communication. The ODAC adaptation for VLC applications was introduced in [7]. However, both hardware designs present ODAC implementations with lower bit depths of 5 bits and 4 bits, respectively. In addition, both proposed communication systems employ off line data processing. The very first real time demonstration of an 8-bit ODAC-based indoor VLC system is presented in [9] where the authors reached data rates up to 30 Mbps. In [10], the performance evaluation of a 4-bit ODAC for VLC applications is explored in more details adapting performance metrics commonly used for EDAC. This is obviously inadequate approach as the authors reveal in their contributions [11], [12]. Author's former work presents that the geometrical set-up as well as channel degradation effects play a key role for overall ODAC emitter performance.

This paper presents for the first time an ODAC performance analysis based on experimental work taking into account real ODAC manner. Two ODAC front-ends having different LED array constellations and various active areas sizes are examined. Furthermore, the performance metrics are well suited to credibly evaluate ODAC front-ends performance. Finally, the work analyzes available modulation bandwidth of both ODAC front-ends.

The paper is arranged into the following sections. Section 2 presents test bed description and experimental set-up. Section 3 is dedicated to ODAC performance evaluation. The last Section 4 gives the conclusions.

2. System Description

2.1 Test Bed Description

Figure 1 depicts a conceptual diagram of the experimental set-up. Evaluation board FPGA Virtex6 - ML605

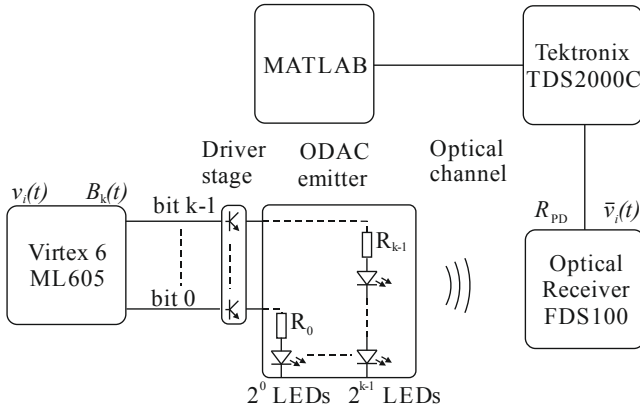


Fig. 1. Experimental system conceptual diagram.

is programmed to generate a signal $v_i(t)$ which is represented by a set of bit streams $B_k(t)$ all having the same amplitude. These digital bit streams drive k independent LED groups in an ODAC emitter array. The transmitted bit streams are merged on the optical channel. Both ODAC front-ends under consideration employ a binary weighted approach as can be seen in Fig. 1. This means that each LED in the ODAC emitter is driven by the same current. Therefore, binary weights are set by the number of LEDs in each group. In case of 8-bit ODAC emitter resolution the number of bit streams as well as the number of LED groups inside the array is equal to $k = 8$. The optical signal impinges the optical receiver where the recovered signal $\bar{v}_i(t)$ is a reconstructed clone of original signal $v_i(t)$. Reconstruction error depends on channel impairments, ODAC quantization error and ODAC distortion error induced by the geometrical set-up between ODAC front-end and the optical receiver. The receiver side uses PIN photo-diode FDS100 followed by an operational amplifier (OPA657) in gain variable transimpedance stage. The recovered signal $\bar{v}_i(t)$ is captured by the scope (Tektronix TDS2000C) and data is imported to MATLAB for further offline signal processing. Since the channel impulse response (CIR) of each LED in the array is given by $h_{m,n}(t)$ the recovered signal $\bar{v}_i(t)$ at the experimental chain end can be expressed by:

$$\bar{v}_i(t) = A_{RX} R_{PD} \sum_{m=1}^k \sum_{n=1}^{2^m-1} B_m(t) * h_{m,n}(t) P_0 + n_0, \quad (1)$$

where P_0 is the optical power corresponding to each LED in the array, R_{PD} represents photodiode responsivity, A_{RX} denotes optical receiver gain and n_0 indicates system noise.

2.2 Implementation

Figure 2 illustrates the hardware implementation of two proposed ODAC front-ends for VLC applications. Specifically, the first ODAC front-end (Fig. 2a) employs conventional discrete blue LEDs encapsulated in a 7.62 mm square package. The second ODAC front-end uses off-the-shelf white LEDs in a PLCC6 housing as depicted in Fig. 2b. The front-ends are made of double layered FR4 PCB, where the top layer is dedicated to the LEDs and the bottom layer to the driving circuits. As both

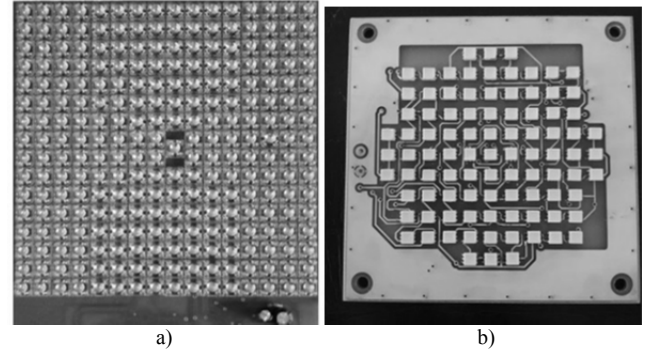


Fig. 2. a) 7.62mm square blue LED ODAC front-end, b) PLCC6 white LED ODAC front-end.

front-ends have 8-bit depth, the overall LED number inside each emitter array is 255 which corresponds to $2^k - 1$. The least significant bit (LSB) is in the array represented by one LED, while the most significant bit (MSB) is formed by 128 LEDs. The first ODAC emitter is formed by 255 LED packages having an active area of 122 mm \times 122 mm. PLCC6 ODAC front-end comprises of 93 PLCC6 LED packages, each containing three LED chips. In order to keep the ODAC's symmetry, the outer LED triplets are placed on a PCB having just one LED chip wired (the central one). Thanks to the PLCC6 surface mount technology, the active area dimensions of the second front-end are reduced to 60 mm \times 60 mm. This supports a better uniformity of the optical intensity displacement in the near field radiation area.

In electrical domain, a BJT NPN transistor switch is chosen as a suitable LED driver circuit with regard to the system complexity and low LED bandwidth. Signals from FPGA are fed into line driver which provides sufficient current for 8 BJT switch blocks driving 8 LED front-end array groups.

3. ODAC Performance Evaluation

3.1 Signal Reconstruction Error

Relative root mean square error E_{RMS} was chosen as an appropriate performance metric able to evaluate signal reconstruction error. Authors in their former work [11], [12] use this performance metric for simulation purposes.

Performance evaluation is based on periodic signals to facilitate comparison between the original and the reconstructed signal version. In this case, a ramp-shaped signal having frequencies of 1 kHz and 98 kHz is used. The normalized versions of $v_i(t)$ generated on the transmitter side and $\bar{v}_i(t)$ captured on the receiver side are considered. It is a prerequisite that the receiver starts processing as the first signal impinges the optical receiver. For performance evaluation purposes it is necessary to consider a delayed replica of the original signal $v_i(t - \Delta t_{min})$ where Δt_{min} is the minimum delay corresponding to the smallest direct path between the front-end and the optical receiver. The root mean square error is then given by:

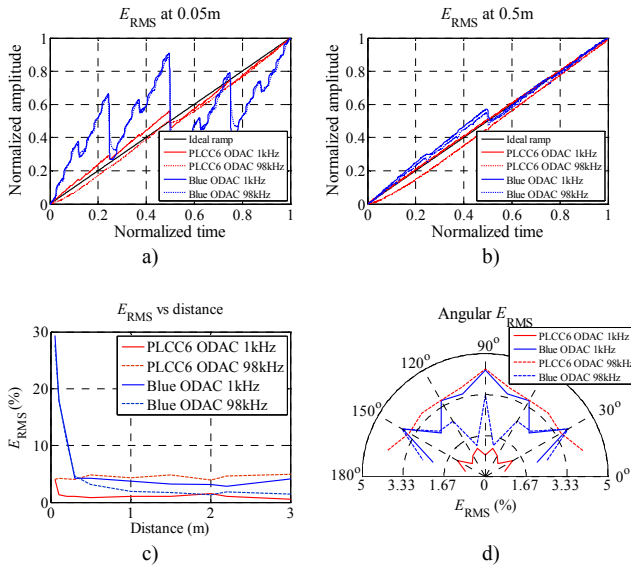


Fig. 3. Reconstruction error: a) E_{RMS} at the distance of 0.05 m, b) E_{RMS} at the distance of 0.5 m, c) E_{RMS} dependent on the distance, d) angular E_{RMS} dependence.

$$E_{RMS}(x, y) = \frac{\sqrt{\frac{1}{T} \int_{\Delta t_{min}}^{T+\Delta t_{min}} (v_i(t - \Delta t_{min}) - \bar{v}_i(t))^2 dt}}{\sqrt{\frac{1}{T} \int_{\Delta t_{min}}^{T+\Delta t_{min}} (v_i(t - \Delta t_{min}))^2 dt}} \quad (2)$$

Figure 3 illustrates reconstruction error of both ODAC samples. Specifically, in Fig. 3a, and Fig. 3b the comparison between normalized versions of the reconstructed signal $\bar{v}_i(t)$ (red and blue curves) and the original signal $v_i(t)$ (black curve) is shown. Blue-colored curves in Fig. 3a illustrate huge E_{RMS} for ODAC emitter employing discrete blue LEDs placed at distance 0.05 m. This excessive error, in percentages 29.33 % and 27.77 % for frequencies 1 kHz and 98 kHz, respectively, is caused by the emitter's higher array dimensions inducing distortion in the emitter near field. In the case of the PLCC6 ODAC emitter, the red-colored curves show typical values of E_{RMS} . Particularly, the E_{RMS} is 4.06 % for signal frequency 1 kHz and 4.01 % for signal frequency 98 kHz. As can be seen in Fig. 3b for the distance of 0.5 m, the blue LED ODAC emitter does not suffer from excessive E_{RMS} anymore.

Figure 3a confirms this fact showing E_{RMS} dependence on the distance between the emitter and optical receiver. $E_{RMS} = 5\%$ is considered as an acceptable E_{RMS} limit. In case of the blue LED front-end this limit lies

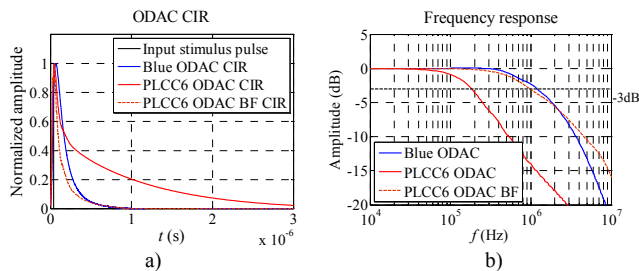


Fig. 4. a) CIR, b) Frequency response.

around the distance of 0.4 m. Naturally, E_{RMS} increases depending on the signal frequency. It is obvious in case of the PLCC6 ODAC front-end where slow yellowish component limits the bandwidth. The E_{RMS} for the 1 kHz and 98 kHz ramp signal is 0.90 % and 4.81 %, respectively, as illustrated in Fig. 3b. Furthermore, an angular E_{RMS} measured at the distance of 0.5 m for both ODAC samples is shown in Fig. 3d. PLCC6 ODAC emitter exhibits better uniformity than the blue ODAC emitter in sense of the error curve shape. This is a consequence of larger blue ODAC front-end active area dimensions resulting in worse optical intensity uniformity displacement in the near field radiation area.

3.2 Channel Impulse and Frequency Response

Frequency response can be considered as one of the key characteristics that implies VLC emitter performance. In conventional VLC applications the emitter is formed by a single LED or single LED array driven via a bias tee. In that case, the LED modulation bandwidth can be easily determined using a simple 3dB test. The bandwidth of an ASMT-YWB1-NGJB2 LED $B_{PLCC63dB}$ is merely 600 kHz ascertained by 3dB test. Since the ODAC concept has a fully digital input, the 3dB bandwidth test is not feasible anymore. In order to investigate ODAC frequency response, the time to frequency domain conversion is employed. In details, the impulse signal (40 ns width and period 100 μ s) is considered as an optimal stimulus to drive the ODAC's LED groups. On the receiver side CIR is captured. As illustrated in Fig. 4a, the blue curve represents CIR of the blue ODAC emitter. The red solid and dashed curves depict PLCC6 ODAC emitter CIRs for the non-filtered and blue-filtered case, respectively.

The ODAC front-end frequency responses, illustrated in Fig. 4b, are obtained using a MATLAB signal post processing based on FFT. The blue curve corresponds to the 1 MHz blue ODAC emitter frequency response. The red curve illustrates PLCC6 ODAC 200 kHz frequency response. Obviously, the ODAC-based front-ends exhibit worse bandwidth compared to the conventional LED front-end using a single LED chip (200 kHz and 1 MHz). This is a usual consequence of driving and wiring constraints typical for the ODAC concept. In case of the PLCC6 ODAC emitter the bandwidth can be further improved filtering out the slow yellow component as can be seen in Fig. 4b (red

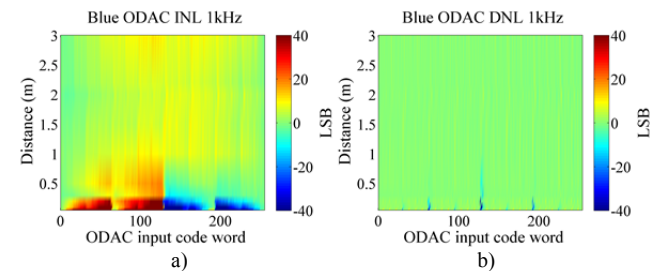


Fig. 5. Blue ODAC 1 kHz: a) INL, b) DNL.

dashed curve). On the other hand, signal filtering induces a notable optical power penalty into the system.

3.1 ODAC Linearity Error

From the perspective of the transfer function linearity, a conventional EDAC can be specified by integral non-linearity (*INL*) and differential non-linearity (*DNL*). Similarly, the same approach can be applied for ODAC specification. Integral nonlinearity is defined as the maximum deviation at any point in the transfer function from the ideal characteristic and can be expressed by:

$$INL(x) = \frac{V_{out}(x) - V_{ideal}(x)}{V_{LSB}} \quad (3)$$

where V_{out} is the amplitude measured at the output of the optical receiver, V_{ideal} is the ideal receiver's output amplitude, V_{LSB} denotes the voltage corresponding to 1 LSB and x corresponds to an input code word.

Differential nonlinearity describes the maximum deviation of the actual and ideal (+1 LSB) analog output step between two adjacent input codes as equation (4) denotes. Moreover, when DNL exceeds -1 LSB the DAC transfer function is non-monotonic [12].

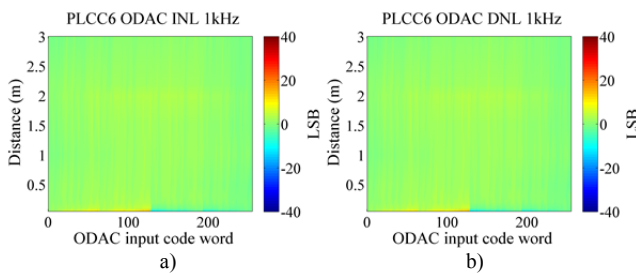


Fig. 6. PLCC6 ODAC 1 kHz: a) INL, b) DNL.

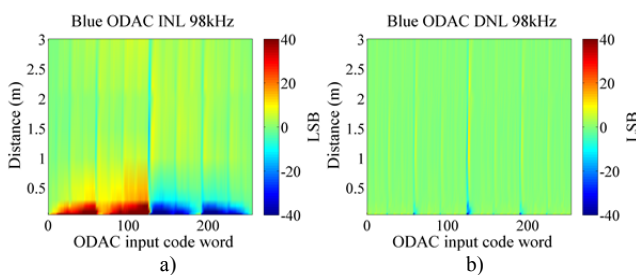


Fig. 7. Blue ODAC 98 kHz: a) INL, b) DNL.

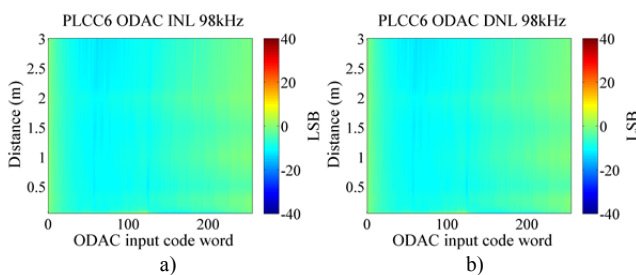


Fig. 8. PLCC6 ODAC 98 kHz: a) INL, b) DNL.

$$DNL(x) = \frac{V_{out}(x+1) - V_{ideal}(x)}{V_{LSB}} - 1 \quad (4)$$

Unlike in EDAC, the linearity error in ODAC also depends on the geometrical set-up between the ODAC emitter and the optical receiver. In order to demonstrate how ODAC INL and DNL depend on geometrical considerations, the graphs in Fig. 5-8 include additional information on the distance between the emitter and optical receiver. Figures 5 and 7 graphically represent INL and DNL of the blue ODAC emitter. Apparently, INL dominates for both signal frequencies. Needless to say, the highest INL is spread in front of the emitter due to the optical intensity non-uniformity as was described formerly. The PLCC6 ODAC front-end shows better INL and DNL at lower frequencies (1 kHz) as depicted in Fig. 6. As illustrated in Fig. 8, INL and DNL increase at higher frequencies (98 kHz) is a result of PLCC6 LED bandwidth shortage.

4. Conclusions

This paper presents a performance evaluation of two ODAC hardware implementations tailored for VLC applications. For the first time, the evaluation takes into account geometrical considerations between the emitter and the optical receiver which is crucial for ODAC performance testing. Furthermore, the performance evaluation is based on dynamic tests rather than static performance tests commonly used for EDAC evaluation. In ODAC architecture, LED array dimensions are a crucial factor influencing ODAC performance especially in the near field area of the emitter. Moreover, the ODAC bandwidth is the key parameter influencing signal distortion on the emitter side. Exceeding the ODAC front-end bandwidth results in significant signal distortion. Although the usable bandwidth of the ODAC concept is typically smaller than in case of single LED front-end, better linearity and no need of an EDAC on transmitter side belong among the strong points of the ODAC concept.

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About the Authors ...

Ales DOBESCH was born in 1989. He received his Ing. (M.Sc.) degree in Electrical Engineering in 2013 and cur-

rently is a Ph.D. student at the Department of Radio Electronics, Brno University of Technology. His main focus is modeling and experimental verification of optical measurement techniques. He is also specialized in modeling and simulating LED radiation distribution and optical communication systems design.

Mónica FIGUEIREDO concluded her Ph.D. study in Electrical Engineering at the University of Aveiro, Portugal, in 2012. She started her research activities in 2001, at the Telecommunications Institute, as a collaborator in the group of Integrated Circuits. Currently, she is a researcher in the same group and an assistant professor in the Polytechnic Institute of Leiria, Portugal. She lectures different courses in digital electronic and communication systems. Her interest fields include timing circuits and high-speed integrated electronics, digital system's implementation in FPGAs and visible light communication systems.

Luis Nero ALVES graduated in 1996 and received his M.Sc. degree in 2000, both in Electronics and Telecommunication Engineering from the University of Aveiro. In 2008, he obtained the Ph.D. degree in Electrical Engineering from the University of Aveiro. His Ph.D. thesis was on high bandwidth gain product amplifiers for optical wireless applications. Since 2008, he is the lead researcher at the Integrated Circuits Group from the Instituto de Telecomunicações – Aveiro. His current research interests are aligned with the IC 1101 COST action (OPTICWISE) on optical wireless communications, where he is an active member. Luis Nero Alves has also participated on several nationally (VIDAS, EECCO both from FCT) and internationally (LITES - CIP, PADSIC - FP7, RTMGear - FP7) funded research projects, and industrial contracts.

Otakar WILFERT was born in 1944. He received the Ing. (M.Sc.) degree in Electrical Engineering in 1971 and CSc. (Ph.D.) degree in Applied Physics in 1984, both from the Military Academy in Brno, Czech Republic. Currently he is a professor at the Department of Radio Electronics, Brno University of Technology. He has investigated problems of free space optical communication under various grant projects from the Ministry of Education of the Czech Republic and the Czech Science Foundation. The main results have been published in prestigious journals and at significant conferences. Areas of his research interest include optical communications and laser radar systems. He is a member of IEEE, SPIE, European Optical Society, Czech and Slovak Photonics Society and the Official Member of Commission D (Electronics and Photonics) of URSI.