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Resistorless Electronically Tunable Grounded Inductance Simulator Design

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***Abstract*—A new realization of grounded lossless positive inductance simulator (PIS) using simple inverting voltage buffer and unity-gain current follower/inverter (CF±) is reported. Considering the input intrinsic resistance of CF± as useful active parameter, the proposed PIS can be considered as resistorless circuit and it only employs in total 16 Metal-Oxide-Semiconductor (MOS) transistors and a grounded capacitor. The resulting equivalent inductance value of the proposed simulator can be adjusted via change of input intrinsic resistance of CF± by means of its supply voltages. The behavior of the proposed simulator circuit is tested via implementation in voltage-mode 5th-order high-pass filter RLC prototype with Bessel, Butterworth, and Chebyshev I approximation. Theoretical results are verified by SPICE simulations using TSMC 0.18 µm level-7 LO EPI SCN018 CMOS process parameters with ±0.9 V supply voltages.**

***Keywords*—Positive inductance simulator; PIS; grounded lossless circuit; current follower; inverting voltage buffer; 5th-order high-pass filter; RLC prototype; Bessel; Butterworth; Chebyshev I; voltage-mode.**

I. INTRODUCTION

The importance of grounded lossless positive inductance simulator (PIS) in circuit theory is well known [1]. Monolithic printed spiral inductors have several drawbacks, for an instance substrate resistive losses, capacitive couplings, not easy tunability in the passive case due to lead of component variations by process tolerances and too costly [2], [3]. Therefore, in order to overcome these disadvantages, researchers have started to focus on ASIC design of synthetic inductors. Therefore, in many cases the size of inductors has been reduce, especially the higher valued ones, their cost, and add the tunability feature for quality factor tuning. A part of those used several passive components in grounded or floating form. Thus, attention was widely focused on the characterization of a passive inductor as an active inductance simulator using different analog building blocks (ABBs), in particularly gain-variable third-generation current conveyor (GVCCIII) [3], modified dual-output differential difference current conveyor (MDO-DDCC) [4], differential second-generation current conveyor (DCCII) [5], [6], modified inverting and conventional first- and second-generation current conveyor (MICCI/MICCII/CCI/CCII) [7]–[11], dual-X second-generation current conveyor (DXCCII) [12], differential voltage current conveyor (DVCC) [13], current-feedback operational amplifier (CFOA) [14], z-copy current-controlled current inverting transconductance amplifier (ZC-CCCITA) [15], positive four-terminal-floating-nullor (PFTFN) [16], differential difference operational mirrored amplifier (DDOMA) [17], voltage differencing inverting buffered amplifier (VDIBA) [18], etc. and their equivalent using commercially available devices [19].

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The aim of this paper is to increase the variety of inductance simulator circuits in the literature with introduction of a new PIS topology based on two inverting voltage buffers (IVBs), unity-gain current follower/inverter (CF±) , and one grounded capacitor. The proposed circuit is electronically tunable via change of intrinsic input resistance of CF± by means of its supply voltages. The behavior of the proposed simulator circuit is tested in voltage-mode 5th-order high-pass filter RLC prototype with Bessel, Butterworth, and Chebyshev I approximation. SPICE simulation results have been performed to confirm the theory.

II. CIRCUIT DESCRIPTION

Basic NMOS-based CMOS IVB is shown in Fig. 1(a) [20], [21]. Considering non-ideal IVB, in which assuming that both transistors work in saturation region, $V_{THN1} = V_{THN2}$, $+V_{DD} = -V_{SS}$, and $k_{N1} = k_{N2}$, it can be described by the following hybrid matrix:

$$\begin{bmatrix} I_{in} \\ V_{out} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ -\beta(s) & R_{IVB\_o} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_{out} \end{bmatrix}, \tag{1}$$

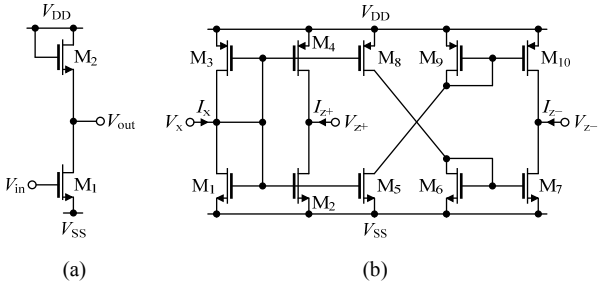

Fig. 1. CMOS implementations: (a) inverting voltage buffer (IVB), (b) unity-gain current follower/inverter (CF±).

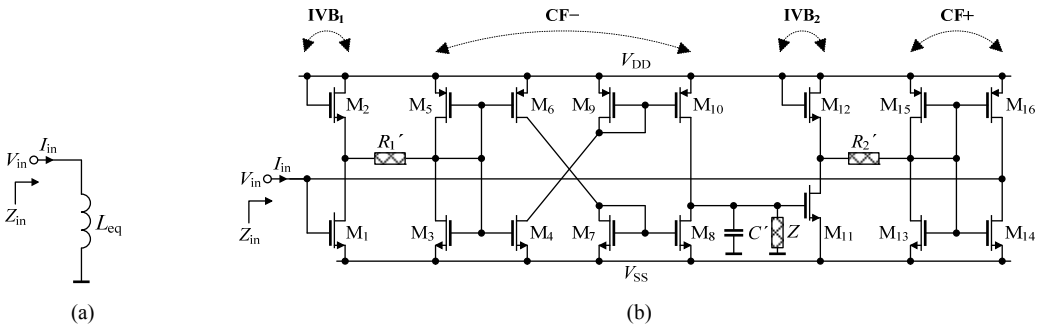

Fig. 2. (a) Symbol of a PIS, (b) CMOS implementation of proposed resistorless PIS including the main parasitics.

where in (1) the main source of non-ideality is a non-zero output resistance $R_{\mathrm{IVB\_o}} \cong (1/g_{\mathrm{m2}}) \,\|\, r_{\mathrm{o1}}$ of the output terminal. Note that the $\beta(s)$ is frequency-dependent non-ideal voltage gain, which using a single-pole model can be expressed as $\beta(s) = \beta_{\mathrm{o}}/(1 + s\tau_{\beta})$, where $\beta_{\mathrm{o}} = 1 - \varepsilon_{\beta v}$ is DC voltage gain of IVB and $\varepsilon_{\beta v}$ denotes voltage tracking error with $|\varepsilon_{\beta v}| \ll 1$.

Similarly, the unity-gain CF± is a three-terminal ABB with CMOS implementations shown in Fig. 1(b) [18], [22]–[24]. Using standard notation and taking into account its main parasitics, it can be described by the following hybrid matrix:

$$\begin{bmatrix} V_{\mathrm{x}} \\ I_{\mathrm{z+}} \\ I_{\mathrm{z-}} \end{bmatrix} = \begin{bmatrix} R_{\mathrm{x}} & 0 & 0 \\ \alpha_{+}(s) & sC_{\mathrm{z+}} + 1/R_{\mathrm{z+}} & 0 \\ -\alpha_{-}(s) & 0 & sC_{\mathrm{z-}} + 1/R_{\mathrm{z-}} \end{bmatrix} \begin{bmatrix} I_{\mathrm{x}} \\ V_{\mathrm{z+}} \\ V_{\mathrm{z-}} \end{bmatrix}, \quad (2)$$

where in (2) the main source of non-idealities is firstly the intrinsic input impedance R_{x}, which value can be found and approximated as given in [22] and its value can be set via supply voltages. Equivalent resistance seen at output ports $z\pm$ can be expressed as $R_{\mathrm{z+}} \cong r_{\mathrm{o2}} \,\|\, r_{\mathrm{o4}}$ and $R_{\mathrm{z-}} \cong r_{\mathrm{o7}} \,\|\, r_{\mathrm{o10}}$, respectively. Secondly, the main source of non-idealities is parasitic admittance $Y_{\mathrm{z\pm}}$ at terminals $z\pm$, which is modeled by a parallel non-ideal output resistance $R_{\mathrm{z\pm}}$ and capacitance $C_{\mathrm{z\pm}}$. Note that the $\alpha_j(s)$ for $j = \{+, -\}$ are frequency-dependent non-ideal current gains, which using a single-pole model can be defined as $\alpha_j(s) = \alpha_{\mathrm{jo}}/(1 + s\tau_{\alpha j})$, where $\alpha_{\mathrm{jo}} = 1 - \varepsilon_{\alpha j}$ are DC current gains of CF±, $\varepsilon_{\alpha j}$ denote current tracking errors described as $|\varepsilon_{\alpha j}| \ll 1$. In ideal case the above mentioned voltage β_{o} and current α_{jo} gains are unity.

III. Inductance Simulator Design

Symbol of a lossless PIS and the CMOS implementation of proposed resistorless PIS including the main parasitics are shown in Figs. 2(a) and (b), respectively. Considering the use of a single grounded capacitor and assuming non-idealities of ABBs, i.e. the input intrinsic resistances R_{xk} at x terminal of CF±s as useful active parameters, finite output admittances at ports $z\pm$, non-zero output resistance $R_{\mathrm{IVB\_o}k}$ of the output terminal of IVBs, and DC voltage gains β_{ok} and current gains $\alpha_{\mathrm{jo}k}$ of both ABBs for $k = \{1, 2\}$, its routine circuit analysis yields the following input impedance:

$$\begin{aligned} Z_{\mathrm{in}}'(s) &= \frac{V_{\mathrm{in}}}{I_{\mathrm{in}}} = \\ &= R_{\mathrm{lossy}} + sL_{\mathrm{eq}} = \frac{R_1' R_2'}{\alpha_{-\mathrm{o}1}\alpha_{+\mathrm{o}2}\beta_{\mathrm{o}1}\beta_{\mathrm{o}2}Z} + \frac{R_1' R_2' sC'}{\alpha_{-\mathrm{o}1}\alpha_{+\mathrm{o}2}\beta_{\mathrm{o}1}\beta_{\mathrm{o}2}}, \end{aligned} \quad (3)$$

where $R_k' = R_{\mathrm{IVB\_o}k} + R_{xk}$, $C' = C + C_{\mathrm{z-1}}$, while $Z = R_{\mathrm{z-1}}$. Note that (3) results in lossy grounded inductance simulator (serial R-L) with quality factor:

$$Q_{\mathrm{L}} = \frac{\omega L_{\mathrm{eq}}}{R_{\mathrm{lossy}}} = \omega C' R_{\mathrm{z-1}}. \quad (4)$$

Hence, its quality factor of PIS is frequency dependent and has finite value.

IV. Simulation Results

To verify the theoretical analysis, the proposed grounded lossless PIS in Fig. 2(b) has been simulated using SPICE program. DC power supply voltages were set $+V_{\mathrm{DD}} = -V_{\mathrm{SS}} = 0.9$ V. In the design, transistors are modeled by the TSMC 0.18 μm level-7 LO EPI SCN018 CMOS process parameters ($V_{\mathrm{THN}} = 0.3725$ V, $\mu_{\mathrm{N}} = 259.5304$ cm^2/(V·s), $V_{\mathrm{THP}} = -0.3948$ V, $\mu_{\mathrm{P}} = 109.9762$ cm^2/(V·s), $T_{\mathrm{OX}} = 4.1$ nm) [25]. Main design parameters of used ABBs are available in [18] and the aspect ratios of CMOS transistors in PIS are listed in Table I. All simulations were done with setting temperature as 25°C.

Additionally, the proposed PIS was simulated with the following active parameters and passive element values: R_k' [18] and $C = \{12.11; 38.63\}$ pF, which result in $L_{\mathrm{eq}} = \{98.36; 313.79\}$ μH, respectively. The ideal and simulated magnitude and phase responses are shown in Fig. 3. Due to parasitics, the performance of the proposed lossless PIS is reduced.

TABLE I. Transistor Dimensions of PIS.

NMOS Transistors	W/L (μm)/(μm)	PMOS Transistors	W/L (μm)/(μm)
M_1, M_2, M_{11}, M_{12}	54/0.18	M_5, M_6, M_9, M_{10}, M_{15}, M_{16}	8.64/1.08
M_3, M_4, M_7, M_8, M_{13}, M_{14}	2.16/1.08		

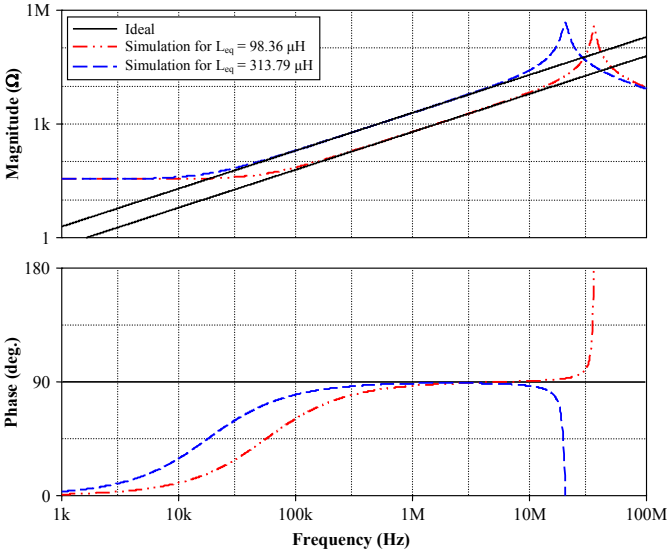

Fig. 3. Ideal and simulated magnitude and phase responses of the proposed PIS with different impedances relative to frequency.

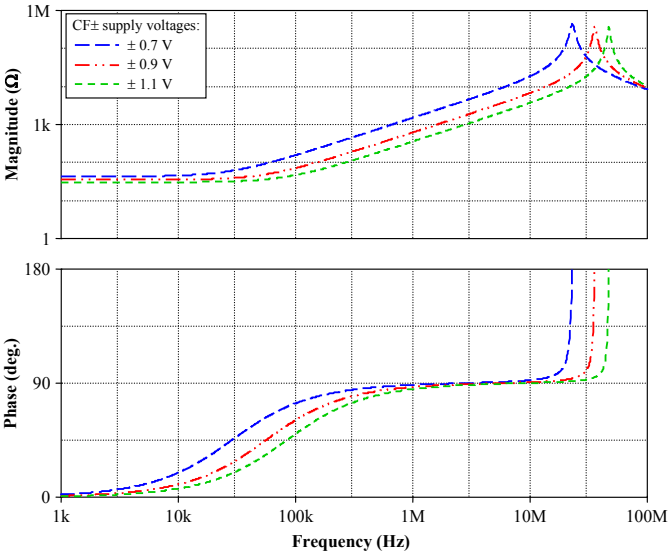

Fig. 4. Simulated magnitude and phase responses of the impedance of the grounded lossless PIS with value L_{eq} = 98.36 µH vs. frequency for different supply voltage of CF±.

Considering 10 deg. phase deviation, the useful frequency ranges for L_{eq} with values mentioned above are about 300 kHz up to 30 MHz and 100 kHz up to 16 MHz, respectively. Figure 4 shows the simulated magnitude and phase responses of the impedance of the grounded lossless PIS with value L_{eq} = 98.36 µH vs. frequency for different supply voltage of CF±.

To demonstrate the usefulness of the proposed resistorless grounded lossless PIS, it was used in a 5th-order high-pass filter (HPF) realization. The passive RLC prototype is shown in Fig. 5. Passive component values and design parameters obtained for $f \cong 1$ MHz cut-off frequency with Bessel, Butterworth, and Chebyshev I type (with passband ripple 1 dB) approximations are given in Table II. Ideal and simulated gain

TABLE II. PASSIVE COMPONENT VALUES AND DESIGN PARAMETERS USED IN 5TH-ORDER HIGH-PASS FILTER RLC PROTOTYPE

Components	Bessel approximation	Butterworth approximation	Chebyshev I approximation
R_S, R_P (kΩ)	1		
C_{S1} (pF)	913.11	257.5	74.55
C_{S2} (pF)	197.95	79.58	53.03
C_{S3} (pF)	70.48	257.5	74.55
L_{P1} (µH) [C_{P1_Leq} (pF)]	313.79 [38.63]	98.36 [12.11]	145.9 [17.96]
L_{P2} (µH) [C_{P2_Leq} (pF)]	143.25 [17.64]		

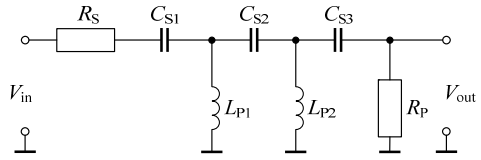

Fig. 5. 5th-order high-pass RLC ladder prototype.

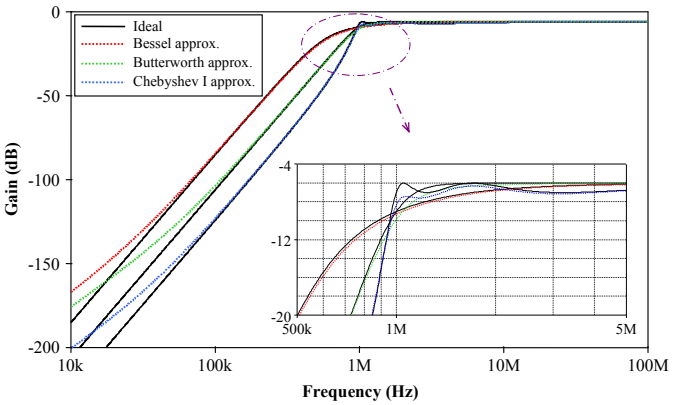

Fig. 6. Ideal and simulated gain characteristics of the 5th-order VM high-pass filter with three different approximations.

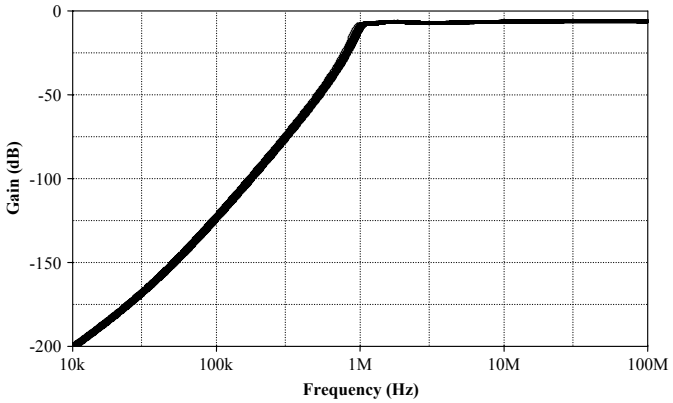

Fig. 7. Monte Carlo analysis: Gain response changes of 5th-order VM high-pass filter with Chebyshev I approximation due to 5% tolerance of passive component values.

characteristics of designed RLC ladder prototype equivalents are shown in Fig. 6. In order to observe possible manufacturing process variations and their effect on 5th-order HPF designed from RLC ladder prototype equivalent based on Chebyshev I type approximations, Monte Carlo analysis was performed with

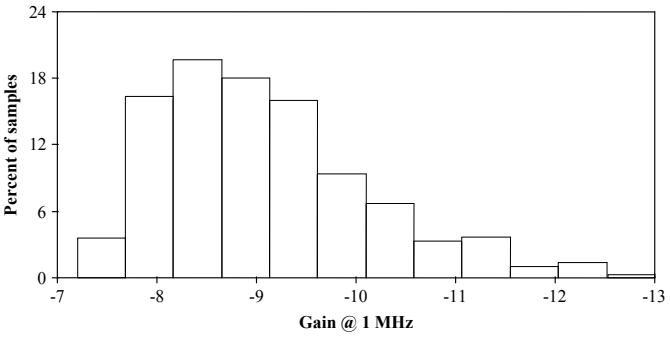

Fig. 8. Monte Carlo analysis: Gain variation of the 5th-order VM high-pass filter with Chebyshev I approximation at 1 MHz.

5% tolerance for passive component values and 300 runs. Figure 7 shows the simulated gain response of the proposed filter. The histogram in Fig. 8 demonstrates the variation of the gain of the selected filter at 1 MHz. From obtained results it can be seen that they are in very good agreement with the theory.

V. CONCLUSION

In this paper, an electronically tunable grounded inductance simulator topology has been presented. It employs simple inverting voltage buffers and unity-gain current follower/inverter as active building blocks and one grounded capacitor as passive element. In total it is composed of 16 Metal-Oxide-Semiconductor (MOS) transistors. Additional main advantages of introduced inductance simulator are the following: (i) employs grounded capacitor, (ii) resistorless circuit, (iii) composed of low number of transistors, (iv) tunability, and (v) provides high linearity and wide bandwidth in high frequencies. To demonstrate the validity of the proposed grounded PIS, its behavior is tested in voltage-mode 5th-order high-pass filter RLC prototype with Bessel, Butterworth, and Chebyshev I approximation. The simulation results verify the theoretical analysis.

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