PRINCIPLE OF THE NEW ADJUSTED ARCHITECTURE OF R-2R D/A CONVERTER

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Abstract: Original R-2R D/A Converter architecture has a shortcoming – while resolution is bigger than 7 bits, switching of MSBs causes a significant non-linearity error, which may even cause DAC to be non-monotonous. A possible solution to this issue is shown in this paper: dividing MSBs into subbits of a lower weight. Analog circuitry and digital driving is published in this paper.

Keywords: Analog Integrated Circuits, D/A Conversion, DNL, INL, R-2R DAC, Small Chip Area

1 INTRODUCTION

A design of an R2R D/A Converter (R2R stands for R-2R resistor ladder) with DNL (Differential Non-linearity Error) and INL (Integral Non-linearity Error) lower than 1 LSB (Least Significant Bit) and small area consumption is published in this paper. Well-known R2R D/A Converter has a disadvantage: when MSB (Most Significant Bit) is switched on and all the lower bits are switched off (0111→1000), DNL is the highest in the whole range. The height of the step may surpass 1 LSB significantly, especially if number of bits is high. If the analog value of the code word 1000 is higher than analog value of 1001, D/A converter is no longer monotonous [2].

Solution of this problem is described in this paper. D/A converter is designed in ON Semiconductor technology I4T (45 V, 180 nm). It is optimized for automotive applications. Technical parameters are 9 bits, $V_{DD} = 3.3$ V, $V_{REF} = 1.6$ V.

2 ARCHITECTURE OF THE R2R D/A CONVERTER

Well-known R2R D/A Converter is based on binary weighing of the bits by resistor ladder [1]. LSB of 9-bit R2R DAC has a weight of $\frac{V_{REF}}{512}$, while MSB $\frac{V_{REF}}{2}$. Switching of MSB causes huge non-linearity error. Mismatch error of this particular resistor has a huge influence on the precision of the whole converter. Solution is suggested in this paper: to avoid switching of such a significant weight in one step.

Experimentally it was proved that switching of the weight bigger than $\frac{V_{REF}}{8}$ is inconvenient [2]. 2 MSB's were divided into 6 subbits of weight $\frac{V_{REF}}{8}$, $(\frac{1}{2}+\frac{1}{4})V_{REF} = \frac{6}{8}V_{REF}$. 3rd MSB, which is originally $\frac{V_{REF}}{8}$, has different digital driving compared to the original DAC. In this paper, they are referred to as 7 subbits even though one of them is technically a bit.

7 subbits have the same weight – they are weighted linearly. All 3 MSB's in total have the weight of $(\frac{1}{2}+\frac{1}{4}+\frac{1}{8})V_{REF} = \frac{7}{8}V_{REF}$. Each subbit has the weight of $\frac{V_{REF}}{8}$. Weight of 1st MSB is equivalent to 4 subbits, weight of 2nd MSB to 2 subbits and the weight of 3rd MSB to 1 subbit.

Details of switching subbits instead of original bits is shown in Table 1. There are two options

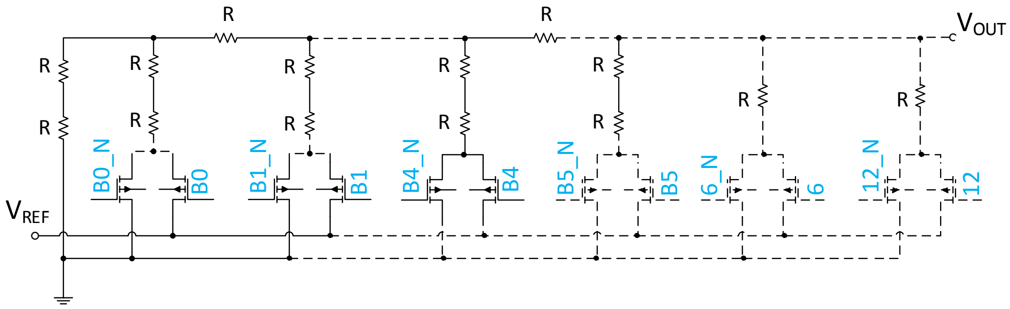

Figure 1: 9-bit R2R DAC. Gate labels stand for digital driving.

presented in this paper. DNL of the crucial steps is diminished via alternative switching. Circuitry is presented in Figure 2.

3 DIGITAL DRIVING

Original Bits			**Thermometric Driving**							**Advanced Driving**						
B8	B7	B6	12	11	10	9	8	7	6	12	11	10	9	8	7	6
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0
0	1	1	0	0	0	0	1	1	1	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1	1	0	0	1	1	1	1	0
1	0	1	0	0	1	1	1	1	1	0	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 1: Thermometric and Advanced Driving: Truth table of 3 MSB's and 7 subbits.

Truth table shown in table 1 is transformed into digital circuits driving the subbits. Thermometric driving requires 6 logic gates (shown in figure 2). Advanced driving requires only 2 logic gates, however, it increases DNL and INL (shown in Figure 3) as bigger weights are switched - two subbits at the same time. DNL and INL can be diminished if the area of the resistors is bigger. However, if thermometric driving is used, precision requirements are met while area consumption in total is smaller.

R2R DAC with both binary and linear weighing is described by equation 1

$$V_{OUT} = \frac{V_{REF}}{m+1}(sb_0 + sb_1 + \ldots + sb_{m-1} + sb_m) + \frac{V_{REF}}{2}b_{n-1} + \frac{V_{REF}}{4}b_{n-2} + \ldots + \frac{V_{REF}}{2^{(n-1)}}b_1 + \frac{V_{REF}}{2^n}b_0. \quad (1)$$

m stays for number of subbits weighted linearly. n stays for number of bits weighted binary. sb_m stays for the value of the subbit, 1 or 0. Weights are added decimaly ($1+1+1=3$). b_n stays for the value of a bit.

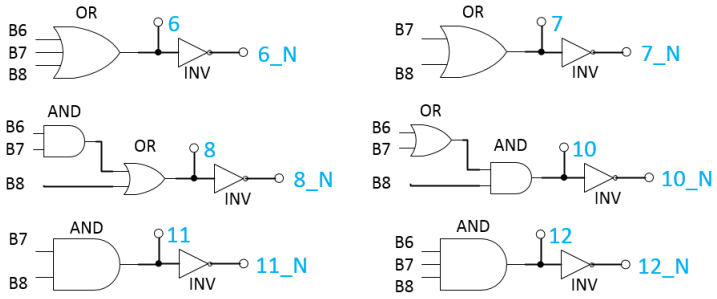

Figure 2: Digital driving circuits switching the subbits on and off – thermometric driving.

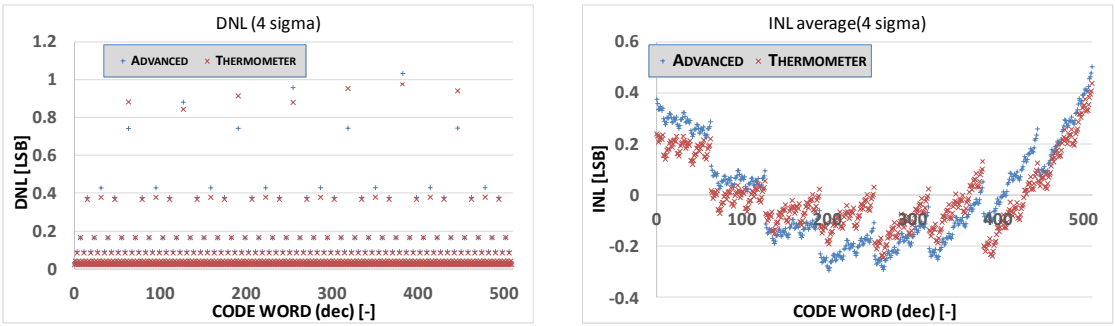

Figure 3: DNL and INL of Advanced and Thermometric solution.

4 CONCLUSION

Alternative architecture of R2R DAC was introduced in this paper. Two options of digital driving were simulated in Cadence Virtuoso 6. MonteCarlo mismatch simulation was performed (100 runs, Cadence Virtuoso), results are shown in Figure 3. It is obvious, that only switching two subbits at the same time makes DNL and INL bigger. If the MSB was switched as in original architecture, DNL and INL would significantly increase.

The area of the resistor bank on the chip is approximately 8 times smaller while using alternative architecture with 7 linearly weighted subbits and thermometric driving compared to the standard one and two times smaller compared to the one using advanced driving.

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[2] Internal documents of the company ON Semiconductor.