INTEGRATED TEMPERATURE SENSOR BIPOLAR CORE

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Abstract: Analog front-end of a bipolar transistor based smart temperature sensor was designed in 110 nm CMOS processing technology TSMC 110 and verified using simulation taking PVT variation into account. The analog front-end of the sensor achieves 3σ inaccuracy of $\pm 3.5\,^{\circ}\mathrm{C}$ untrimmed or $\pm 0.7\,^{\circ}\mathrm{C}$ after single point trim over the military temperature range ($-55\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$), requiring supply voltage of 2.7-3.63 V, consuming as little as 1 µW at 1 S/s and taking up less than $0.012\,\mathrm{mm}^2$.

Keywords: bipolar, smart temperature sensor, CMOS, analog, integrated circuit, IP core

1 INTRODUCTION

Smart temperature sensors are integrated circuits which consist of three main parts: the analog front-end (biasing and sensing circuits), the ADC (usually ΣΔ modulator) and digital signal processing (DSP). As small independent units which require no external references and which directly output temperature as a digital word, they are distributed as IP cores to be used in customer ASICs. As the precision of the analog front-end is severely affected by process spread and device mismatch and trimming is expensive, advanced circuit techniques such as Dynamic Element Matching (DEM) or chopping are employed to achieve precision competitive with discrete solutions with at most one trim.

2 BIPOLAR ANALOG FRONT-END THEORY OF OPERATION AND DESIGN

The CTAT dependence of V_{BE} and the PTAT dependence of ΔV_{BE} of substrate PNP bipolar junction transistors (BJT) is exploited to sense the die temperature. The β of these BJTs is ≈ 2.5 and their collector is irreversibly grounded, but they are less susceptible to process variation, their I-V characteristics are close to ideal and they do not require expensive process options to manufacture.

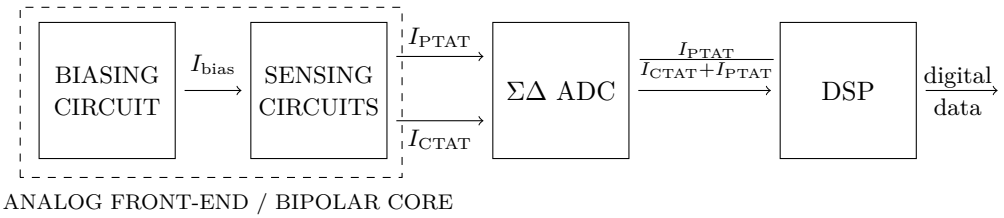

Figure 1: BJT-based smart integrated temperature sensor block diagram

An analog front-end of a BJT-based smart temperature sensor, also known as bipolar core, consists of a self-biasing circuit which generates a PTAT biasing current I_{bias} derived from ΔV_{BE}, and the sensing circuits which use I_{bias} to produce V_{BE} and ΔV_{BE}, which are converted into PTAT and CTAT currents and scaled appropriately. The ΣΔ modulator digitizes the linearly temperature dependent ratio of these currents $\mu(T) = \frac{I_{\mathrm{PTAT}}}{I_{\mathrm{CTAT}}+I_{\mathrm{PTAT}}}$ into a high speed 1-bit signal and the DSP then averages, decimates and scales the bitstream to output temperature reading in Celsius as a digital word.

2.1 BIASING CIRCUIT

The biasing circuit consists of the ΔV_{BE} generator loop, controlled by a 90 dB-gain folded cascode opamp chopped at 20 Hz (only 30 µV input voltage offset remains), and the starting circuit shown on far left of figure 2. A steeply PTAT I_{bias} (300 nA at 27 °C) is generated by applying a PTAT voltage ΔV_{BE} to a negative TCR polysilicon resistor R_{bias}, as such current helps to reduce the intrinsic curvature of V_{BE} [1, p.77]. The ΔV_{BE} is generated by the two BJTs biased at current ratio m=5, which is accurately set by six PMOS current sources, which are cyclically interchanged at f_{m-DEM}=6·2·f_{chop} so that their mismatch is averaged out to 0.01% precision. The smaller resistor makes I_{bias} dependent on β in such a way that the β dependence of the sensing circuit BJTs is canceled out. The main error in this circuit is the process spread of R_{bias}, which causes spread of I_{bias}.

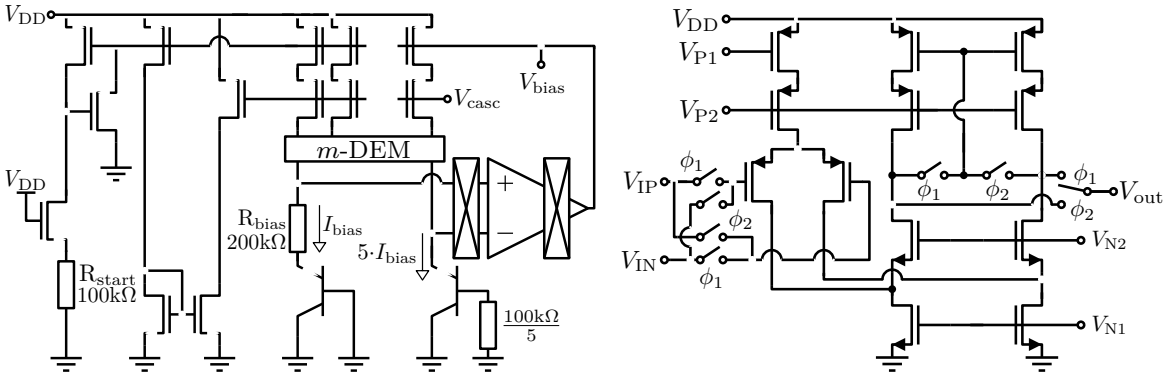

Figure 2: Simplified biasing circuit and chopped folded cascode opamp schematics

2.2 SENSING CIRCUITS

The sensing circuits utilize I_{bias} to generate the PTAT and CTAT currents used for measuring the temperature utilizing the same opamp as in the biasing circuit. The PTAT sensing circuit uses 10 DEM-ed current sources (f_{r-DEM}=10·f_{m-DEM}) and DEM-ed resistors (f_{R-DEM}=2·f_{r-DEM}) to produce ΔV_{BE} based on accurate current density ratio $r = 9$. The CTAT sensing circuit converts V_{BE} to a current and divides it by $\alpha = 10$, which is a ratio precisely set by DEM ($f_{\alpha-DEM}$=11·f_{R-DEM}). This scaling performs ratiometric curvature correction and helps to make $\mu(T)$ more linear [1, p.88]. Resistance

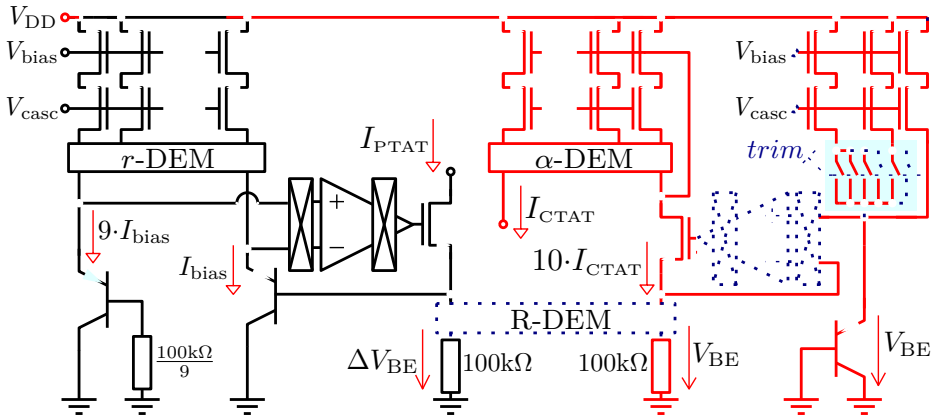

Figure 3: Sensing circuits simplified schematic

spread in the sensing circuits is not an issue as it is the ratio and not the absolute value of CTAT and PTAT currents which is digitized. As ΔV_{BE} is only dependent on the current ratio and therefore

precise, V_{BE} is the main source of error due to BJT process spread and I_{bias} spread. A 6-bit binary-weighted current divider network allows to set the correct V_{BE} in steps of $\approx 0.3\,\text{mV}$ by trimming the emitter current. The unused trimming currents are redirected to a dummy BJT which is not shown.

3 ACHIEVED PERFORMANCE

The simulated precision is depicted on figure 4. The error of untrimmed sensor is mainly PTAT, as it is dominated by the process spread of BJTs and the spread of I_{bias}, while the remaining error after trimming is dominated by the remanent curvature of V_{BE}, charge injection, bipolar transistor mismatch etc. For comparison, untrimmed 3σ error with chopping and DEM turned off is $\pm 12\,^{\circ}\text{C}$.

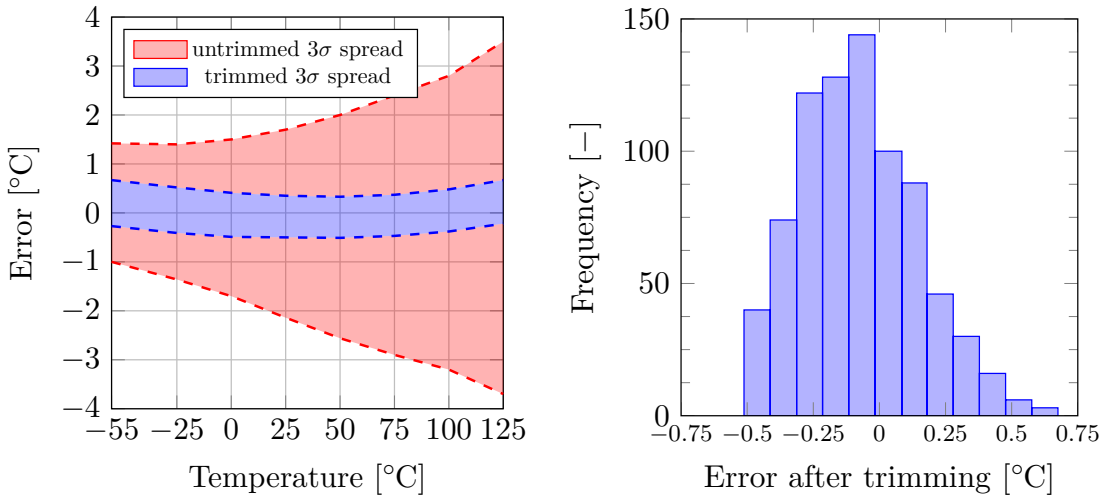

Figure 4: Temperature reading error across all PVT conditions

The bipolar core can work with supply voltage as low as 2.7 V, consumes at most 200 µW when on and takes up 0.012 mm^2, assuming 20% of the area is used for routing, dummy devices etc. In power-down mode, the circuit draws less than 8 nA, which is mostly given by leakage at high temperature.

4 SUMMARY

Analog front-end of a smart temperature sensor was designed in CMOS process technology TSMC 110 and verified by simulation. Precision of $\pm 3.5\,^{\circ}\text{C}$ untrimmed or $\pm 0.75\,^{\circ}\text{C}$ after trimming was achieved over the military temperature range on area smaller than 0.012 mm^2.

These results closely approach the theoretical limits of this particular architecture and as such, this design is competitive with the current state of the published art. As most errors were already eliminated by trimming, DEM, chopping and β compensation, any further improvements would require increasingly more complex circuits which might not justify their area and power consumption costs.

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