UNIVERSAL POWER SEQUENCER FOR RF POWER AMPLIFIERS

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Abstract: More often used Galium Nitride (GaN) based Radio-Frequency high power transistors in the various RF PA configurations e.g. Doherty is by their nature easily destroyed, great care must be taken, when powering-up and shutting down this circuits. That means, proper power biasing and sequencing is necessary. The Doherty type RF PA with RF drivers four different gate, drain voltages and time when the individual voltages are turned on or off must be controled. Universal power sequencer and biasing device, which meets this requirements is described in this article.

Keywords: GaN, RF PA, Biasing, Power Sequencing

1 INTRODUCTION

Emerging 5G technologies promising greener, environmetaly friendly technologies with demand for higher bandwiths by introducing massive multiple - input - multiple output (MIMO), beamforming, small cells techniques, while network should be as much energy efficient as possible. To achieve this goals special care must be taken for radiofrequency power amplifiers (RF PA). Nowadays, promissing technology for RF PAs power transistors are Galium Nitride types - an effiecient, wide band-gap transistors, offering supperior properties e.g. power density, power added efficiency (PAE), gain, impedance matching and so on. Common techniques to achieve higher efficiency is to push bias point closer to saturation region in combination with some kind of predistorting technique due to non-linear behavior of the transistor in this region. This require intensive measurements and tests of the power amplifiers and predistorters, with many on-off cycles. Power transistors in the RF PAs are very sensitive devices and require special care, particularly GaN devices are very sensitive, because they are opend, when V_{GATE} is equal zero.
Recommended power sequence for correct turn on sequence is shown in fig. 1 a), where is very important to turn on drain voltage (V_{drain}) after gate voltage (V_{pinch}) is applied and stable. Than is bias gate voltafe set. Power sequence for correct turn off sequence is shown in fig. 1 b).
Commercial solution is either using of several power supplies with triggering option or using multichannel programmable power supply with possibility of the power sequencing e.g Keysight [2] or Rohde & Schwarz [1]. This solutions are expensive for such problem, so cheaper alternative with use of the shelf power supply is introduced, which is able to automatically and correctly cycle thru this sequencing is introduced. Commercial product of this type is not known in the time of writing this paper. Nowadays are often used and investigated various structures for RF PA and one of them is Doherty structure consisting pair of output the power transistors and often pair of the driver transistors and therefor four channel sequencer is necessary, with need of synchronized outputs. Brief simplified schematic is schown in fig. 2.
Proposed RF PA power sequencer should have this properties.

- Four channel output

- Gate voltages generated internally, it is highly recommended to set pinch off voltage, and after drain voltage set, bias gate voltage
- Possibility to set up all parameters, e.g. pinch off voltage, gate voltage, drain on-off time, gate time directly on the sequencer
- Able to switch drain voltage up to 60V with current at least 10A.
- Internally generated gate voltage $\pm 10V$
- Basic fault sensing
- As compact as possible
- Cheaper than commercial programmable power supplies

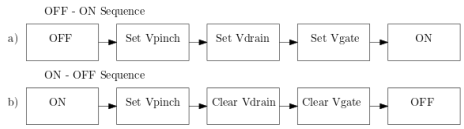

Figure 1: a) Recommended turn on sequence b) Recommended turn off sequence

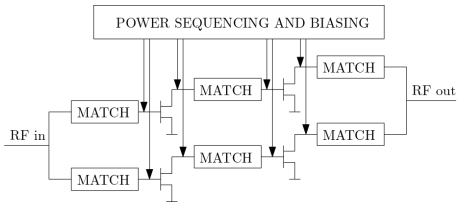

Figure 2: Connecting sequencer to RF Power Amplifier

2 IMPLEMENTATION

Block diagram of the proposed fig. 2 consist main microcontroller, in this case ARM Cortex M4 by NXP semiconductor, MK64FN1, which is controlling whole system, to which is connected rottary encoder for data input and setup sequence according to requirements, TFT display with internal driver for displaying status of the sequencer, setted values e.g. pinch off voltage, gate voltage, time delays and which channel is enabled or disabled, and realtime measured voltages of the gate, drain in voltage and drain out voltage. Next, microcontroller is responsible for correctly controlling quad channel modules CH1 - CH4. Signal $V_{drain}ON$ is turning in P-MOSFET transistor for drain voltage. This is supplied from external source and is only monitored by internal analog to digital converted (ADC), where are connected monitoring signals $V_{Din}Monitor$ and $V_{Dout}Monitor$. Gate and pinch-off voltage is generated internally, because pinch-off and gate biasing voltages are generally different. Digital to analog converter (DAC) in the channel modules is used for this purpose and is controlled via SPI bus from microcontroller. Gate voltage is enabled with signal $V_{Gate}ON$ and is monitored by ADC measuring signal $V_{Gate}Monitor$. Start and Stop sequence are triggered by separated push buttons located at the front panel of the power sequencer.

More detailed block diagram of the ciruitry if one of the channels, which is the same for all of them, is shown in fig. 4. Drain voltage is switched by P-MOSFET power transistor. Parameters of this transistor are crucial for this operation. On behalf of required switching current, transistor should be able to swith at least 10A current and have as low R_{DSON} as possible. Firstly due to minimizing termal loss and secondly for keep voltage drop between V_{Din} and V_{Dout} as low as possible. Gate driver for this transistor is causing correct switching characteristics of the transistor and level shift from 3.3V

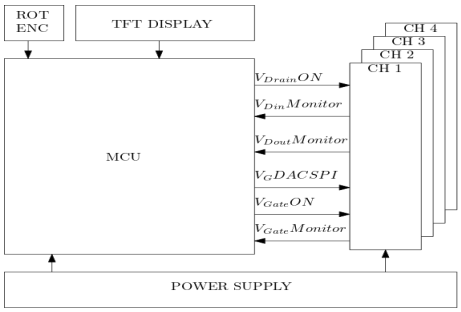

Figure 3: Block diagram of the sequencer

logic of the microcontroller. Sensing drain voltages are done by attenuation, filtering, buffering by operational amplifiers, filtered by anti-aliasing filters and than fed into internal ADC channels of the microcontroller. Gate voltage is generated by digital to analog converter located as close as possible to output terminals, driven by SPI interface from microcontroller. Used DAC is Texas Instruments DAC8811, one channel DAC with reolution of 16bit and current output, which is transformed into bipolar voltage $\pm 10V$, than filtered and fed into high power operational amplifier OPA453, with shutdown option. Generated gate voltage is monitored and fed back after attenuation, buffering and filtering to microcontroller's ADC. Channel modules are implemented on the separated printed ciruit boards (PCB) and are located as close as possible to output terminals. Prototype realization is shown in fig. 5, where is visible channel terminals on the bottom, START, STOP push-buttons on the right, rottary encoder between push-buttons and TFT display, and TFT display. Display is showing current state of the sequencer (idle state on the picture), parameters legend, values set by user and realtime measured voltages on the sequencer terminals. Output set voltages error is shown in fig. 6. Accuracy of the output voltage is well within range of $\pm 0.0001\%$

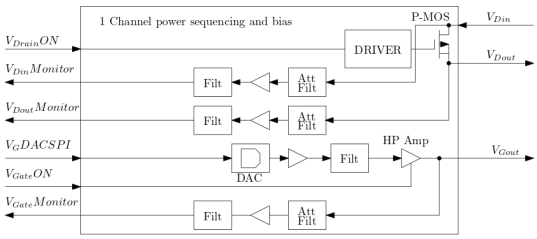

Figure 4: Block diagram of one channel of the sequencer

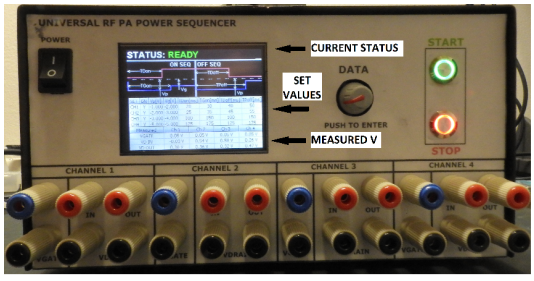

Figure 5: RF Power sequencer prototype

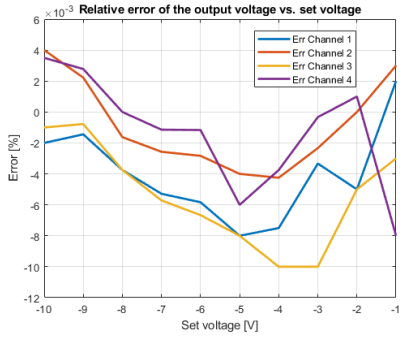

Figure 6: Output voltage relative error vs. set voltage

3 SOFTWARE IMPLEMENTATION

There are two main parts implemented in the software of the power sequencer. First part is setup parameters. By holding encoders push-button for at least 3 seconds, sequencer enters setup device, where is possible to set these parameters:

- Active channel - enables - disables current channel. Necessary for operation with fewer channels.
- Pinch-off voltage V_p
- Biasing gate voltage V_g
- Time to switch on drain voltage T_{Don}
- Time to switch gate bias voltage T_{Gon}
- Time to switch drain voltage off T_{Doff}
- Tme to switch pinch-off gate voltage T_{Poff}

Second part of the software is main control loop, which is best described by flow-diagram in fig. 7. After power up, sequencer immediately enter idle mode, when gate and drain voltages are turned off, which is shown on the display as STATUS: READY and is waiting for triggering start sequence by START button or activating setup menu by pressing and holding down rotary encoder knob. Firstly are checked all voltages on the enabled channels. If exist voltage failure there, e.g. drain voltage not present, this cause fault message and it is restricted to continue in the sequence. After correct voltage check, pinch-off voltage is set by DAC which is also monitored (in case there is no voltage in the gate terminals, fault is generated and sequence is interrupted) and sequencer is waiting Td ms to turn on, which follows setting up biasing gate voltage after Tg ms. Correct operation and successful sequence is shown on the display as STATUS: RUNNING. Now, sequencer constantly checking voltages on the terminals and in case, there is problem e.g. difference between set and measured gate voltage, drain voltage missing, immediatelly is state interrupted. This means as soon as possible is switched off drain voltage and after Tgoff gate voltage. Other way, sequencer is waiting for stop sequence trigger caused by STOP button. After STOP button is hitted gate voltage is set to pinch-off voltage, than waits TDoff ms to switch off drain voltage and after Tpinch ms is switched off gate voltage also. Then sequencer enters IDLE mode.

Output voltage waveforms of the start sequence and stop sequence are shown in fig. 8 for two channels, where yellow trace is gate voltage, green trace is drain voltage of channel 1, blue trace gate voltage and magenta drain voltage of the channel 2.

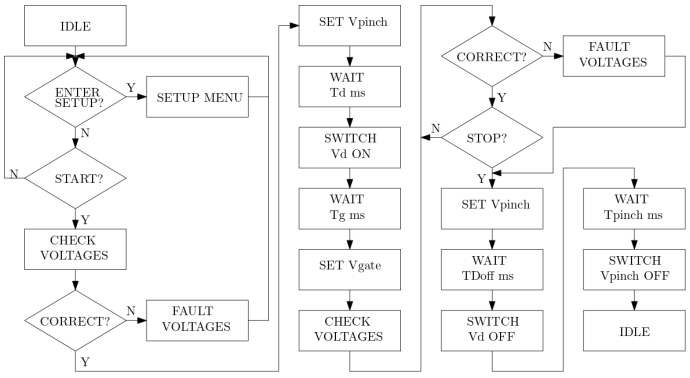

Figure 7: Flow diagram of the sequencer

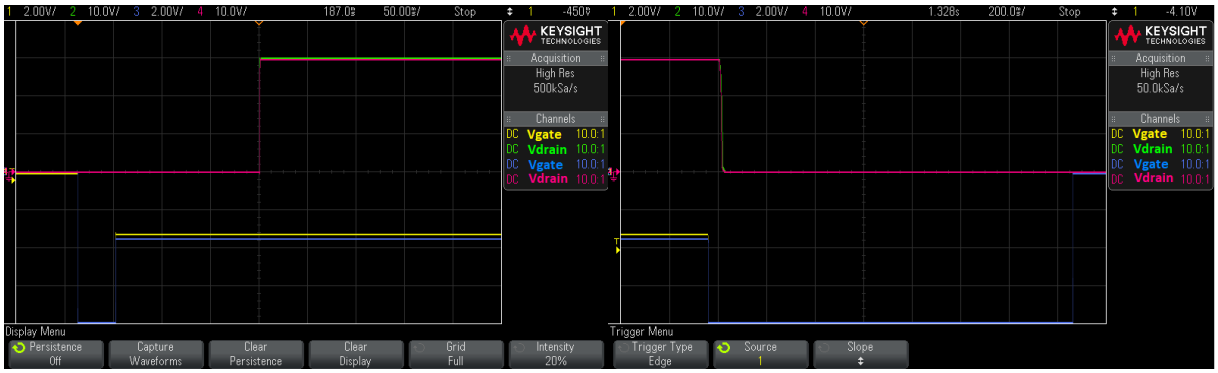

Figure 8: Measured start (left) and stop (right) sequence

4 CONCLUSION

Prototype of the power sequencer was built and it turn out, that it is very valuable device during designing and testing of the various kind of RF power amplifiers and predistorters, mostly for ease of the GaN transistors to be destroyed and ability to set various biasing parameters during development.

ACKNOWLEDGEMENT

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