

DESIGN AND IMPLEMENTATION OF WAVE DIGITAL FILTERS

Marcela ANTOŠOVÁ, Vratislav DAVÍDEK

Department of Circuit Theory

Czech Technical University in Prague

Technická 2, 16627 Praha 6, Czech Republic

Abstract

One of possibilities of the Wave Digital Filters (WDF) design is using the classical LC-filters theory. The aim of this paper is to demonstrate the design of WDF from the LC filter and the implementation of WDF on the fixed-point digital signal processor. The theory of wave digital filter has been developed by using the classical scattering parameter theory. The theory of ladder filters is well-known, and so our present problem can thus be reduced to a problem how to replace the L and C elements of the filters by adaptors and delay elements, adders and multipliers.

Keywords

Wave digital filter, parallel adaptor, serial adaptor, LC reference filter, implementation, digital signal processor.

1. Introduction

The purpose of this paper is to show that it is possible to design digital filters according to structures which are closely related to those used for the realization of LC filters. The classical lossless LC filter inserted between resistive terminations from which a wave digital filter is derived will be called reference *filter* here.

Wave filters are simulated at most by lossless ladder or lattice configurations. In the design of wave digital filters the first step is to design the appropriate reference filter to meet the desired frequency specification. In the next step a block diagram of the corresponding reference filter must be derived. Wave filters are usually not transformed directly to wave flow diagram or simply to wave digital filter. The derivation of a wave flow graph from an analog reference filter can be achieved in two steps. In the first step the wave flow graph should be derived for one port circuit elements as resistors, capacitors, inductors. In the second step the models of single circuit elements must be appropriately interconnected by using special elements called adaptors. In the last step should be implemented the

digital wave filter flow graph in to special hardware as signal processor, SC structure, FPGA structure etc.

In order to establish the correspondence between a WDF and its reference filter we must at first observe that this can be done in the frequency ψ domain [1], [2], [5] using the bilinear transform

$$\psi = \frac{z-1}{z+1} = \tanh \frac{sT}{2}, \quad z = e^{sT}. \quad (1)$$

A wave digital filter is a digital system with two ports characterized by relations between voltages and currents on these ports. Let us assume the instantaneous quantities $u = u(t)$ for voltage and $i = i(t)$ for current. The instantaneous wave quantities are then defined by relations

$$a_j = u_j + R_j i_j, \quad b_j = u_j - R_j i_j, \quad (2)$$

where a_j and b_j are incident and reflected voltage waves on the j -th port, R_j is a port resistance. Correspondingly, we can consider steady-state wave quantities A_j, B_j respectively in the form

$$A_j = U_j + R_j I_j, \quad B_j = U_j - R_j I_j. \quad (3)$$

Wave digital filters have very useful properties [1]. Some of the interesting features of an one dimensional WDF are stability for a wide range of the multiplier coefficients under linear conditions, an easy extension of WDF to any number of dimensions, low sensitivity to round off errors and a wide dynamic range.

2. Building Blocks

A typical WDF design starts with a prototype LC network and each element in the LC network is transformed into an equivalent digital element. The transformation is carried out using wave quantities defined above. In the reference ψ domain a capacitance and an inductance are described by equations

$$U_C = RI/\psi, \quad U_L = \psi RI. \quad (4)$$

The wave normalization resistance R is linked to the value of the capacitor and the inductor. Let us now select for the port resistance the same value as in Eqn. (3). To find a relationship between the wave-voltage signals we substitute (1) and (3) to (4) and choose $R_j = 1/C, R_j = 1/L$ [1], [3], [5].

We obtain relations for wave quantities in the form

$$B = z^{-1} A \quad \text{and} \quad B = -z^{-1} A. \quad (5)$$

The transformation of basic L and C elements used in analog and digital wave filters was derived in [1], [2] and are demonstrated in Fig. 1.

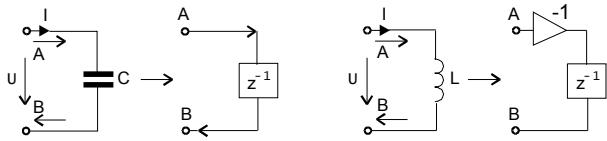


Fig. 1 Basic elements of LC filters and their transformation into the z-plane.

2.1 Simulation of interconnections

In order to fully establish an equivalence between reference filter and a corresponding wave digital filter it is necessary also to simulate the wire interconnections [1], [2], [6]. These interconnections are simulated by special multiports, called adaptors. The wave flow diagrams of wave digital filters are simulated at commonly using two-port or three-port adaptors. In this paper we use for WDF design and implementation only three-port adaptors.

These adaptors forming the main building blocks of WDFs are divided into series and parallel adaptors.

2.1.1 Parallel adaptor

A parallel adaptor simulates the parallel connection of multiports having a port resistances R_j ($j = 1, 2, \dots, n$). It must be possible for the latter to take arbitrary values since these are usually fixed by whatever element is connected to the corresponding port.

The incident waves a_j and reflected waves b_j are related to the voltages u_j and currents i_j by (2). From the equalities for the three-port adaptor

$$\begin{aligned} u_1 &= u_2 = u_3 \\ i_1 + i_2 + i_3 &= 0 \end{aligned} \quad (6)$$

we can get [1], [2], [6] coefficients of parallel adaptor

$$\alpha_j = \frac{2 G_j}{G_1 + G_2 + G_3}; \quad G_j = \frac{1}{R_j}, \quad (j = 1, 2, 3) \quad (7)$$

If for any port, say k -th port, incident and reflection waves are mutual independent then the port k is reflection-free. Reflection-free ports play an important role in WDFs design. The absence of reflection in port n is represented on adaptors in Fig. 2a) and c).

2.1.2 Series adaptor

A series adaptor simulates the series connection of n ports, with port resistances R_j ($j = 1, 2, \dots, n$). From the relations for voltages and currents of a three-port series adaptor

$$\begin{aligned} u_1 + u_2 + u_3 &= 0 \\ i_1 = i_2 = i_3 & \end{aligned} \quad (8)$$

we obtain [1], [2], [6] equation for series adaptor coefficients

$$\beta_j = \frac{2 R_j}{R_1 + R_2 + R_3}, \quad (j = 1, 2, 3) \quad (9)$$

According to [1], [2] the three-port parallel and serial adaptors require maximally $n-1$ multiplication. Structures of three-port adaptors used in WDF's are shown in Fig. 2.

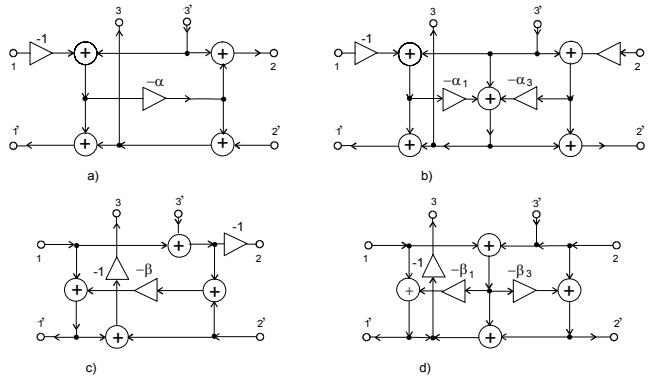


Fig. 2 Structures of WDF adaptors: a) parallel reflection-free adaptor, b) parallel adaptor, c) series reflection-free adaptor, d) series adaptor.

3. Design of wave digital filter

In previous paragraphs we have seen how various types of elements and adaptors can be used as building blocks for constructions of wave digital filters.

From the filter theory it is known that LC ladder filters are built by cascading of a certain number of elements. In our example let us consider a low pass LC reference filter. We assume the magnitude response to be approximated using Chebyshev approximation. This magnitude response has ripples in the passband and it is smooth in a transientband and in a stopband.

Let us consider the following filter specification:

passband	ripples	$a_{max} = 1 \text{ dB}$,
	frequency	$\omega_p = 100 \text{ s}^{-1}$
stopband	attenuation	$a_{min} = 15 \text{ dB}$,
	frequency	$\omega_s = 250 \text{ s}^{-1}$.

This specification corresponds to the filter order $N = 2$, see Fig. 3. LC reference filters of an even order (in our case $N=2$) approximated by Chebyshev have not an equal value of source and load impedance. This fact corresponds to a not zero value of attenuation for $\Omega = 0$. Normalized values of the analog filter elements was designed by procedure mentioned in [9] and [10]. Values of components are

$$L = 1.82193, C = 0.68501.$$

The second-order analog LC reference filter has a source and load normalized impedances of $R_0 = 1$ and $R_Z = 2.659$. These values can be determined according [9] and [10] or computed using some programs for filter synthesis for example SYNTFIL. The reference structure in Fig. 3 contains a series adaptor S1 and parallel adaptor P2.

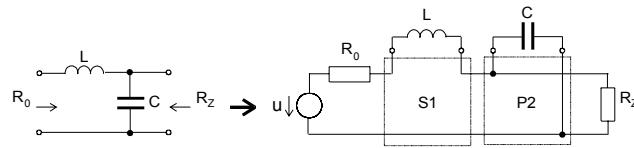


Fig. 3 Analog reference LC filter ($N=2$) and interconnection of basic elements using adaptors S1, P2.

Fig. 4 shows the designed WDF structure with symbols used commonly for adaptors. The capacitance and inductance of the filter were replaced by delay elements.

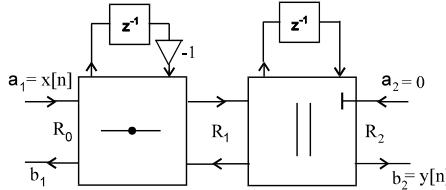


Fig. 4 Second-order WDF with symbols of adaptors.

Let us replace the symbols of adaptors by implementation structures from Fig. 2 c) and b). The coefficients of a series adaptor β and of a parallel adaptor α_1 and α_3 were calculated using (7), (9) for normalized port resistances R_0 , R_2 and R_1 , where $R_1 = R_0 + Z_1(1) = 1 + 1.82193 = 2.82193$.

The coefficient values of a designed WDF are

$$\beta = \frac{R_0}{R_0 + Z_1(1)} = 0.3544, \quad \alpha_1 = \frac{2G_1}{G_1 + Y_2(1) + G_2} = 0.5007$$

$$\alpha_3 = \frac{2G_2}{G_1 + Y_2(1) + G_2} = 0.5313$$

where $Z_1(1) = L$ and $Y_2(1) = C$ for $\Omega = 1$.

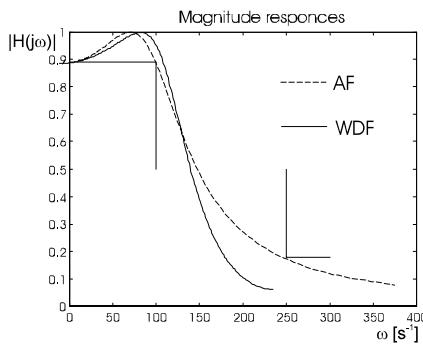


Fig. 5 The comparison of magnitude characteristic of analog and wave digital filter.

Magnitude responses of an analog filter (AF) and a wave digital filter (WDF) are presented in Fig. 5.

4. WDF Implementation

Digital filters as digital processing algorithms can be implemented in different manners, for example using

- a) general purpose processors
- b) programmable logic arrays,
- c) special IOs,
- d) digital signal processors, etc.

In our implementation we have used fixed-point signal processor TMS320C50. We debugged the WDF algorithm using software simulator and by real-time implementation using DSP starter kit.

The Analog Interface Circuit (AIC) of the evaluation starter kit was used to input the sampled sequence. According to the frequency bandwidth of the designed WDF, was the AIC configured through software to sample at the rate of 8.066 kHz.

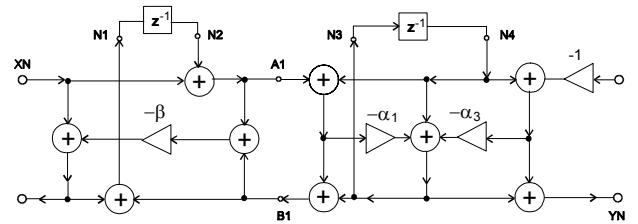


Fig. 6 Implementation structure of the second-order WDF.

The initialization part of assembler code includes configuring the AIC, setting the 2-complement arithmetic of DSP, setting of an overflow mode and spacing of filter coefficient values in to program memory.

The executable main program was assembled from WDF structure. In Fig. 6 is shown the block diagram of the second-order WDF, designed in the previous section. In this diagram there are marked the nodes connecting with internal variables. The WDF can be then characterized using difference equations in particular nodes as follow

$$\begin{aligned} A1 &= XN + N2 \\ N1 &= XN - \beta(A1 + B1) + B1 \\ N3 &= -\alpha_1(A1 + N4) + N4 - \alpha_3 N4 \\ B1 &= A1 + N3 + N4. \end{aligned} \quad (10)$$

The state-variables $N1$ and $N3$ describing the signals on an inputs of delay elements are saved in internal RAM, where is realized linear delay line

$$\begin{aligned} N1 &\rightarrow N2 \\ N3 &\rightarrow N4. \end{aligned} \quad (11)$$

State-variables $N1$ and $N3$ can be expressed as functions of variables XN , $N2$ and $N4$

$$\begin{aligned} N1 &= XN K_1 + N2 K_2 + N4 K_3 \\ N2 &= XN K_4 + N2 K_5 + N4 K_6 \\ YN &= N3 + N4 \\ N1 &\rightarrow N2 \\ N3 &\rightarrow N4. \end{aligned} \quad (12)$$

where constants K_1 to K_6 depend on WDF coefficients

$$\begin{aligned} K_1 &= 2 - 2\beta - \alpha_1 + \alpha_1\beta & K_4 &= -\alpha_1 \\ K_2 &= 1 - 2\beta - \alpha_1 + \alpha_1\beta & K_5 &= -\alpha_1 \\ K_3 &= 2 - \alpha_1 - \alpha_3 - 2\beta + \alpha_1\beta + \alpha_3\beta & K_6 &= 1 - \alpha_1 - \alpha_3 \end{aligned}$$

Difference equations (16) were implemented into assembler of DSP and the designed WDF was analysed. In Fig. 7 are shown impulse and magnitude responses computed on digital signal processor with word-length of 16 bits.

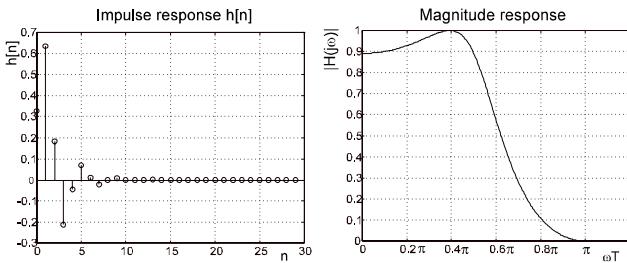


Fig. 7 Impulse and magnitude responses of the simulated WDF, given from digital signal processor.

The limited word length 16 bits of used signal processor causes quantization errors on the filter output. The quantization error $e(\omega)$ was determined as a difference between a full precision magnitude response $|H_F(\omega)|$ computed in Matlab and a magnitude response $|H_I(\omega)|$ of an implemented filter

$$e(\omega) = |H_F(\omega)| - |H_I(\omega)|. \quad (13)$$

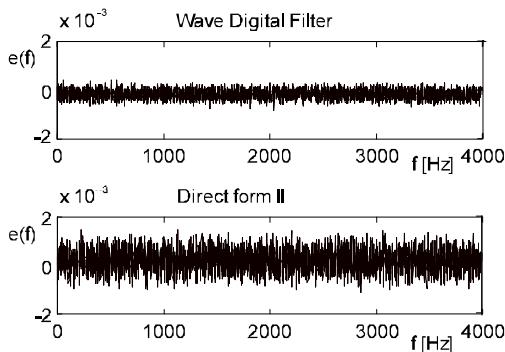


Fig. 8 Comparison of quantization errors of implementations in second-order WDF and the direct form II.

Fig. 8 shows that the quantization error of the WDF of second-order in its rms value is approximately three-times smaller in comparison to digital filter of direct form II structure.

5. Conclusion

The WDFs can be realized using large number of different structures according to the different realization possibilities of the analog reference filters. We have presented

the design and implementation of the WDF built from reactance ladder structure. WDF of this type has an advantage in the approximately similar low passband and stopband sensitivity to the coefficient variations. Quantization errors are smaller in comparison to direct structures. Another realization WDF structures, followed by authors, are lattice structures. They have very low passband sensitivity however, the sensitivity at stopband can be higher.

References

- [1] FETWEIS, A: Digital Filter Structures Related to Classical Filter Networks. *AEU*, Band 25, 1971.
- [2] FETWEIS, A., MEERKOETTER, K. On Adaptors for Wave Digital Filters. *IEEE Trans. ASSP-23*, 1975.
- [3] HASLER, M., NEJRYNK, J. Electric Filters. Artech House, Inc., 1986
- [4] FETWEIS, A. Wave Digital Filters: Theory and Practice, Fellow. Proceedings of IEEE, vol. CT-19, Feb. 1986.
- [5] UNBEHAUEN, R., CICHOCKI, A. MOS SC and Continuous-Time Integrated Circuits and Systems, Springer-Verlag, 1989.
- [6] ANTOŠOVÁ, M. Wave Digital Filters. Ph.D. equiv. thesis, CTU Prague, 1992 (in Czech).
- [7] PŠENIČKA, B., UGALDE, F. G., SAVAGE, J., DAVÍDEK, V.: Design of State Digital Filters. *IEEE Trans. on Signal Processing*, vol. 46, No. 9, September 1998.
- [8] CHUNG, J., PARHI, K. Pipelined Lattice and Wave Digital Recursive Filters. Kluwer Academic Publishers, Boston, 1996.
- [9] DAVÍDEK, V., LAIPERT, M., VLČEK, M. Analog and Digital Filters. Monografie CTU, Prague, 2000 (in Czech).
- [10] WINDER, S. Filter Design. Newnes-Butford Techn. Publishing, 1998.

About authors

Marcela ANTOŠOVÁ was born in Prague 20th March 1965. She received M.Sc. and Ph.D. equiv. degrees both in Telecommunications in 1988 and 1992 respectively at the CTU Prague. Since 1988 she is an Assistant Professor at the Department of Circuit Theory at the Faculty of Electrical Engineering of CTU in Prague.

Vratislav DAVÍDEK was born in Prague 5th April 1942. He received M.Sc. equiv. degree in control technique in 1964 and Ph.D. equiv. degree in Radio Electronics in 1977 at the CTU Prague. Since 1993 he is an Associated Professor at the Department of Circuit Theory of the Faculty of Electrical Engineering of CTU in Prague.