HIGH POWER SINUSOIDAL GENERATOR WITH USE OF PCM-PWM CONVERTER

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Abstract: This paper deals with the study of generating a sinusoidal signal with output power up to hundreds of watts. Selected microcontroller calculates sinusoidal data which are used as the input for PWM module. Four outputs of the module directly drive four transistors of H bridge which ensures high output power. Purposed method of calculating integer sinusoidal samples allows changing the frequency at any time with minimal latency.

Keywords: sinusoidal generator, Class-D amplifier, fast calculation of sine function

1 INTRODUCTION

There are many branches in electronic where sinusoidal generator with high output power is main part of the device. This paper is based on the generator developed for electromagnetic vibration exciter. However, the same design can be used in car sockets which convert 12 V battery voltage to 230 VAC or some another equipment working with AC supply.

The project is built on microcontroller; therefore, digital to analogue converter needs to be used. Since high output power (up to 1 kW, but actual output power depends on the realization) is required, a power amplifier has to be placed in front of the output. In order to minimize power losses and thus increase efficiency Class-D amplifier has been selected. Chain of DAC and power amplifiers can be substitute by power stage of a Class-D amplifier (H bridge) driven directly from the Pulse Width Modulation (PWM) module of the microcontroller. This substitution brings higher harmonics components in the output signal. On the other hand, it saves some components and gives more freedom of driving the bridge; therefore, the H bridge method has been used.

2 HARDWARE BLOCK DESIGN

Figure 1 shows simplified block diagram of the system and its real implementation. Following subchapters details each block.

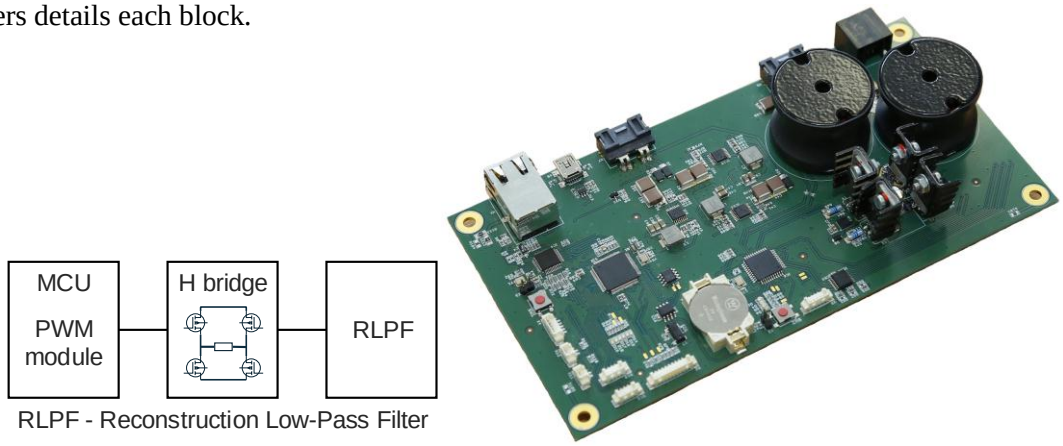

Figure 1: Hardware block diagram and real implementation of generator.

2.1 PCM – PWM CONVERTER

Pulse-Code Modulation – PWM (PCM-PWM) converter creates PWM signal directly from digital signal representation; such signal is commonly called Uniform PWM (UPWM) [1]. The difference between this method and PWM signal acquired by sampling analog signal with a triangular or sawtooth wave (Classical class-D amplifier) is that the UPWM generates a harmonic content of fundamental frequency of input signal. In addition, both have periodic copies of baseband at multiplies of PWM frequency (reciprocal value of PWM period; acting as sampling frequency) [1].

As the author of [1] states another downside of this method is a requirement on a high-speed clock signal of PWM module. The reason is that the resolution of source data expressed as the number of bits N has to be transformed into time resolution of PWM signal. This means that PWM period has to consist of 2^N steps. The module's clock source frequency for single-sided PWM can be calculated as follows [1]:

$$f_{CLK} = f_s \cdot 2^N , \tag{1}$$

where f_S [Hz] is sampling frequency of source wave. With the maximum clock frequency of selected microcontroller (dsPIC33EV256GM004) of the 140 MHz and acceptable bit resolution of 11 bits in mind source signal sampling frequency has been fixed to 68 kHz. Frequency spectrums based on simulation are depicted in Figure 2 [2]. In the line graph at the top is shown digitalized input signal. The second spectrogram spectrum of PWM acquired by PCM-PWM converter is presented. As mentioned earlier, harmonic content of fundamental 5 kHz signal and modulation products can be seen.

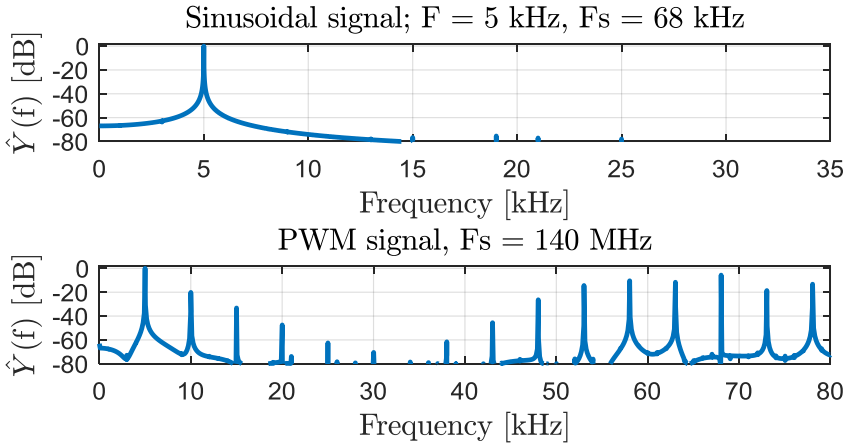

Figure 2: Normalized single-sided spectrums of input sinusoidal signal and PWM signal.

Due to harmonic distortion, 5 kHz has been fixed as the maximum frequency. It is clear that with decreasing fundamental frequency, level of harmonic content decreases as well. For example, the first harmonic frequency of the fundamental frequency of 500 Hz is about 35 dB smaller.

2.2 CLASS-D AMPLIFIER

This design borrows only power stage from a Class-D amplifier, i.e. H bridge. Every single transistor of the bridge is driven by the PWM module. It provides more possibilities to control the process. For example, specific dead time can be adjusted, a load can be shorted or not connected, and mode of operation can be selected just by editing the firmware.

Looking at Figure 3, the most obvious principle of H bridge is alternative switching the crossed transistors. That is while T1L and T2H are switched on, T1H and T2L are switched off; in the next period, the opposite transistors are switched on. This way there are only 2 possible levels across the load. Also, with 0.5 duty cycle, the current flows through load equally and there is observed no useful effect. This switching method is classified as class AD [3].

The second approach to switching transistors builds on an inverted form of the input signal for driving the second branch, more details provide Figure 3 [3]. In this instance, the driving waveform for the second transistor is inverted in level as well as in time within the PWM period. This adds the third state in differential voltage across the load and so eases requirements on the output filter.

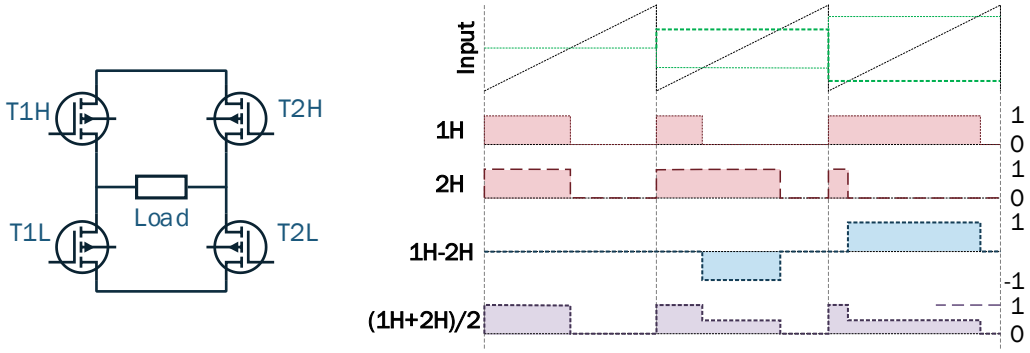

Figure 3: Schematic of H bridge and Class BD oper.; 1H, 2H drive transistors T1H, T2H.

Usually, PWM modules dispose of several channels and outputs, where two outputs can be bind together in a complementary mode. These two outputs cover one half of the bridge; another channel with 2 outputs can be used for the second half. For the BD mode, time base can be the same for both channels and only duty cycle registers have to be updated. Once the duty cycle is calculated for the first channel; the result with minor adjustment (*periodRegister* – *dutyCycle1*) can be used also for the second channel. The use of the periphery is necessary because even a slight time deviation between samples is notable in the output signal.

This method of driving transistors also allows implementing feedback from any digital or analog sensors. However, the speed of feedback is limited by the PWM period.

2.3 RECONSTRUCTION FILTER

In [4] are described calculations of reconstruction filter. The process is based on audio design, but it can be applied to this design as well. Schematic is presented in Figure 4. Care must be taken with capacitance of capacitors; not only that high capacitance increases Q factor, but it also requires enough capacitance to blocking supply voltage. If supply voltage is not blocked properly switching transistors on will draw peak current from the supply source causing considerable drop of the supply voltage. Since the power supply rejection ratio is essentially 0 dB, this peak voltage drop will be also present in the output.

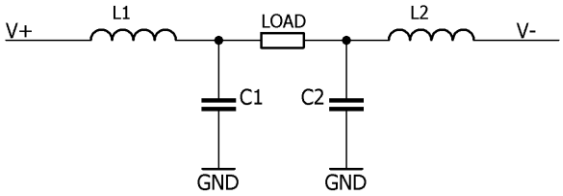

Figure 4: Schematic of reconstruction filter.

3 DUTY CYCLE SAMPLES

In order to enable setting output frequency, the firmware must calculate new sinusoidal sample within PWM period. This is because storing samples for sinusoids of every frequency is impossible and pre-calculating period of the desired sine curve is impractical; it is needed $M = f_{out} / \gcd(f_{out}, f_s)$ periods to seamlessly repeat samples, where f_s (Hz) is sampling frequency (1/ *PWMperiod*) and f_{out} (Hz) is integer output frequency. Output frequencies with decimal part represent even more difficulties. Of course, there is a point in which it would be possible to end sequence of pre-calculated samples with minimal error, but it would mean a different number of elements for each frequency.

3.1 CALCULATION

Calculation of sinusoidal value with use of native C function sin() takes the target MCU about four times longer than PWM period. That makes this approach unsuitable and more effective method must be applicated.

A look up table with pre-calculated sinusoid is a fast way to get a sinusoidal curve, but to get actual value of sin(x) additional calculation have to be performed. The reference table has been created by dividing the period of sine function into $360 \cdot N$ parts, where N depends on available program memory and tolerable error. Because of sinusoidal symmetry, it is sufficient to store only a quarter of the sinusoid. This adds a tiny complication but allows to reach $N = 900$ for target MCU.

Using the reference table, the calculation of new sample is done by adding a constant to a cumulative pointer. Sinusoidal value is read from the table at the index equal to the cumulative pointer. If the pointer is greater than the length of the reference table, this length of the table is subtracted from it. The constant is different for each frequency and can be determined by the equation [2]:

$$Add_{Index} = \frac{f_{out} \cdot N_{ref} \cdot N_{pre}}{f_s}, \qquad (2)$$

where Add_{index} (-) is added to the cumulative pointer to get next sample, N_{ref} (-) is the length of reference table and N_{pre} (-) represents an increase of precision for integer division (N_{pre} shall be 2^N). Since calculating with floating point format is not beneficial in terms of speed and acceptable error is required, the precision increase is necessary to minimize rounding errors.

A downside of the cumulative method in combination with taking rounded integer part from the result of (2) is that the error of a maximum of 0.5 is cumulated with every sample. This means that after 1 second ($68 \cdot 10^3$ samples) the cumulated error would be $34 \cdot 10^3$. Fortunately, samples are divided by N_{pre} before application, hence the error is divided by N_{pre} as well. For integer output frequencies the situation is always the same, at the end of every second accumulated error is reset to zero. The described method is illustrated in Figure 5. However, for non-integer frequencies accumulated error may not be reset (reset is performed if AccumulativePointer / N_{pre} is equal to zero) before it exceeds the value of 2^{16} (N_{pre}). This causes a slow phase shift. If that is an issue, additional corrections have to be made or the following method can be used.

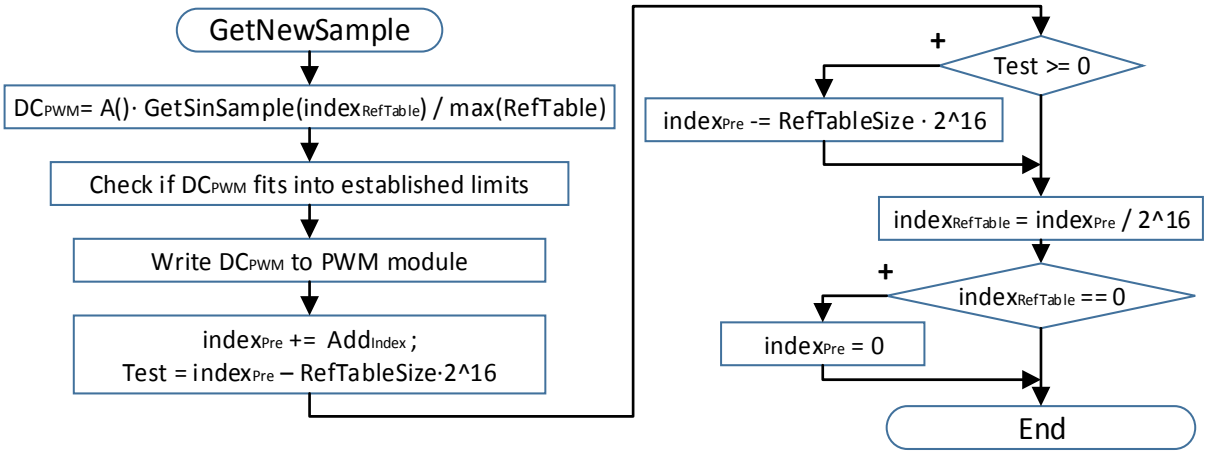

Figure 5: Flowchart of sinusoidal calculation algorithm.

There is no error accumulation when the numerator of (2) is multiplied by *Index* (for each sample the index is incremented by 1) and calculation of each sample is done according to edited (2). Based on a simulation the time required for the execution of edited (2) is about 11 µs, which is ten times greater than the time needed to add two numbers with additional logic (without phase shift correction). Therefore, the second method is not suitable for target MCU. Phase shift correction

could be implemented as a combination of both mentioned methods; edited (2) would be calculated only for every *n*-th sample, where n is between 1000 and 100 000. The accumulated error would be reset in these *n*-th samples (the accumulator would be set to result of edited (2)).

4 MEASUREMENT RESULTS

The spectrum of the measured 500 Hz sine wave is shown in Figure 6. The first harmonic frequency is about 65 dB and the second about 45 dB smaller. Because of inductive character of the vibration generator, which helps to filtrate higher frequencies, measured results are better than results based on simulation. For frequency greater than 2 kHz the generator's amplitude is only a few μm.

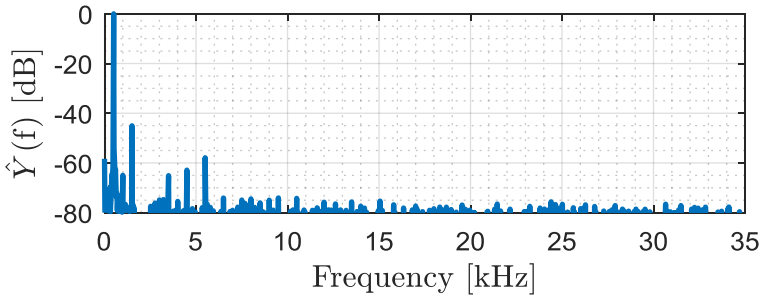

Figure 6: Normalized single-sided spectrum of a measured 500 Hz sinusoid.

5 CONCLUSION

This paper deal with the study of generating a sinusoidal waveform with an output power of hundreds of watts. The power amplifier is realized as H bridge, where each transistor is driven by PWM module of MCU. Sinusoidal integer samples for duty cycle register are calculated directly on board. For fast calculation, all calculations are done in integers. Switch to new frequency is performed at the beginning of the period when new Add_{Index} is ready, i.e. at the latest after one period of current frequency. The manufactured device is able to deliver about 400 W to load with supply voltage about 30 V. The generator can be controlled via Ethernet or USB interface.

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