CONTROL UNIT FOR CUBESAT

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Abstract: The aim of the project was to design a CubeSat control unit. The board is composed of commercial parts yet reliable in the space environment. Because of its benefits, an FPGA was selected as the core of the board. The FPGA is periodically checked for errors and reset if an error is found. The unit has various sensors to monitor its condition and can do necessary measures. Two MRAMs allow to store a golden bitstream and upload new bitstream in flight.

Keywords: Space, CubeSat, Control Unit, Radiation, FPGA

1. INTRODUCTION

CubeSat are defined as U-class spacecraft with dimensions of 10x10x10 cm (1U) and weight up to 1.33 kg per unit. Because of their small volume and weight, CubeSat are significantly specialized. In most cases, there is not a need for high computing power. Therefore, the most of the control units use microcontrollers as CPU. If there is a need for faster signal processing, parallel processes or high computing power, a customer has to develop suitable board by himself as same types are not available on the market. That significantly increases overall cost and development time. The aim of this project was to design a control unit which can fill the gap on the market.

2. SPACE ENVIRONMENT

Understanding of space environment is necessary to reduce failure possibility. One of the most important aspects of the environment is radiation. The ionizing particles may generate failures in integrated circuits and semiconductor devices, as they can change a transistor state. These failures can be transient or permanent, depending on charge and location of the interaction [1].

The most frequent are Single Event Effects (SEE). They are considered as Soft Errors, as their effect is only temporary. The SEE can be divided to Single Event Upset (SEU) and Single Event Transient (SET). The SEU causes a change of state of a memory cell. Information, saved in the memory, is corrupted but the logic cell works normally. When new information is written, the logic cell will contain the new information unless another SEU occurs. The SET happens when radiation causes a voltage spike on an output of a circuit. The effect is only temporary, but the output can be latched during the spike and lead to serious failures. Radiation can also open parasitic bipolar transistors, which leads to destruction of the chip [2].

To reduce overall cost, CubeSat are mostly made by commercial parts. The commercial electronics is mostly made without any special protection against radiation and can survive radiation usually only up to 10 krad(Si) [1].

3. CONTROL UNIT

Designed board (shown in Figure 1) uses an automotive version of Spartan 6 FPGA. The FPGA does not have any additional protection and therefore is vulnerable to radiation. The circuit use CRC to constantly check FPGA's configuration memory. Also, a separate watchdog circuit is used

to check for SEE errors. If any error is found, the FPGA is reset and reprogrammed from a separate memory.

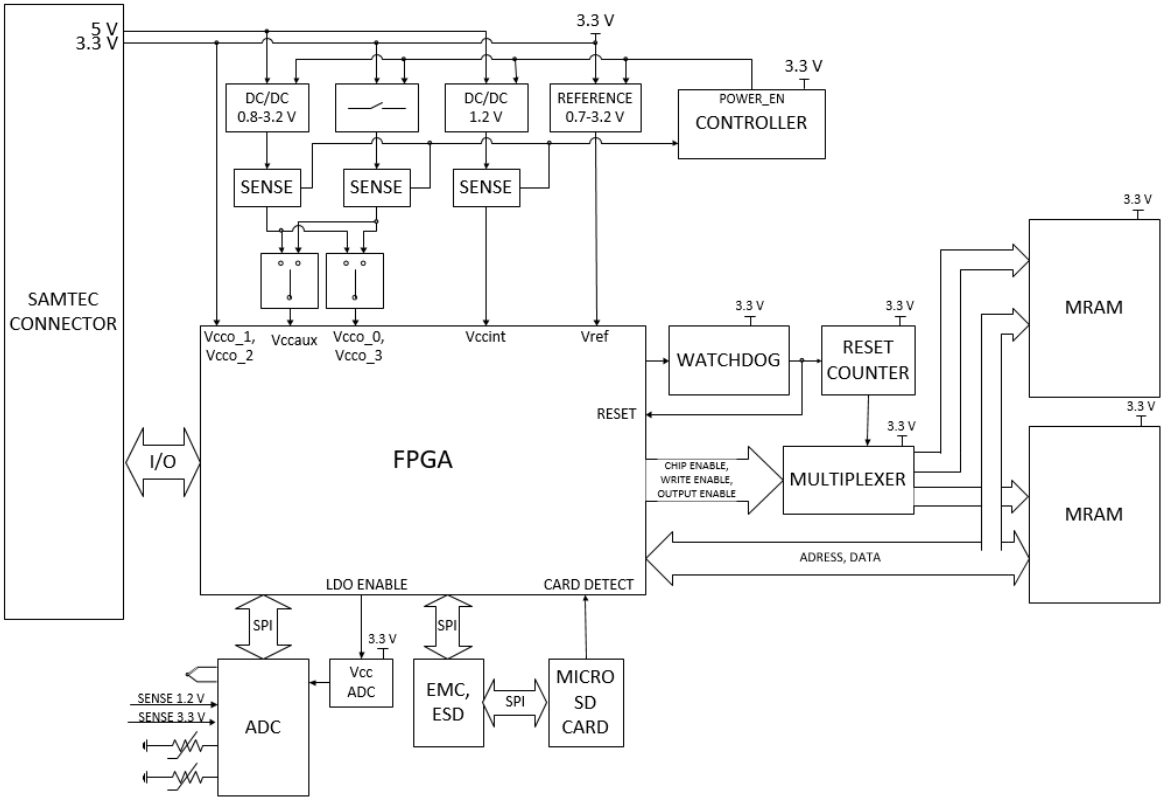

Figure 1: Block diagram of the control unit

As the FPGA is SRAM based, there is a need for separate bitstream storage. The design uses two MRAM memories for storing the bitstream. Their biggest advantage is the immunity to radiation and therefore they can be used to safely store data in the radiation environment.

The first memory is used to store proven, tested and errorless golden bitstream. The memory has a Write enable pin. The voltage on the pin can be set to zero (active mode) only by plugging a jumper in. The bitstream is uploaded to "golden" memory before launch. Then the jumper is unplugged and the bitstream cannot be changed. This solution provides reliable bitstream storage.

The second MRAM can be used to store a new version of the bitstream. It can be deleted, changed or uploaded during flight. Also, any user data can be stored to the second MRAM (and/or MicroSD card).

If any error is found, the watchdog timer resets the FPGA. Afterward, the FPGA is configured from the second MRAM. There can be an event when the configuration from the second MRAM fails. The reset can take place while uploading the bitstream, new code can incorporate an error and other faults. The FPGA can be stuck in reconfiguration loop and the whole CubeSat is unusable. To prevent this outcome, the board counts the number of configuration cycles. If the FPGA is reset three times in a row, a multiplexer to selects the first MRAM with the golden bitstream.

3.1. POWER SUPPLY

The CubeSat specification requires that all satellite must provide 5 V and 3.3 V supply rails. The board uses two DC/DC converters for powering FPGA's, one for core and second for I/Os. The voltage for I/Os can be changed so that any FPGA's I/O standard can be used. If only 3.3V standards are required, it is possible to bypass the second converter by connecting its output to V_{CCAUX}, which decreases overall power consumption by 40 %. All supply rails are monitored

and shut down in any case of short-circuit. Turning supplies off is the only solution if parasitic transistors are opened.

The board consumes less than 100 mA in total with current digital design, which is low enough to be powered in 1U CubeSat. The most of CubeSat use batteries with several Ah capacities, therefore the FPGA can be configured to do desired tasks (which need more power) and then be reconfigured back to low power state.

3.2. TELEMETRY

The circuit uses 24-bit ADC for telemetry. The ADC measures voltages of the supply rails, current consumption, and temperature on the board.

The main way how parts dissipate their heat is mostly through heat convection. This way is not present in space vacuum; therefore, the power dissipation is a big concern. The LDOs and converter have internal temperature sensors, which shut them down in a case of high temperature, yet another sensor can warn the FPGA early and some measures may be used. The ADC has two thermistors, which measure temperature on the board. As the main heat transfer in space is by conduction, a thermistor placed close to a part can sense the part's temperature. Thermistors are used to measure the temperature of the FPGA and DC/DC converters. Connection to thermocouple is also provided. The thermocouple can by connected directly to FPGA's package or any other place on the board.

3.3. PCB AND DIGITAL DESIGN

The circuit is placed on 6-layer 10x10 cm PCB which complies CubeSat standards. The PCB has a copper pour in all layer and uses via stitching to reduce EMI and provide maximize heat conduction. It also reduces deflection of the board.

The digital design depends on mission and requirements of a customer. Its purpose in this project is to test and verify all the functions of the unit. The unit periodically measures and stores its telemetry, can store bitstream in MRAM memories and allows storing user data. The FPGA uses UART interface for communication, but other interfaces can be used. The FPGA has 68 I/O pins connected to the connector. The digital design consumes about 5 % of logic, which leaves enough resources for customer's application.

Software-Implemented Error Recovery, Profile-Guided Code Transformation, and other techniques can be used to further improve error mitigation [2].

4. SUMMARY

Unlike other units on the market, this control unit has faster signal processing, parallel processes, and high computing power. It provides radiation-resistant bitstream storage, reliable reset and reconfiguration and bitstream upload in-flight. The FPGA and its interfaces can be designed according to customer's requirements which would not be possible with microcontrollers. The control unit can be used for various missions in Low Earth Orbit and beyond (with additional shielding).

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