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***Abstract*—This contribution presents a design of a current–mode fractional–order electronically controllable integrator which can be used as a building block for a design of fractional–order (FO) circuits. The design is based on a 2nd–order Follow–the–Leader–Feedback topology which is suitably approximated to operate as an integrator of a fractional order. The topology is based on Operational Transconductance Amplifiers (OTAs), Adjustable Current Amplifiers (ACAs) and Current Follower (CF). The proposed structure offers the ability of the electronic control of its fractional order and also the electronic control of the frequency band. Simulations in Cadence IC6 (spectre) and more importantly experimental measurements were carried out to support the proposal. If wider bandwidth where the approximation is valid is required, a higher order structure must be used as also shown in this paper by utilization of a 4th–order FLF topology.**

Keywords—current mode, electronic control, fractional order, fractional–order emulator, integrator

I. INTRODUCTION

One of the current research topics revolving around the analog circuit design is a topic of synthesis of fractional–order (FO) circuits and their utilization for modelling of systems with fractional–order characteristics, measurement of various samples in medicine and agriculture, or the implementation in the electrical engineering [1]. The FO systems can provide wider range of application in diverse technical areas due to their ability to provide characteristics in between integer–orders in comparison to standard (integer–order) circuits.

The most typical approach to design of electrical circuits with FO characteristics is the employment of so–called Fractional–Order Elements (FOE). The FOE can be understood as a passive element with the slope of the attenuation of $20\times\alpha$ dB/decade, where parameter α stands for a real number in range $0 < \alpha < 1$. Similarly, the phase shift of such element is equal to $90\times\alpha$ degrees. The FOE usually has the character of a FO capacitor (element with its character being between a capacitor and resistor). The impedance of such element is given as $Z_{C\alpha} = 1 / \boldsymbol{s}^{\alpha}C_{\alpha}$, where $\boldsymbol{s}^{\alpha}$ represents the FO Laplacian operator and C_{α} is a pseudo–capacitance with units of Farad/sec$^{1-\alpha}$ [2]. There are three general ways how to obtain the FOE. The first technique is based on the fabrication of these elements [3–6] on various basis (electro–chemical [3–4], resistive, capacitive and conductive layers on silicon [5] organic materials [6], for instance). The main disadvantages of this approach are the fact that the fabrication of these solutions is a complex and expensive process, commercial unavailability and the absence of the electronic control of the resulting order. The second method comprises the substitution of the FOC by RC ladder structures with suitably selected values [2], [7–9]. There are multiple topologies of the RC ladder structures such as Foster I, Foster II, Cauer I, and Cauer II, for instance [7]. The selected approximation of the FO Laplacian operator $\boldsymbol{s}^{\alpha}$ will determine the values of resistors and capacitors within the RC structure. The advantage is the requirement of only basic parts (standard resistors and capacitors). The drawback is the fact that we need specific values in comparison to the values of resistors and capacitors which are available only in fabrication series (in case of discrete implementation). Thus, the serial/parallels combinations are usually necessary. Moreover, the electronic control of the order is not available similarly to the previous approach (the values of the RC structure need to be recalculated for each value of FO). The last general way involves the use of a topology with electronically controllable active elements [10–15] to approximate the function of a FOE [10–12] or a FO building block (to behave as a FO integrator/differentiator) [13–15]. The disadvantage is higher complexity of the resulting structure and necessity of active elements. The advantage, on the other hand, is the presence of the electronic control of the order which can be easily set depending on the desired value of α. Table I provides the comparative summary of mentioned FO emulators ([10–15]).

If considering valid operational bandwidth within range of ±5° (in case of the phase shift) from the ideal value, the solutions in [11], [13] and [14] provide less than two decades

TABLE I. COMPARISON OF RECENLY INTRODUCED FO EMULATORS WITH ELECTRONICALLY CONTROLLABLE ORDER

Ref No.	[10]	[11]	[12]	[13]	[14]	[15]	Fig. 2
Number of active/passive elements	9/10	9/2	3/1[a]	N/A[b]	10/2	14/5[c]	6/2 10/4[d]
Usable bandwidth	2 decades	< 2 decades	4 decades	< 2 decades	< 2 decades	< 3 decades	2 decades/ < 3 decades
El. BW shift control	Yes	Yes	N/A[e]	N/A[e]	N/A[e]	N/A[e]	Yes
Simulations/Measurement	Yes/No	Yes/No	Yes/No	Yes/No	Yes/No	Yes/No	Yes/Yes

Note: [a]Number of elements of one bilinear section which provides usable bandwidth less than one decade, [b]All transistor-based topology, [c]The paper contains the solution based on other active elements as well. [d]Number of active/passive parts in case of the presented 4th-order FLF topology, [e]The feature not available or available but not investigated/presented

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where the approximation is valid. It is 2 decades for [10], < 3 decades for [15] and it is 4 decades for [12] considering usage of 7 sections so the resulting number of active and passive elements is 21/7. The design proposed in this paper offers valid bandwidth of < 2 decades for 5/2 parts or < 3 decades for 9/5 parts as discussed further. The proposed solution as the only one is also supported by experimental measurements.

II. Fractional–Order Integrator Design

The proposed current–mode (having current input and current output) fractional–order integrator is based on the 2nd–order Follow–the-Leader-Feedback (FLF) topology with a FO approximation applied onto it so it behaves as a FO integrator (or differentiator if suitably calculated). The integrator was briefly introduced in [16] for the purpose of a demonstration of an electronically controllable FO of therein proposed structure, nonetheless, the integrator was not investigated closer. The topology itself is based on Operational Transconductance Amplifiers (OTAs), Adjustable Current Amplifiers (ACAs) and an auxiliary Current Follower (CF). Schematic symbols of the OTA, ACA and CF are presented in Fig. 1 a), b), c), respectively. The OTA element can be described by the relation $I_{OUT\pm} = \pm g_m(V_{IN+} - V_{IN-})$, where g_m stands for the transconductance of this element. The behavior of the ACA can be expressed as $I_{OUT\pm} = \pm B(I_{IN})$, where B represents the current gain. The CF is described by $I_{OUT\pm} = \pm I_{IN}$. All mentioned active elements were simulated by the integrated building cells presented in [17]. The chip contains two multiplication units (CMOS and BJT), second–generation current conveyor CCII with four outputs, voltage differencing differential buffer (VDDB) and adjustable current amplifier. The OTA element has been created by the CMOS multiplication unit. Since the multiplication unit has only one output, the CCII (in form of a current follower) has been connected to this output in order to provide copies of the output current. The ACA has been created by the CMOS multiplication unit and one resistor (as shown in Fig. 1 d)) as the current amplifier in the chip has very limited dynamic range. The CCII was used to perform a function of the CF. The experimental measurements are done with a universal current conveyor (UCC) [18] substituting the OTA and CF elements and EL2082 [19] device to implement ACA element.

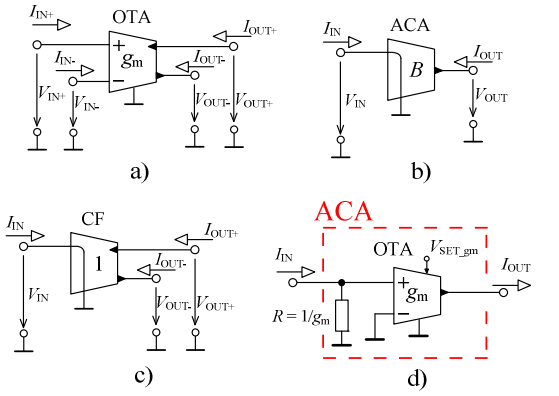

Fig. 1. Schematic symbol of a) OTA, b) ACA, c) CF, d) implementation of ACA by a CMOS multiplication unit and one resistor

The 2nd–order FLF topology used for the approximation of the CM FO integrator is depicted in Fig. 2. It contains two OTAs, one CF, three ACAs (6 active elements in total) and two grounded capacitors. The number of active elements can be decreased to five as current gain B_2 is always equal to 1 (given by approximation) with a proper polarity of this branch in mind. The expected power consumption of the CMOS-based implementation is approximately 145 mW.

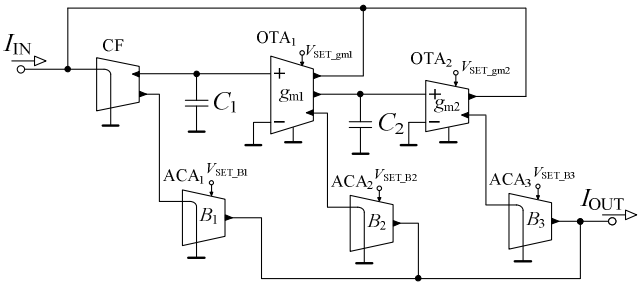

Fig. 2. 2nd–order FLF topology used for the approximation of a CM FO integrator

The transfer function of the structure in Fig. 2 is given by:

$$K(s) = \frac{s^2 C_1 C_2 B_1 + s C_2 g_{m1} B_2 + g_{m1} g_{m2} B_3}{s^2 C_1 C_2 + s C_2 g_{m1} + g_{m1} g_{m2}}. \quad (1)$$

The second–order approximation of s^α is expressed as:

$$s^\alpha \cong \frac{a_0 s^2 + a_1 s + a_2}{a_2 s^2 + a_1 s + a_0}. \quad (2)$$

The values of a_0, a_1, a_2 (when using a second–order approximation provided in [18]) are being given as $a_0 = \alpha^2 + 3\alpha + 2$, $a_1 = 8 - 2\alpha^2$, $a_2 = \alpha^2 - 3\alpha + 2$ (obtained by Continued fraction expansion (CFE) method). Thus, the general transfer function which approximates the 2nd–order FLF topology in order to behave as a FO integrator is given as:

$$K(s) = \frac{(\frac{\alpha^2 - 3\alpha + 2}{\alpha^2 + 3\alpha + 2}) s^2 + \frac{1}{\tau}(\frac{8 - 2\alpha^2}{\alpha^2 + 3\alpha + 2}) s + \frac{1}{\tau^2}}{s^2 + \frac{1}{\tau}(\frac{8 - 2\alpha^2}{\alpha^2 + 3\alpha + 2}) s + \frac{1}{\tau^2}(\frac{\alpha^2 - 3\alpha + 2}{\alpha^2 + 3\alpha + 2})}. \quad (3)$$

The values of each variable in (1), for selected value of α and chosen operational frequency, can be determined when comparing (1) with (3).

III. Simulation and Experimental Results

In order to support the proposed design, simulations in Cadence IC6 (spectre) (using CMOS I3T25 0.35 µm ON Semiconductor technology) and experimental measurements were carried out. The dependency of the transconductance of used multiplication unit on the driving DC voltage is given as $g_m \approx (2 \times V_{SET\_gm})/1000$. Simple V–I/I–V convertors together with network analyzer Agilent 4395A were used for the measurement. The central operational frequency f_C of the bandwidth where the approximation is valid has been chosen to be 50 kHz. The values of capacitors are as follows C_1 = 1 nF and C_2 = 10 nF. The values of transconductances g_{m1} and g_{m2} and current gains B_1, B_2, B_3 are then calculated based on the selected operational frequency and chosen approximation.

The electronic control of FO of the proposed integrator is demonstrated in Fig. 3 for the simulation results represented by black dashed lines and the experimental results denoted by colored lines. The results are provided for α equal to 0.1 to 0.7 with step of 0.1. Specific values of transconductances and current gains in dependence on α are provided in Table II. As it is evident from the table, higher values of α require

values of current gains which are more difficult to obtain (either too low (B_1) or too high (B_3)). Thus, the proposed circuit is more suitable for lower values of α. From the graphs, it can be seen that the approximation of fractional order is valid for approximately two decades. The usable bandwidth is also limited by the frequency limitations (effect of parasitic characteristics) of used active elements as observable at frequencies above 3 MHz. The experimental values (in case of the magnitude) are slightly (about 3 dB) higher than the simulation results, nonetheless, both results support the intended function and design correctness.

TABLE II. VALUES OF INDIVIDUAL PARAMETERS OF THE INTEGRATOR IN DEPENDENCE ON VALUES OF ALPHA

α [-]	0.1	0.2	0.3	0.4	0.5	0.6	0.7
g_{m1} [µS]	1090	942	822	718	628	550	480
g_{m2} [µS]	673	571	478	393	314	242	175
B1 [-]	0.74	0.545	0.398	0.286	0.2	0.135	0.085
B2 [-]	1						
B3 [-]	1.35	1.833	2.51	3.5	5	7.43	11.77

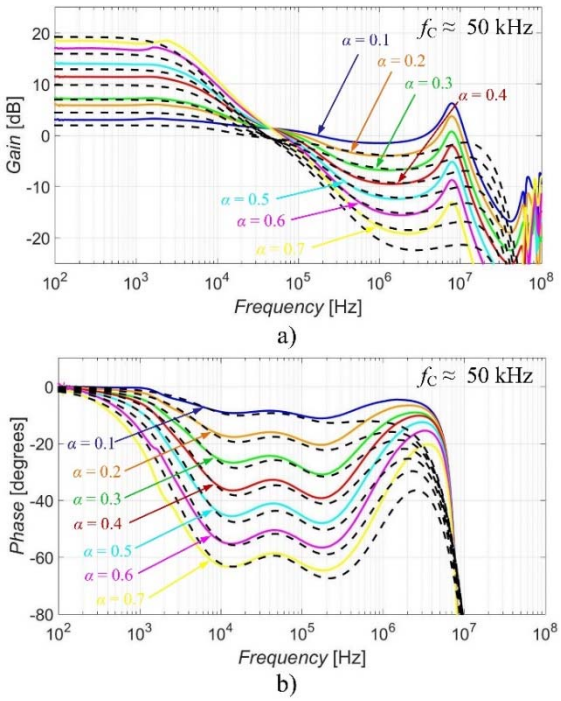

Fig. 3. Electronic control of the order of proposed FO integrator (experimental measurment (colored lines), simulations (black dashed lines)): a) magnitude characteristics, b) phase characteristics

The other beneficial electronic control is the control of the frequency of the operational bandwidth where the approximation is valid. The control id achieved through the change of transconductances (g_{m1} and g_{m2}) as long as the ratio between them stays unchanged. That way we can shift the bandwidth to desired frequencies. Fig. 4 demonstrates the frequency shift of the operational bandwidth for three different settings of transconductances (provided in the Table III) where the theoretical (center) frequency f_C is approximately equal to 25 kHz, 50 kHz and 100 kHz. The demonstration is done for α = 0.5, thus the setting of current gains is the same as for α = 0.5 in Table II for all three cases in Fig. 4. Lower upper DC gain of the 25kHz characteristic is most likely caused by limited linear behavior based on the values of transconductances.

TABLE III. VALUES OF TRANSCONDUCTANCES (FOR ALPHA = 0.5) IN DEPENDENCE ON THE CONTROL OF THE FREQUENCY BAND

Theoretical frequency f_C	25 kHz	50 kHz	100 kHz
g_{m1} [µS]	314	628	1256
g_{m2} [µS]	157	314	628

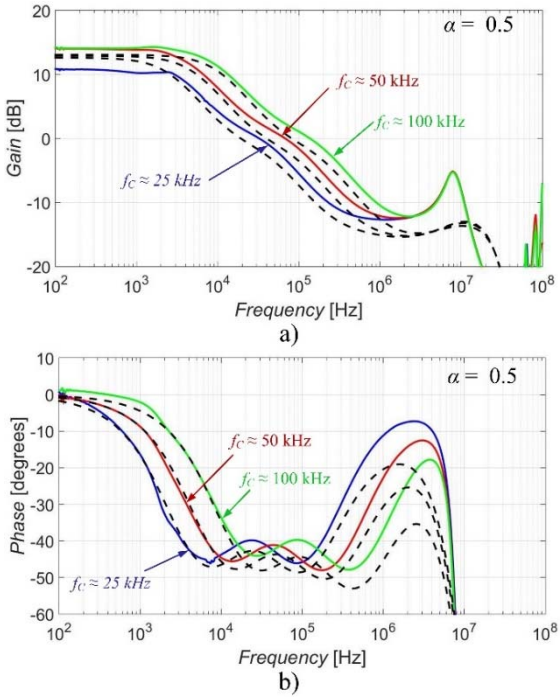

Fig. 4. Electronic control of the frequency band of proposed FO integrator (experimental measurment (colored lines), simulations (black dashed lines)): a) magnitude characteristics, b) phase characteristics

In order to provide wider operational bandwidth, the analogous 4th–order FLF topology (Fig. 5) has been designed. It consists of one CF, four OTAs, five ACAs and four grounded capacitors. Since the value of current gain B_3 is always 1, the ACA_3 can be omitted decreasing the number of active elements by one (9 in total). The 4th–order approximation provided in [15] has been used. When choosing the operational frequency being approximately equal to 50 kHz and α = 0.5, C_1 = 100 pF, $C_2 = C_3$ = 1 nF, C_4 = 10 nF, the values of remaining parameters were calculated accordingly: g_{m1} = 293 µS, g_{m2} = 471 µS, g_{m3} = 898 µS, g_{m4} = 87 µS, B_1 = 0.11 B_2 = 0.43 B_3 = 1, B_4 = 2.33 B_5 = 9. The values of transconductances and current gains were obtained in similar manner as in case of the topology from Fig. 2 by comparison of the transfer function of the proposed structure and the relation of the 4th–order FO approximation. The transfer function of the structure in Fig. 5 is given as $K(\boldsymbol{s}) = N(\boldsymbol{s})/D(\boldsymbol{s})$, where:

$$N(\boldsymbol{s}) = \boldsymbol{s}^4 C_1 C_2 C_3 C_4 B_1 + \boldsymbol{s}^3 C_2 C_3 C_4 g_{m1} B_2 + \\ + \boldsymbol{s}^2 C_3 C_4 g_{m1} g_{m2} B_3 + \boldsymbol{s} C_4 g_{m1} g_{m2} g_{m3} B_4 + \\ g_{m1} g_{m2} g_{m3} g_{m4} B_5 \quad , \qquad (4)$$

$$D(\boldsymbol{s}) = \boldsymbol{s}^4 C_1 C_2 C_3 C_4 + \boldsymbol{s}^3 C_2 C_3 C_4 g_{m1} + \\ + \boldsymbol{s}^2 C_3 C_4 g_{m1} g_{m2} + \boldsymbol{s} C_4 g_{m1} g_{m2} g_{m3} + \\ g_{m1} g_{m2} g_{m3} g_{m4} \quad (5)$$

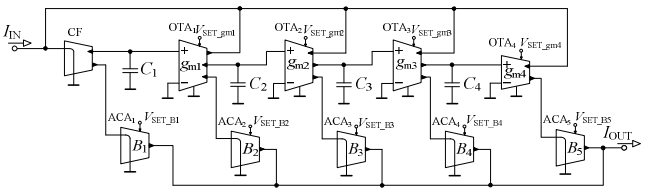

Fig. 5. 4th–order FLF topology used for the approximation of a CM FO integrator

The comparison of the simulation results (colored lines) and theoretical expectations (black dashed lines) of the integrator from Fig. 2 (blue lines) and the integrator from Fig. 5 (red lines) is presented in Fig. 6. It can be seen that the integrator from Fig. 5 can provide wider bandwidth where the approximation is valid (about three decades) in comparison to the integrator from Fig. 2 (about two decades). It can provide wider bandwidth with the same amount of active elements (10(9) in this case) in comparison to solutions in Table I. It can be seen that the usable bandwidth is depending on the order of the used approximation. Considering 5° phase error for the case when α = 0.5, the bandwidth is given as approximately $f_c/10$ and $f_c \cdot 10$ for order of used approximation n = 2 and $f_c/25$ and $f_c \cdot 10$ for n = 4.

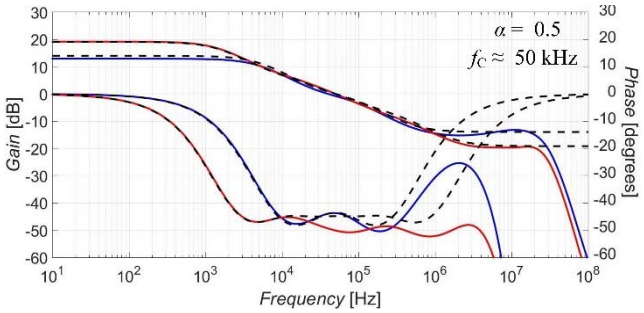

Fig. 6. Comparison of the simulation (colored lines) and theoretical (black dashed lines) results of the integrator from Fig. 2 (blue lines) and the integrator from Fig. 5 (red lines)

IV. Conclusion

Cadence IC6 (spectre) simulations and experimental measurements were carried out to support the design. The electronic controls of the FO and frequency band were proven to function as intended (see Figs. 3 and 4). The design requires five active elements and two passive elements in case of the 2nd–order topology (with usable bandwidth of about 2 decades) and nine active and four passive elements in case of the 4th–order topology (with usable bandwidth of about 3 decades) which is less active elements needed in comparison to other proposed integrators while providing same bandwidth range. The proposed integrator can also function as a FO differentiator when calculated accordingly.

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