CIRCUITS FOR ANALOG SIGNAL PROCESSING
EMPLOYING UNCONVENTIONAL ACTIVE ELEMENTS

SHORT VERSION OF PH.D. THESIS
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Klíčová slova
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INTRODUCTION

Although in most modern electronic systems, signal processing and storage are performed in digital domain, but ASP (Analog Signal Processing) is still required since the real-world signal is represented in the analog form. As a result, most electronic equipments comprise analog processing circuitry that acts as interface between the digital-world and the real-world. However, analog signal is processed for variety of purposes, such as to remove unwanted noise, to correct distortion, to make the signal suitable for transmission or to extract certain meaningful information. The term ASP expresses plentiful of techniques that can be implemented to process analog signals including the theory and application of filtering, coding, transmitting, estimating, detecting, analyzing and reproducing analog signals.

Many years ago, analog blocks, so-called active elements, have been appeared. These active blocks replaced the passive ones. Through active elements numerous of applications can be designed to process analog signal such as filters, oscillators, rectifiers and so forth. However, the term CM (Current Mode), VM (Voltage Mode) and MM (Mixed Mode) is inherent to active element term.

However, the aim of this thesis is to find new active elements or even improve the existing ones and applying those to new applications such as filters and oscillators. Factually, the main focus of this thesis is on LV LP (Low voltage Low Power) field for implementing analog circuits because this field has become essential in IC design in order to ensure reliable functioning of devices, to prevent overheating caused by increasing density of components per unit area and to prolong the battery lifetime in case of portable electronic equipment and implantable medical devices.

It is worth mentioning here that all circuits exhibited in this thesis are novel and their advantages are compared with the literature presented solutions. Moreover, most of them are already published in international journals with high impact factor and were cited by numerous researchers.

1. STATE OF THE ART

The field of LV LP CMOS technology has grown rapidly in recent years; it is an essential prerequisite particularly for portable electronic equipment and implantable medical devices due to its influence on battery lifetime. Recently, significant improvements in implementing circuits working in the LV LP area have been achieved, but circuit designers face severe challenges when trying to improve or even maintain the circuit performance with reduced supply voltage.

In order to achieve an excellent performance of analog circuits, the input and output voltage swing capability should be extended, preferably to obtain rail-to-rail input and output operation capability. However, to achieve this, the threshold voltage of MOST needs to be reduced. Indeed, the threshold voltage does not scale down with reducing supply voltage of standard CMOS technologies; hence analog designers face many difficulties and challenges due to the limited voltage headroom.

Several MOST (MOSFET Transistor) design techniques exist for LV LP analog circuit design. However, only a few of them have found their way in modern designs, for instance, MOSTs operating in the sub-threshold (weak inversion) region, level shifter techniques, self-cascode structures, BD (Bulk Driven) technique, FG (Floating Gate) approach and QFG (Quasi Floating Gate)
It is essential to point out that the lower transconductance value of BD, FG and QFG leads not only to lower bandwidth but also to higher input referred noise in comparison to GD MOST. Another issue is that the FG and QFG MOSTs can't process DC signals, since their input terminals are capacitively connected to the FG and QFG, respectively. Also, due to the input capacitors the silicon area requirements of FG and QFG MOSTs are increased.

From the upper mentioned drawbacks, the idea of new two techniques has appeared in order to combine the advantages and eliminate the disadvantages of the BD, FG and QFG techniques. These interesting techniques are named BD-FG and BD-QFG and they are created by combining the BD with either the FG or QFG techniques. However, in this work the BD-QFG technique is used, since the BD-FG MOST suffers from undesirable drawbacks related to the FG-MOST such as: large occupied area on the chip, initial charge trapped on the FG and lack of simulation models.

In view of limitation of op-amp with capacitive load and inherent on-chip tunability, the OTA operational transconductance amplifier is extensively preferred in many applications. Hereafter, active elements were appeared to replace the op-amp element

2. **THEESIS OBJECTIVES AND RESULTS**

In the last decade, massive number of active elements were designed and introduced in area of ASP. However, designers still aim to develop new active elements or even improve the characteristics of the old ones to achieve better features than theirs counterparts. These better features can be described as higher-frequency performance/ inherent signal bandwidths, greater linearity, wider dynamic range, lower supply voltages, lower power consumption and simplicity in designing. Therefore, the main objective of this thesis is to implement and improve various types of active elements.

In this chapter many concepts and techniques are utilized for implementing new design of active elements. For example, many LV LP techniques are used, circuits working in CM are used as well, etc. hence achieving the previously mentioned aims.

Since conventional GD technique is still used, as well VM is still utilized in many ASP area then this thesis will cover them as well to become more versatile in terms of being containing a different number of principles/applications.

However, to validate the functionality of active elements thus they are further utilized in this thesis for various interesting applications, i.e. filter and oscillator designs.

2.1 **NEW DESIGN OF ACTIVE ELEMENTS AND THEIR PROPERTIES**

This sub-chapter presents new promising designs of well-known active elements, where most of them have been designed by utilizing LV LP techniques. The simulation results of these new structures appear to be superior compared to their counterparts based on the conventional GD technique or even on LV LP ones. The chapter mainly presents and illustrates an elegant approach to designing a CCII of good performance; the CCII was chosen as main active element in this thesis because it is considered as fundamental and versatile active one that can be used in massive number of applications, moreover, the CCII is the basic block of many other active elements.

Furthermore, defining new active element i.e. DBeTA based on BD is also one of the main contributions of this thesis. However, other active elements are exhibited as well.
2.1.1 LV LP BD-CCII± Based on Folded Cascode OTA

The novel LV LP CCII± based on folded cascode BD-OTA is shown in Fig. 2.1.

![Diagram](image)

**Fig. 2.1.** CMOS implementation of the novel LV LP CCII± based on folded cascode BD-OTA [1].

The simulation result of the proposed LV LP CCII± based on folded cascode BD-OTA is shown in Fig 2.2.

![Graph](image)

**Fig. 2.2.** DC curves $I_Z^+$ and $I_Z^-$ versus $I_X$.

Based on the simulation results the novel high-precision LV LP BD-CCII± has the following advantages:

1. LV supply requirements around ±400 mV.
2. LP dissipation around 64 µW.
3. Nearly rail-to-rail operating range and voltage swing for the Y terminal around ±380 mV, which could not otherwise be achieved at lower supply voltages with a tracking error of less than 0.13 %.
4. High precision tracking of $I_X$ vs. $I_{Z+}$ and $I_Z$ with an acceptable range of ±7 μA and with a tracking error of less than 0.013 %.
5. The conventional MOS transistor is used to model the BD-MOS transistor.
6. The bulk terminals of only NMOS transistors are used here as a signal path, and thus there is no need to use expensive twin-tub technology.
7. Acceptable gain bandwidth product (GBW) close to 13 MHz.
8. Acceptable low $X$-node parasitic DC resistance around 27 Ω.
9. Design simplicity.
10. Reduced voltage supply and proper circuit design prevent latch-up problems.

It is worth mentioning here that our CMOS structure presented in this sub-chapter is already published in Microelectronic Journal [1] with Impact Factor IF: 0.919.

### 2.1.2 Ultra-LP FG-CCII+ Based on Folded Cascode OTA

The novel LV LP class AB CCII+ based on folded cascode FG-OTA is shown in Fig. 2.3.

![Fig. 2.3. CMOS implementation of the novel LV LP class AB CCII+ based on FG folded cascode OTA [2].](image)

Fig. 2.4 shows DC curve $I_{Z+}$ versus $I_X$ and current error $I_{Z+} - I_X$, simulated on condition that $Y$ terminal is grounded. Note that for input current $I_X$, the boundary of linear operation is in the range of –30 to +30 μA. This DC range of linear operation is suitable for many applications that need extra low power consumption. The current error $I_{Z+} - I_X$ is in range of 116 pA to –30 nA, and for $I_X = 0$ A the $I_{Z+} = 5$ pA.
Based on the simulation results the novel high-precision LV LP FG–CCII+ has the following advantages:

1. LV supply requirements around ±500 mV.
2. Ultra-LP dissipation around 10 µW.
3. Threshold voltage requirement is removed from the signal path.
4. Rail-to-rail voltage swing for the Y terminal [-500 to +500] mV, which could not otherwise be achieved at lower supply voltages.
5. High precision tracking of \( I_X \) vs. \( I_Z \), thanks to the cascode mirrors structure.
6. High precision tracking of \( V_X \) vs. \( V_Y \) thanks to the unity gain OTA.
7. High Z node parasitic DC resistance around 53 MΩ.
8. Acceptable gain bandwidth product (GBW) close to 8.2 MHz.
9. Acceptable low X node parasitic DC resistance around 42 Ω.
10. A conventional MOS transistor is used to model the FG MOS transistor.
11. Design simplicity.

It is worth mentioning here that our CMOS structure presented in this sub-chapter is already published in Circuits Systems and Signal Processing journal [2] with Impact Factor IF: 0.817.

### 2.1.3 LV Ultra-LP QFG–CCII Based On Folded Cascode OTA

The LV LP class AB CCII based on folded cascode OTA is shown in Fig. 2.5.

Fig. 2.6 shows the \( I_Z \) curve vs. \( I_X \) and the current error of the LV LP CCII, simulated on the condition that the Y terminal is grounded. Note that for input current \( I_X \), the boundary of linear operation is in the range of [-100 to +100] µA. For a current range of [-75 to +75] µA the current error is only in the range from [2.45 to -2] nA. However, this DC range of linear operation is suitable for many applications that need extra low power consumption and high precision.
Fig. 2.5. CMOS implementation of the LV LP class AB CCII based on QFG transistors [3].

Fig. 2.6. DC curve $I_Z$ versus $I_X$ and the current error.

It is worth mentioning here that our CMOS structure presented in this sub‐chapter is already published in Radioengineering Journal [3] with Impact Factor IF: 0.739.

2.1.4 **LV Ultra LP FG-DVCC Based on Folded Cascode OTA**

The novel LV ultra LP DVCC based on folded cascode FG-OTA is shown in Fig. 2.7.
Fig. 2.7. CMOS implementation of the novel LV LP DVCC based on floating-gate folded cascode OTA [4].

The simulation results of the proposed FG-DVCC are shown in Fig. 2.8.

![Graph showing frequency dependence of parasitic impedance of X terminal.]

**Fig. 2.8.** Frequency dependence of parasitic impedance of X terminal.

Based on the simulation results the novel LV ultra LP FG-DVCC has the following advantages:

1. LV supply requirements ±500 mV.
2. Ultra-LP dissipation 10 µW.
3. Threshold voltage requirement removed from the signal path.
4. Rail-to-rail voltage swing capability for the Y₁, Y₂ terminals which could not otherwise be achieved at lower supply voltages.
5. The conventional MOST is used to model the FG-MOS transistor.
6. Acceptable current gain bandwidth product (GBW) close to 10.2 MHz.
7. Acceptable X-node parasitic DC resistance around 70 Ω.
8. Very high Z parasitic resistance 55.7 MΩ.
9. Design simplicity.

It is worth mentioning here that our CMOS structure presented in this sub-chapter is already published in Microelectronic Journal [4] with Impact Factor IF: 0.919.

2.1.5 LV LP High-Precision BD-DBeTA

The internal structure of the BD-DBeTA is built from BD folded cascode OTAs as shown in Fig. 2.9.

![BD-DBeTA Diagram](image)

**Fig. 2.9.** Internal structure of BD-DBeTA built from BD folded cascode OTAs.

The LV LP BD folded cascode OTA is shown in Fig. 2.10. The DC biasing of the topology is provided by transistors \(M_{b1} - M_{b3}\) and current bias \(I_{bias}\). The \(I_{bias}\) could be realized either by LV LP current source circuitry or simply could be replaced by a resistor.

![CMOS Implementation Diagram](image)

**Fig. 2.10.** CMOS implementation of the LV LP BD folded cascode OTA [5].
Fig. 2.11 shows the $I_z$ versus $I_p$ or $I_n$ curves and current errors $I_z-I_p$, $I_z+I_n$ of the LV LP BD-DBeTA, simulated on condition that the $y_p$ and $y_n$ terminals are grounded. Note that for $I_p$ and $I_n$ in the range from -30 to 30 µA the current error is fairly below ±1.6 nA. However, this range of linear operation is suitable for many applications that need extra low power consumption and high precision performance.

Based on the design and simulation results the high-precision LV LP BD-DBeTA has the following advantages:

1. LV supply of ± 400 mV.
2. LP dissipation of a mere 62 µW.
3. Rail-to-rail operating range capability, which could not otherwise be achieved at lower supply voltages.
5. The conventional MOS transistor is used to model the BD-MOS transistor.
6. The bulk-terminate of only NMOS transistors are used here as a signal path, therefore there is no need to use the expensive twin-tub technology.
7. Acceptable current and voltage gain bandwidth products (GBW) around 10 MHz.
8. Acceptable low X node parasitic DC resistance around 14 Ω.
9. Design simplicity.
10. Reduced voltage supply and proper circuit design prevent latch-up problems.

It is worth mentioning here that our CMOS structure presented in this sub-chapter is already published in Circuits Systems and Signal Processing Journal [5] with Impact Factor IF: 0.982.

2.1.6 Ultra-LV BD-QFG Transconductor

The internal CMOS structure of the BD-QFG transconductor is shown in Fig. 2.12.
Fig. 2.12. CMOS structure of the transconductor based on new BD-QFG technique [6].

To demonstrate the wide linear range and the tunability of the BD-QFG transconductance value of the transconductor, the DC output current versus input voltage with stepping $R_{set}$ from $[80$ to $320]$ kΩ with 40 kΩ step is shown in Fig. 2.13. It is evident the wide range of operation.

Fig. 2.13. DC output current versus input voltage with stepping $R_{set}$ from $[80$ to $320]$ kΩ with 40 kΩ step.

Finally, based on the upper mentioned discussion yields that using the BD-QFG MOST offers mainly the following advantages:

1. High transconductance value closed to the GD one, resulting in increase of the bandwidth and reducing the input referred noise of the proposed circuit.
2. Ultra-LV LP operation capability,
3. Simple circuitry and
4. Extended input voltage range nearly rail-to-rail.

It is worth mentioning here that the presented technique of the proposed CMOS shown in this sub-chapter was registered as a national utility model application by Industrial Property Office in the Czech Republic. In addition, it was also registered as a patent [7] and [8]. Moreover, it was also published in Circuits Systems and Computers Journal IF: 0. 238 [6].
2.1.7 High-Precision GD-CCCDBA

The proposed MOS structure of the CCCDBA is presented in Fig. 2.14.

The frequency responses of current gains $I_z/I_p$ and $I_z/I_n$ for $I_B = 10 \mu A$ are shown in Fig. 2.15. Both current gain magnitudes $I_z/I_p$ and $I_z/I_n$ are unity up to high frequencies and their $-3\text{dB}$ bandwidths are 110 MHz and 155 MHz, respectively.

It is worth mentioning here that our CMOS structure presented in this sub-chapter is already published in Analog Integrated Circuits and Signal Processing Journal [9], with Impact Factor IF: 0.553.

2.1.8 High-Precision GD-VDBA

The characteristics of the proposed circuit have been verified using PSpice simulations, the CMOS-based VDBA is simulated using the schematic implementation shown in Fig. 2.16.
To show the simulation results of VDBA, simulated plots are illustrated in this section. The frequency responses of Z terminal impedances with varying the bias current for values $I_B = [0.001, 0.01, 0.1, 1, 10, 100] \mu A$ are shown in Fig. 2.24. The values of these impedances at low frequency $R_Z$ have the values of $[640 M, 85.19 M, 11.6 M, 2.24 M, 0.833 M, 0.6 M] \Omega$, respectively. It is evident that with varying $I_B$, the Z terminal still possesses a high impedance values.

Fig. 2.17 demonstrates that the output W terminal possesses extremely low value impedances which is nearly zero at low frequencies i.e. 0.016 $\Omega$.

It is worth mentioning here that our CMOS structure presented in this sub-chapter is already published in IEEE Conference [10].
2.1.9 Sub-Conclusion

The limitations of Op-Amp led to the development of active elements. First active element is so-called OTA which is a voltage to current convertor. Inherent capability of OTA with its output current getting controlled by the external bias current, makes it very productive in many application designs.

However, in this chapter new design of well-known active elements are presented, where most of them have been designed by utilizing LV LP techniques. CMOS internal structure with simulation plots are proposed to verify the behavior of the presented active elements.

2.2 FILTERS AND OSCILLATORS APPLICATIONS

All of these applications circuits are new and presented in Intentional Journals with high impact factor. The SPICE simulations confirm the feasibility of all proposed circuits and results are in good agreement with theory.

2.2.1 Current Mode Multifunction Filter Based on BD-CCII±

As an application example of our novel BD-CCII± with extremely LV and LP, we have chosen a frequency filter, because these circuits are widely used in many signal processing systems. The filter is suitable for LV LP systems that do not require a high frequency range, e.g. biological signal processing.

The structure is shown in Fig. 2.18 and it is a current mode second order multifunction filter with single input and multiple outputs.

![Diagram of Current Mode Multifunction Filter](image)

Fig. 2.18. Second order current mode multifunction filter [1].
The results of simulations in PSpice in Fig. 2.19 are in agreement with these values.

It is worth mentioning here that our filter application presented in this subchapter is already published in Microelectronic Journal [1] with Impact Factor IF: 0.919.

### 2.2.2 Current Mode Quadrature Oscillator Based on FG-CCII+

As an application example of the introduced LV LP FG-CCII+ we have designed a current mode quadrature oscillator with dual output FG-CCII+ as shown in Fig. 2.20.

![Quadrature oscillator based on LV LP FG-CCII+](image)

**Fig. 2.20.** Quadrature oscillator based on LV LP FG-CCII+ [2].

The waveforms of the output currents are shown in Fig. 2.21.
It is worth mentioning here that our oscillator application presented in this sub-chapter is already published in Circuits Systems and Signal Processing Journal [2] with Impact Factor IF: 0.817.

### 2.2.3 Current Mode Quadrature Oscillator Based on QFG-CCII±

As an application example of the proposed LV LP QFG-CCII we have designed a current mode quadrature oscillator as shown in Fig. 2.22.

![Quadrature oscillator with LV LP class AB CCII](image)

**Fig. 2.22.** Quadrature oscillator with LV LP class AB CCII [3].

The growing oscillations is shown in Fig. 2.23.
Fig. 2.23. Growing oscillations of the quadrature oscillator output currents.

The simulated oscillation frequency is in agreement with the theoretical value. The THD is 0.20 % for \( I_{O1} \) and 0.43 % for \( I_{O2} \). The total power consumption of the proposed oscillator is only 33 \( \mu \text{W} \).

It is worth mentioning here that our oscillator application presented in this sub-chapter is already published in Radioengineering Journal [3] with Impact Factor IF: 0.739.

2.2.4 Voltage Mode Multifunction Filter Based on FG-DVCC

To show the features of the proposed FG-DVCC, a multifunction filter shown in Fig. 2.24 has been designed. The circuit topology bases on the idea of Akerberg-Mosseberg structure, e.g. the internal loops with integrators are always realized by two active elements, which provide better phase compensation of the filter when high frequency effects of the active elements are considered.
Fig. 2.24. Multifunction voltage mode filter using DVCCs [4].

Fig. 2.25. LP and HP voltage responses for $Q = 1$, $f_0 = [0.3, 1, 3]$ kHz.

The simulation results of the LP and HP responses are shown in Fig. 2.25. The values were chosen as: $C_1 = C_2 = 10$ nF, $R_1 = R_4 = 11$ kΩ to set the value of $Q = 1$. For chosen values of natural frequency $f_0 = [0.3, 1, 3]$ kHz the values of the resistors $R_2$ and $R_3$ have to be $R_2 = R_3 = [53.6, 16.2, 5.36]$ kΩ.

It is worth mentioning here that our filter application presented in this subchapter is already published in Microelectronic Journal [4] with Impact Factor IF: 0.919.
2.2.5 Voltage Mode Oscillator Based on BD-DBeTA

As an application example of the proposed BD-DBeTA element we have designed an oscillator with voltage output shown in Fig. 2.26. It employs one active element, two resistors and two capacitors. Three passive elements are grounded, which is advantageous for integrated implementation. Note that the p terminal is intentionally left unconnected and no current flows into it. The yp terminal is grounded in this case.

![Diagram of BD-DBeTA oscillator](image)

**Fig. 2.26.** The proposed oscillator based on BD-DBeTA [5].

The waveforms of the oscillator output voltage are shown in Fig. 2.27.

![Oscillator waveforms](image)

**Fig. 2.27.** Growing oscillations of the oscillator output voltage.

It is worth mentioning here that our oscillator application presented in this subchapter is already published in Circuits Systems and Signal Processing Journal [5] with Impact Factor IF: 0.982.
2.2.6 Voltage Mode Multifunction $G_m$-$C$ Filter Based on BD-QFG Transconductor

Fig. 2.28 shows a second order $G_m$-$C$ multifunction filter based on two BD-QFG transconductors and two capacitors to realize the LP, HP and BP responses.

![Diagram of a second order $G_m$-$C$ multifunction filter](Image)

**Fig. 2.28.** Second order $G_m$-$C$ multifunction filter based on two BD-QFG transconductors and two capacitors [6].

Fig. 2.29 shows the frequency and phase responses of the second order $G_m$-$C$ filter presented in Fig. 2.28. By setting $C_1=C_2=20 \ \text{pF}$ and $R_{\text{set1}}=R_{\text{set2}}=265 \ \text{k}\Omega$, which yield $f_0=30 \ \text{kHz}$ and $Q=1$. It is evident that the simulation results are in agreement with theory. The total power consumption of the filter is $37 \ \mu\text{W}$.

![Frequency and phase responses](Image)

**Fig. 2.29.** The frequency and phase responses of the second order $G_m$-$C$ multifunction filter.

It is worth mentioning here that our filter application presented in this sub-chapter is already published in Circuits Systems and Computers Journal [6] with Impact Factor IF: 0.238.
2.2.7 Electronically Tunable Voltage Mode Quadrature Oscillator Based on GD-CCCDBA

As an application of the proposed CCCDBA we introduced the quadrature oscillator shown in Fig. 2.30.

![Quadrature oscillator based on CCCDBA](image)

**Fig. 2.30.** Quadrature oscillator based on CCCDBA [9].

The simulation results of the proposed quadrature oscillator are shown in Figs. 2.47 to 2.48. The capacitances were chosen \( C_1 = C_2 = 100 \, \text{pF} \), bias currents \( I_{B1} = I_{B2} = 5 \, \mu\text{A} \), and \( R = 3.8 \, \text{k}\Omega \) to set the circuit slightly behind the stability limit.

The growing oscillations of the quadrature oscillator output voltages are shown in Fig. 2.31.

![Growing oscillations of the quadrature oscillator output voltages](image)

**Fig. 2.31.** Growing oscillations of the quadrature oscillator output voltages.

It is worth mentioning here that our oscillator application presented in this sub-chapter is already published in Analog Integrated Circuits and Signal Processing Journal [9] with Impact Factor IF: 0.553.
2.2.8 Voltage Mode Multifunction Filter Based On GD-VDBA

To assure the validity and practical usefulness of the proposed VDBA, this section will discuss new interesting filter application. The universal filter is shown in Fig. 2.32.

![Filter Diagram](image)

**Fig. 2.32.** VM Filter application [10].

The simulation results of the filter with \( C_1 = C_2 = 1 \) nF and \( I_{B1} = I_{B2} = I_{B3} = 120 \) µA are shown in Fig. 2.33, where three types of transfer functions are available, namely LP, BP and HP. Simulated natural frequency value is 46.9 kHz. It can be clearly said that both simulated and theoretical results are close agreement with each other.

![Frequency Response](image)

**Fig. 2.33.** Frequency response of the proposed universal filter.

It is worth mentioning here that our filter application presented in this sub-chapter is already published in IEEE conference [10].

2.2.9 Sub-Conclusion

This chapter was devoted to the realization of new interesting applications working on CM or VM.
3 CONCLUSION

Since the emergence of electronics, the active elements have been always appeared as fundamental parts in analog integrated circuits. Recently, researchers continuously seek to implement new principles of active elements to improve the functionality of the old ones. However, to achieve the universality of active elements, both the current and the voltage types of output signals should be available. Thus, an easy implementation of filters and oscillators operating in mixed voltage–current modes is obtained. Therefore, the main objective of this thesis was to implement and improve various types of active elements [11].

While a LV (Low Voltage) feature becomes an essential demand particularly in the case of portable devices, the CM (Current Mode) technique is ideally suited for this purpose, more than VM (Voltage Mode). CM has shown its superiority over VM, especially in larger dynamic range, higher signal bandwidth, greater linearity, simpler circuitry, higher speed, higher accuracy and lower power LP consumption. Hence, the main part of this thesis was focusing on LV LP-CM circuits [12].

However, to validate the functionality of the presented CMOS circuits, thus, many interesting applications i.e. filters and oscillators were illustrated.

Based on the presented internal CMOS structure of active elements and the relevant applications, it can be declared that aims of this thesis were fulfilled.

It is noteworthy that almost all parts of this thesis were already published in many international journals with high impact factor. In addition, one of the presented techniques in this thesis was registered as a patent. Furthermore, these published articles have received many citations. Please refer to my Curriculum Vitae for further information.
4 REFERENCES


CURRICULUM VITAE

Nabhan Khatib

Current Address: Czech Republic, Brno.
Mobile phone: +420 775 604 282
E-mail: xkhati02@stud.feec.vutbr.cz

Academic Education:


Computer knowledge:

- Cisco Certified Network Associate.
- Cisco Certified Network Associate Security.
- Cisco Certified Network Professional.
- Linux.
- C++.
- HTML and PHP.
- PSPICE Program.
- MATLAB & Simulink.
- Windows XP/7, Microsoft Office, Internet.

Languages:

- Arabic: Mother tongue.
- English: Very good.
- Czech: Very good.
- French: Elementary knowledge.

Research:

- Patent: Connection of FG MOS and QFG MOS transistors for analog integrated circuits.
- Ph.D. project: Circuits for analog signal processing employing unconventional active elements.
- Master project: Designing software for database of audio records.
- Bachelor project: Usage of digital filter banks for noise removing.
Ph.D. Information:

- H-index according to Web of Science: 3
- Number of published papers in journals with Impact Factor IF: 7
- Number of papers under review in journals with IF and not included in this thesis: 5
- Invited reviewer for the following scientific Journals:
  - International Journal of Electronics.
  - Microelectronics Journal.
- Citations:


**What:** KHATEB, F.; KHATIB, N.; KUBÁNEK, D. Novel Low-Voltage Low-Power High-Precision CCII Based on Bulk- Driven Folded Cascode OTA. Microelectronic Journal, 2011, Year. 2011 (42), n. 5, p. 622-631. ISSN: 0026-2692. IF:0. 919.


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**Where:** Suadet, V. Kasemsuwan, A CMOS inverter-based class-AB pseudo-differential amplifier with current-mode common-mode feedback (CMFB), Analog Integr Circ Sig Process, 2013 p. 387-398.

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**Practical experiences:**

- **Electronics:**

- Teaching practical labs of “Electronic devices”, “Analog electronic circuits” and “Modeling and computer simulation” subjects at Microelectronic Department, Faculty of Electrical Engineering and Communication, Brno University of Technology, Czech Republic.
ABSTRACT

The dissertation thesis deals with implementing new structures of modern active elements working in voltage-, current-, and mixed mode. The functionality and behavior of these elements have been verified by SPICE simulation. Sufficient numbers of simulated plots are included in this thesis to illustrate the precise and strong behavior of those elements. However, a big attention to implement active elements by utilizing LV LP (Low Voltage Low Power) techniques is given in this thesis, this attention came from the fact that growing demand of portable electronic equipments and implantable medical devices are pushing the development towards LV LP integrated circuits because of their influence on batteries lifetime.

More specifically, the main contribution of this thesis is to implement new CMOS structures of: CCII (Current Conveyor Second Generation) based on BD (Bulk Driven), FG (Floating Gate) and QFG (Quasi Floating Gate); DVCC (Differential Voltage Current Conveyor) based on FG; Transconductor based on new technique of BD-QFG (Bulk Driven-Quasi Floating Gate); CCCDBA (Current Controlled Current Differencing Buffered Amplifier) based on conventional GD (Gate Driven); VDBA (Voltage Differencing Buffered Amplifier) based on GD.

Moreover, defining new active element i.e. DBeTA (Differential-Input Buffered and External Transconductance Amplifier) based on BD is also one of the main contributions of this thesis.

To confirm the workability and attractive properties of the proposed circuits many applications were exhibited. The given results agree well with the theoretical anticipation.
ABSTRAKT

Disertační práce se zabývá zaváděním nových struktur moderních aktivních prvků pracujících v napěťovém, proudovém a smíšeném režimu. Funkčnost a chování těchto prvků byly ověřeny prostřednictvím SPICE simulací.

V této práci je zahrnuta řada simulací, které dokazují přesnost a dobré vlastnosti těchto prvků, přičemž velký důraz byl kladen na to, aby tyto prvky byly schopny pracovat při nízkém napájecím napětí, jelikož poptávka po přenosných elektronických zařízeních a implantabilních zdravotnických přístrojích stále roste. Tyto přístroje jsou napájeny bateriemi a k tomu, aby byla prodloužena jejich životnost, trend navrhování analogových obvodů směřuje k stále většímu snižování spotřeby a napájecího napětí.

Hlavním přínosem této práce je návrh nových CMOS struktur: CCII (Current Conveyor Second Generation) na základě BD (Bulk Driven), FG (Floating Gate) a QFG (Quasi Floating Gate); DVCC (Differential Voltage Current Conveyor) na základě FG, transkonduktor na základě nové techniky BD-QFG (Bulk Driven-Quasi Floating Gate), CCCDBA (Current Controlled Current Differencing Buffered Amplifier) na základě GD (Gate Driven), VDBA (Voltage Differencing Buffered Amplifier) na základě GD a DBeTA (Differential-Input Buffered and External Transconductance Amplifier) na základě BD.

Dále je uvedeno několik zajímavých aplikací užívajících výše jmenované prvky. Získané výsledky simulací odpovídají teoretickým předpokladům.