

Design of Passive Analog Electronic Circuits using Hybrid Modified UMDA Algorithm

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Abstract. Hybrid evolutionary passive analog circuits synthesis method based on modified Univariate Marginal Distribution Algorithm (UMDA) and a local search algorithm is proposed in the paper. The modification of the UMDA algorithm which allows to specify the maximum number of the nodes and the maximum number of the components of the synthesized circuit is proposed. The proposed hybrid approach efficiently reduces the number of the objective function evaluations. The modified UMDA algorithm is used for synthesis of the topology and the local search algorithm is used for determination of the parameters of the components of the designed circuit. As an example the proposed method is applied to a problem of synthesis of the fractional capacitor circuit.

Keywords

Evolutionary algorithm, optimization, estimation of distribution algorithm, EDA, fractional capacitor

1. Introduction

In many areas of the engineering applications Estimation of Distribution Algorithms (EDA) have proved excellent capabilities of dealing with various kinds of problems of different nature. However, in the area of the evolutionary electronics utilization of the EDA algorithms has not been sufficient. Several papers focused on the evolutionary design of the whole analog circuit (the topology and the parameters of the components) have been published. In [2] Zinchenko published method of synthesis of the passive analog circuits using Univariate Marginal Distribution Algorithm (UMDA) algorithm however the method has two drawbacks. Parallel connection of the components in the branches of the circuits is not possible and with increasing number of the nodes of the designed circuit the number of the components is increasing more than necessary. Another paper focused on the evolutionary synthesis of the passive analog circuits using EDA algorithms was published by Torres [3] however the method employs UMDA algorithm only for determination of the number of the resistors, capacitors and inductors in the designed circuit. Minimal Switching Graph Problem solved using hybrid EDA algorithm method was presented in [4]. The method employs the UMDA to sample start search

points and a hill-climbing algorithm to find local optimum of the search space.

The proposed EDA algorithm solves the drawbacks of the method [2] mentioned above. The maximum number of the nodes and the maximum number of the components of the synthesized circuit can be set independently. Also encoding of the parallel components is possible. Furthermore the proposed method employs efficient hybrid approach which significantly reduces the number of the objective function evaluations. For the same optimization problem the number of the evaluations of the objective function of the proposed method is almost four times lower than for simulated annealing algorithm [12].

2. Hybrid Modified UMDA Algorithm

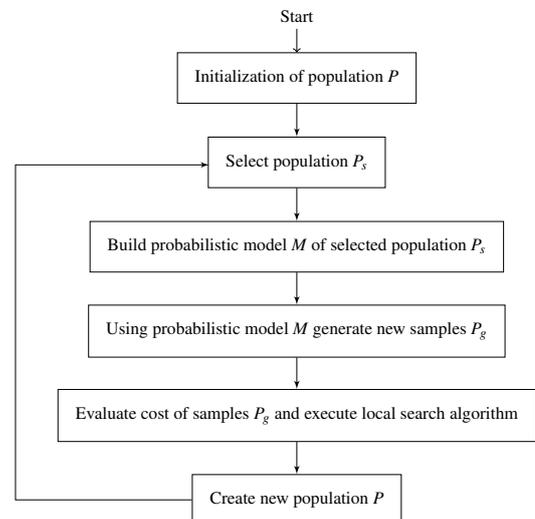


Fig. 1. Principal flowchart of the proposed method [1].

The flowchart of the proposed method is presented in Fig. 1. Population P is formed of binary vectors of length 135 bits which are initialized randomly with seeding of 10 bits ($n_c = 10$). Parameters storage e_{ps} is formed of a vector of length 135 consisting of real numbers in the range $(0,1)$. Parameters storage e_{ps} is dynamically optimized during the whole synthesis process and it is adapted to the selected topologies in the selection phase of the algorithm. The vector includes a component value for every single admittance of the used expanded fully connected ad-

mittance network (see Sec. 6). During initialization phase e_{ps} is set randomly with uniform distribution.

In the next step selected population P_s is formed of the good individuals of the previous population P .

Probabilistic model M of selected population P_s is built. For more information on building of the probabilistic model in UMDA algorithm please refer to [5].

Probabilistic model M built in the previous step is used for generation of new samples of solutions P_g . The new samples are generated using Stochastic Universal Sampling method (SUS) and are repaired using the repairing method described in Sec. 3.

The generated samples are evaluated using the topological information stored in the individuals of P_g and the parameters of the components stored in e_{ps} . If the condition of execution of the local search algorithm is fulfilled, the local search algorithm tries to optimize the parameters of the current solution. If the accuracy of the current solution is improved, then storage of the parameters e_{ps} is updated according to the results of the local search algorithm. Detailed description of the cost evaluation phase and the local search algorithm is presented in Sec. 4.

In the next step new population P is formed of the best individuals of P_g and selected population P_s . The described process is repeated until one of the termination criteria of the algorithm is met.

3. The Unitation Constraints

Generally desired specifications of an analog circuit are easier to reach using an analog circuit of higher complexity. Due to the fact the evolutionary analog circuits synthesis methods tend to evolve analog circuits with complexity as large as possible. Without restriction of the number of the components of the evolved circuit its complexity becomes higher than necessary.

Therefore the number of the components of the evolved circuit should be restricted to a user define value. Since in the proposed encoding method (section 6) the number of the components of the encoded circuit is determined by the number of the "ones" of the binary characteristic vector c the restriction of the number of the components leads to a problem with unitation constraints [6].

Definition 1. Let's define vector $x = (x_1, x_2, \dots, x_n) \in \Omega$. Then the unitation value of x is defined as

$$u(x) := \sum_{i=1}^n x_i. \quad (1)$$

Value of unitation function $u(x)$ depends only on the number of the "ones" in an input binary vector x . The unitation values of two vectors with the same numbers of "ones" are equal.

A problem with unitation constraints is defined as solution e in which unitation value $u(e)$ (the number of the "ones" in solution e) is restricted to a defined number [6].

As was described above the analog circuit synthesis problem has to be viewed as a problem with unitation constraints [6]. Modification of Factorized Distribution Algorithm (FDA) [7] which enables solving problems with unitation constraints was described in [6]. Modification of the UMDA algorithm which is able to handle the problems with unitation constraints is proposed in the text bellow. Pseudo-code of the original UMDA algorithm [5] is presented in Fig. 2.

step0: Set $k = 1$. Generate $n_i \gg 0$ points randomly.

step1: Select $n_s \leq n_i$ points. Compute the marginal frequencies $r_{k,i}(x_i)$ of the selected set.

step2: Generate n_i new points according to the distribution $q_{k+1}(x) = \prod_{i=1}^n r_{k,i}(x_i)$. Set $k = k + 1$.

step3: If not terminated, go to **step1**.

Fig. 2. Pseudo-code of the original UMDA algorithm [1].

In [6] to handle unitation constraints problems only generation phase (sampling) of FDA algorithm was modified. The presented approach was adopted also in the proposed modification of the UMDA algorithm. The UMDA algorithm was implemented using toolbox MATEDA 2.0 [8]. Pseudo-code of the modified UMDA algorithm is presented in Fig. 3.

step0: Set $k = 1$. Generate $n_i \gg 0$ points randomly.

step1: Select $n_s \leq n_i$ points. Compute the marginal frequencies $r_{k,i}(x_i)$ of the selected set.

step2: Generate n_i new points according to the distribution $q_{k+1}(x) = \prod_{i=1}^n r_{k,i}(x_i)$. Set $k = k + 1$.

step3: With regard to unitation constraints repair generated points.

step4: If not terminated, go to **step1**.

Fig. 3. Pseudo-code of the modified UMDA algorithm [1].

One additional step (**step3**) was added to the original UMDA algorithm. In **step3** the generated samples are repaired to satisfy the desired unitation constraints.

The repairing function is applied to every single individual of the population of the generated samples in **step2**. Only n_c "ones" with the highest marginal frequencies $r_{k,i}$ of every generated sample are accepted. The rest of the "ones" of the samples are set to zero. If the number of the "ones" of the sample is equal or lower than n_c then the sample is accepted without any modification and no repairing is performed. This way the number of the "ones" (which corresponds to the number of the components of the encoded analog circuit) of every generated sample never exceeds n_c .

Note that the repairing function is applied only for the part of the encoding vector e which encodes the topology of the solution (characteristic vector c in Fig. 13).

4. The Local Search Algorithm

Evaluation of the cost values and using of the local search algorithm will be discussed in the section. Principal flowchart of this phase is presented in Fig. 4.

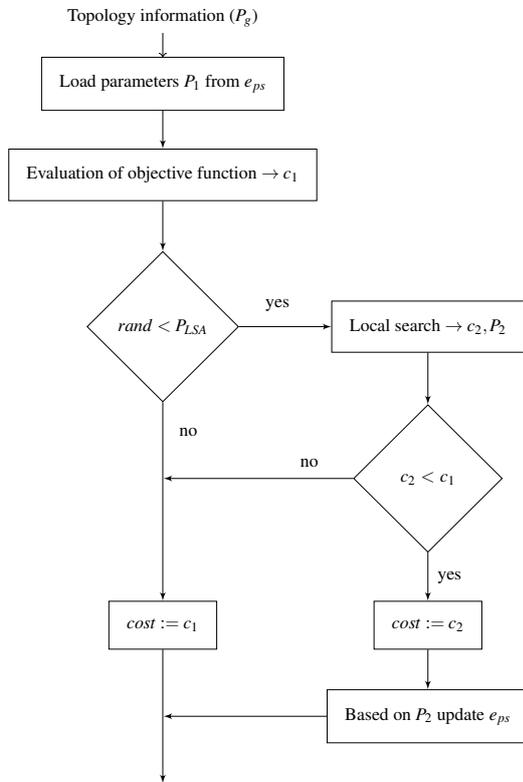


Fig. 4. Evaluation of the cost value and employing of the local search algorithm [1].

The following procedure which is described bellow is performed for every single individual $P_g(i)$ of the population of the generated samples P_g .

Based on the topology information stored in the binary vector of individual $P_g(i)$ appropriate set of parameters P_1 is loaded from parameters storage e_{ps} and cost value c_1 of individual $P_g(i)$ is evaluated.

If the condition of execution of the local search algorithm (LSA) is fulfilled ($rand < P_{LSA}$) the LSA tries to improve accuracy of individual $P_g(i)$. The probability of execution of the LSA is set to $P_{LSA} = 0.02$. The initial point of the search of the LSA is set to parameters set P_1 . The number of the objective function evaluations of the LSA is set to $MaxFunEvals = 100$. The results of the LSA are the cost value of the optimized solution c_2 and set of the optimized parameters P_2 .

If the LSA is successful in improving of the accuracy of individual $P_g(i)$ and its cost value was improved ($c_2 < c_1$) then value $cost$ of individual $P_g(i)$ is set to c_2 ($cost := c_2$) and the appropriate parameters of parameters storage e_{ps} are updated according to parameters set P_2 .

If the condition of execution of the LSA was not fulfilled ($rand > P_{LSA}$) or the LSA was not able to improve the cost value of individual $G(i)$ ($c_2 \geq c_1$) the resulting value $cost$ of individual $P_g(i)$ is set to c_1 ($cost := c_1$).

After performing of the described process cost value $cost$ of individual $P_g(i)$ and updated parameters storage e_{ps} are obtained. During the run of the algorithm the parameters stored in e_{ps} are adapted to the topological information of the good individuals selected in the selection phase of the algorithm (Fig. 1). This way the information about the topology stored in P_g and the information about the parameters stored in e_{ps} are mutually optimized and the whole synthesis process is directed towards the promising areas of the solution space.

5. Application of the Method

A problem of synthesis of a fractional capacitor circuit was adopted from [9] and will be used for demonstration of the synthesis capabilities of the proposed method. The goal is to synthesize a circuit with input impedance (2)

$$Z_{in} = s^{-0.6} \tag{2}$$

In Fig. 5 there is a circuit realization of function (2) as presented in [9]. For the rest of the section, the circuit will be called original approximation circuit.

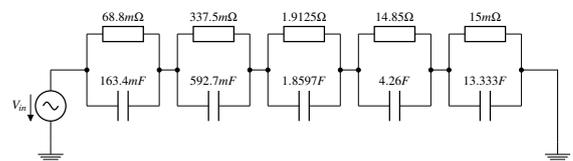


Fig. 5. Schematic of the original approximation circuit [1].

Comparison of the magnitude and the phase of Z_{in} of the original approximation circuit and (2) is presented in Fig. 6 and Fig. 7 respectively. Deviation of the magnitude and the phase of Z_{in} of the original approximation circuit and (2) is presented in Fig. 8 and Fig. 9 respectively.

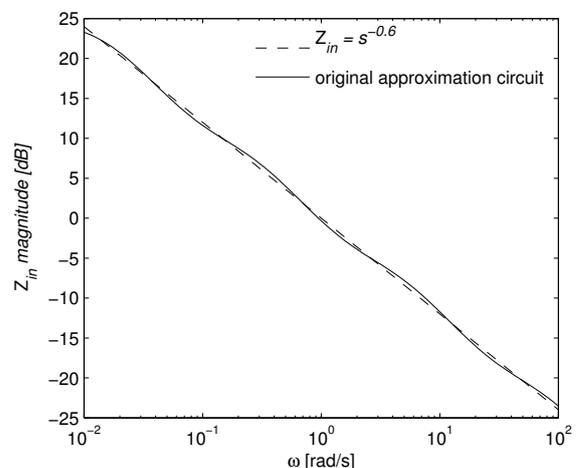


Fig. 6. Comparison of the magnitude characteristics of Z_{in} regarding (2) and the original approximation circuit [1].

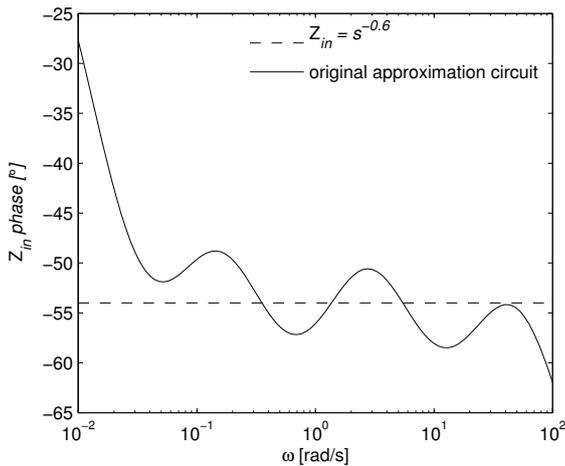


Fig. 7. Comparison of the phase characteristics of Z_{in} closer (2) and the original approximation circuit [1].

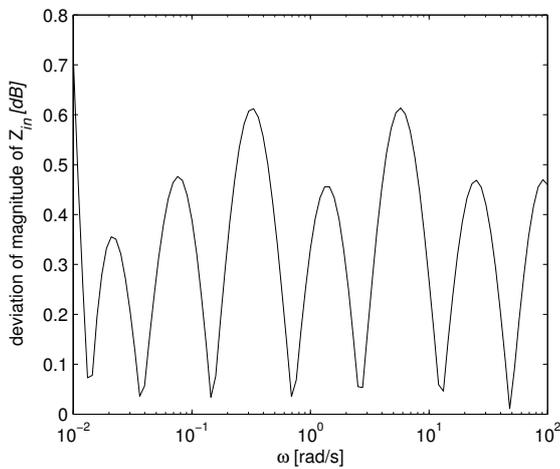


Fig. 8. Deviation of the magnitude of Z_{in} of the original approximation circuit [1].

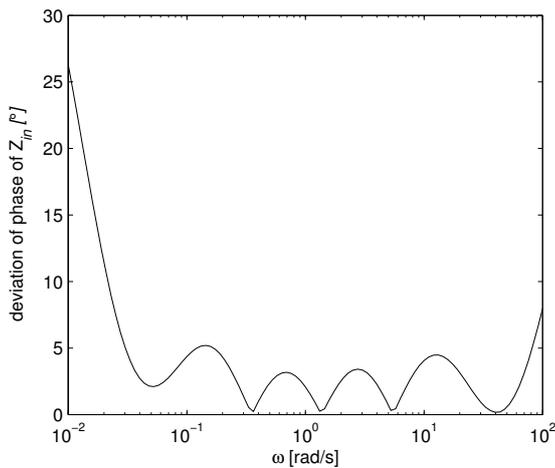


Fig. 9. Deviation of the phase of Z_{in} of the original approximation circuit [1].

The highest deviations of the magnitude and the phase of Z_{in} of the original approximation circuit are presented in Tab. 1.

Magnitude			
ω [rad/s]	0.01	100	0.33
Δ_m [dB]	0.71	0.46	0.61
Phase			
ω [rad/s]	0.01	100	0.14
Δ_p [°]	26.3	7.98	5.2

Tab. 1. The highest deviations of the magnitude and the phase of Z_{in} of the original approximation circuit.

The following sections will be focused on synthesis of the fractional capacitor circuit problem using the proposed hybrid modified UMDA method.

6. The Encoding Method

The used encoding method is based on the idea of fully connected admittance network. For chosen number of the nodes the fully connected admittance network is formed by connecting the admittances between all combinations of the nodes of the network. The number of the admittances of the fully connected admittance network with n_n nodes can be calculated according to (3)

$$n_{adm} = \binom{n_n}{2} = \frac{n_n!}{2!(n_n - 2)!} \tag{3}$$

Every single admittance of the fully connected admittance network can be replaced by resistor, capacitor, inductor or their parallel combination. Therefore the largest circuit which can be for chosen number of the nodes n_n obtained is the circuit where every single admittance of the fully connected admittance network is replaced by parallel combination of resistor, capacitor and inductor. In this paper such circuit is denoted as expanded fully connected admittance network and includes $3n_{adm}$ components. Example of the expanded fully connected admittance network is presented in Fig. 10.

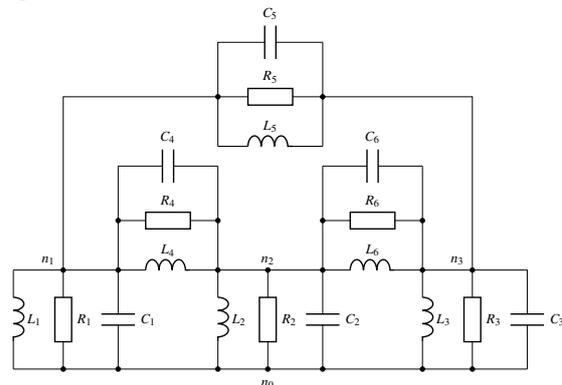


Fig. 10. Expanded fully connected admittance network N_c ($n_c = 4$) [1].

The expanded fully connected admittance network can be represented using complete multigraph with three multiple edges at the most [10]. Complete multigraph G_c corresponding to expanded fully connected admittance network

N_c is presented in Fig. 11. Nodes n_0 to n_3 of network N_c correspond to vertices v_0 to v_3 of complete multigraph G_c . Branches of network N_c correspond to edges of complete multigraph G_c . For example edges $e_5(1), e_5(2), e_5(3)$ (on complete multigraph G_c) correspond to components L_5, R_5, C_5 (in network N_c) respectively. Then the problem of searching of the topology of the analog RLC circuits can be defined as searching of subgraph G_s on complete multigraph G_c [10].

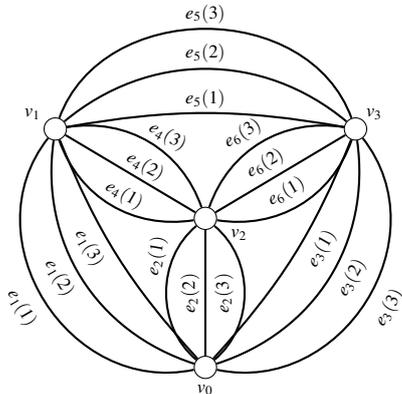


Fig. 11. Complete multigraph G_c representing expanded fully connected admittance network N_c [1].

Subgraph G_s can be encoded using binary characteristic vector c of length $3n_{adm}$. Every single bit of characteristic vector c represents including or not including of the corresponding edge of the complete multigraph G_c in subgraph G_s . For example complete multigraph G_c is encoded using characteristic vector c of length 18 bits where $c(i) = 1$ for $i \in \{1, 2, \dots, 18\}$. Example of subgraph G_s , corresponding analog circuit and its characteristic vector c are presented in Fig. 12.

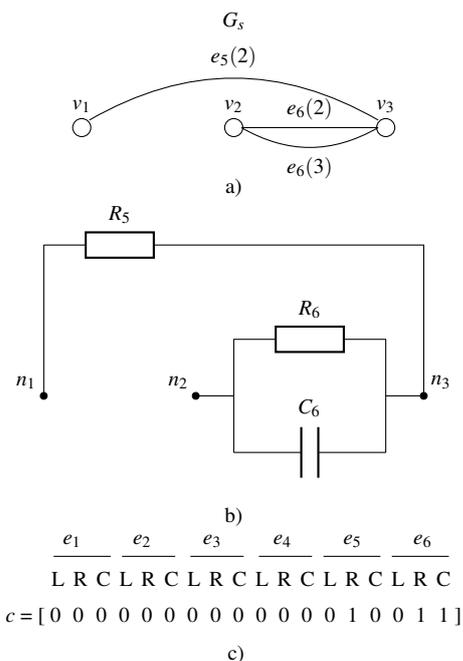


Fig. 12. a) Example of subgraph G_s b) analog circuit corresponding to G_s c) characteristic vector c of G_s [1].

Encoding vector e of every single solution is formed of two parts. The first one represents the topology and is encoded using characteristic graph c approach as described above. The number of the nodes of the expanded fully connected admittance network was experimentally chosen $n_n = 10$. To enable direct comparison of the accuracy of the circuits synthesized using the proposed method and the original approximation circuit presented in [9] the maximum number of the components of the synthesized circuit was set to the number of the components of the original approximation circuit ($n_c = 10$). According to (3) the topology is encoded using binary characteristic vector c of length 135 bits ($3n_{adm}$).

The second part of encoding vector e represents information about the parameters of the components and is represented by vector of real numbers p of length n_c .

Schematic of the used encoding vector e is presented in Fig. 13. The topological information is encoded using binary characteristic vector $c = \{b1, b2, b3, \dots, b135\}$ and the parameters (the values of the components) are encoded using vector of real numbers $p = \{dbl1, dbl2, dbl3, \dots, dbl10\}$.

$$e = \overbrace{[b1 \ b2 \ b3 \ \dots \ b135]}^c \ \overbrace{[dbl1 \ dbl2 \ dbl3 \ \dots \ dbl10]}^p$$

Fig. 13. Schematic diagram of encoding vector e [1].

Based on the components selected in the topological part of the information (characteristic vector c) corresponding values of the parameters are loaded from storage of the parameters e_{ps} and copied to vector p . For example let's assume that the topology is encoded using characteristic vector $c(j) = 1$ for $j \in \{1, 3, 15, 18, 28, 52, 78, 92, 107, 115\}$. Based on the information in characteristic vector c corresponding parameters of storage of the parameters e_{ps} will be loaded to vector of the parameters p as follows: $p(k) = e_{ps}(j)$ for $k \in \{1, 2, \dots, N_c\}$ and $j \in \{1, 3, 15, 18, 28, 52, 78, 92, 107, 115\}$.

Based on the parameters in vector p the values of the components are calculated using formula (4)

$$v = \frac{2 \times 10^6}{1 + e^{(-1.4(10r-14))}} \tag{4}$$

where r are values of the parameters loaded from vector of the parameters p . Formula (4) was formed to map the values of the parameters stored in vector p to suitable range of the values of the components. Since the parameters in vector p are set in the range $\langle 0, 1 \rangle$ corresponding values of the components for the lowest $r = 0$ and for the highest $r = 1$ are $v_{min} = 0.0061$ and $v_{max} = 7.3685 \times 10^3$ respectively. Note that formula (4) is used for all three types of components RLC. Since the used angular frequency range is from 0.01 rad/s to 100 rad/s, the values of the components are set to non-realistic values.

7. The Objective Function

Cost value *cost* is according to (7) computed as weighted summation of the magnitude and the phase differences. Difference of magnitude Δ_m is according to (5) calculated as weighted absolute value of differences of desired magnitude function f_{md} and magnitude of current solution f_{mc} over $m = 101$ frequency points in the range 0.01 rad/s to 100 rad/s. Similarly difference of phase Δ_p is according to (6) calculated as weighted absolute value of differences of desired phase function f_{pd} and phase of current solution f_{pc} .

$$\Delta_m = \frac{1}{m} \sum_{i=1}^m w_{dm}(i) |f_{md}(i) - f_{mc}(i)| \tag{5}$$

$$\Delta_p = \frac{1}{m} \sum_{i=1}^m w_{dp}(i) |f_{pd}(i) - f_{pc}(i)| \tag{6}$$

$$cost = \Delta_m w_{cm} + \Delta_p w_{cp}. \tag{7}$$

Weights w_{cm} and w_{cp} were set to 1 and 2 respectively. Setting of weights w_{dm} , w_{dp} is presented in Tab. 2. All weight coefficients were set experimentally.

angular frequency range:	w_{dm}	w_{dp}
0.01 rad/s to 0.0398 rad/s	1.3	1.3
0.0437 rad/s to 20.8930 rad/s	1	1
22.9087 rad/s to 100 rad/s	1.3	1.3

Tab. 2. Setting of weights w_{dm} and w_{dp} .

Frequency responses of the current solution f_{mc} and f_{pc} are obtained using nodal analysis method implemented in Matlab.

8. Settings of the Proposed Algorithm

The goal of the synthesis is to design a circuit which approximates function (2). The only information supplied to the system is desired magnitude and phase characteristics (2), maximum number of the used components ($n_c = 10$), maximal number of the nodes ($n_n = 10$) and types of the used components (resistors, capacitors, inductors).

The number of the objective function evaluations (evals) required by the proposed algorithm consists of the number of the evaluations required for calculation of the cost values of all individuals of the population (*PopEvals*) and the number of the evaluations required by the used local search algorithm (*LSEvals*). Population size was set $PopSize = 200$ and number of generations was set $MaxGen = 200$. Therefore $PopEvals = 40e3$. The local search method requires $MaxFunEvals = 100$ evaluations in each its run and it is executed with probability $P_{LSA} = 0.02$ (2% Lamarckian approach [11]). The condition of execution of LSA is tested during every single objective function evaluation. Therefore $LSEvals = 80e3$ and the total number of the objective function evaluations required by the proposed algorithm is $120e3 (PopEvals + LSEvals)$. Local search algorithm was realized using Matlab function *fmincon*.

All parameters of the synthesized problem and settings of the proposed algorithm are summarized in Tab. 3.

maximum number of the nodes (n_n)	10 (0 to 9)
maximum number of the components (n_c)	10
used types of the components	R,L,C
negative resistors	not allowed
angular frequency range	0.01 rad/s to 100 rad/s
number of the points (m)	101 (25 points/decade)
population size (<i>PopSize</i>)	200
number of generations (<i>MaxGen</i>)	200
probability of execution of LSA (P_{LSA})	0.02
w_{cm}	1
w_{cp}	2

Tab. 3. Settings of the proposed algorithm.

The algorithm UMDA is realized using Matlab toolbox MATEDA 2.0 [8]. MATEDA initialization file is presented in Fig. 14

```
PopSize = 200; n = 135; cache = [0,0,0,0,0];
Card = 2*ones(1,n); MaxGen = 200; MaxVal = -1e-2;
stop_cond_params = {MaxGen,MaxVal};
Cliques = CreateMarkovModel(n, 0);
edaparams{1} = {'seeding_pop_method','seedingFract',25};
edaparams{2} = {'learning_method','LearnFDA',{Cliques}};
edaparams{3} = {'sampling_method','SampleFDAmoDiF',{PopSize}};
edaparams{4} = {'stop_cond_method','maxgen_maxval',stop_cond_params};
[AllStat,Cache]=RunEDAfractal(PopSize, n, F, Card, cache, edaparams);
```

Fig. 14. Configuring of MATEDA 2.0 toolbox for realization of the proposed algorithm [1].

The whole program flow of the UMDA algorithm is realized using the functions of MATEDA 2.0 toolbox. The only exception is the sampling phase of the algorithm which is modified to enable dealing with the problems with unitation constraints. All the parameters in Tab. 2 and Tab. 3 were set experimentally after high number of experiments. The experiments were performed on a computer with processor AMD Athlon II X2 245, 6GB RAM and operational system Centos 6.5.

9. Experiments and The Solutions

There were executed 20 instances of the proposed algorithm. Average running time of a single execution was 11 min. The cost values of the solutions are presented in Tab. 4.

id of run	1	2	3	4	5
cost value	3.805	2.442	3.805	2.431	2.428
id of run	6	7	8	9	10
cost value	2.437	2.443	3.653	2.433	2.436
id of run	11	12	13	14	15
cost value	2.432	3.662	5.197	5.663	5.353
id of run	16	17	18	19	20
cost value	6.071	3.805	5.691	6.072	2.429

Tab. 4. Results of 20 runs of the proposed algorithm.

As can be seen in Tab. 4 the best solution was achieved in run 5 with cost value 2.428. The schematic diagram is presented in Fig. 15. Schematic diagrams of another three good solutions (run 4, run 11, run 20) are presented in Fig. 16 to Fig. 18.

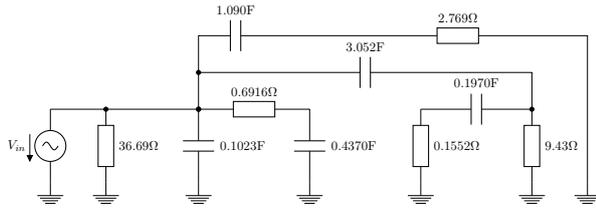


Fig. 15. Schematic of the circuit synthesized in run 5 [1].

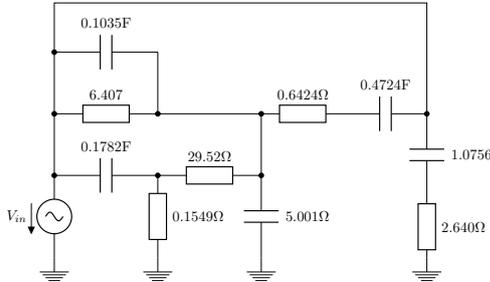


Fig. 16. Schematic of the circuit synthesized in run 4 [1].

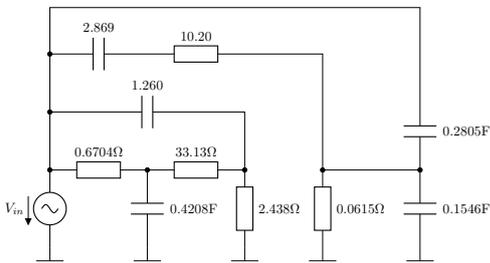


Fig. 17. Schematic of the circuit synthesized in run 11 [1].

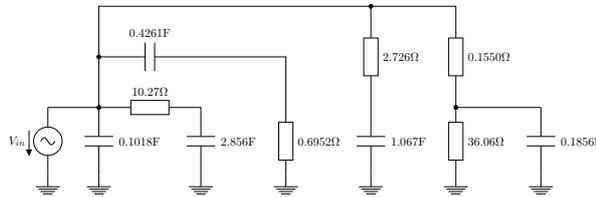


Fig. 18. Schematic of the circuit synthesized in run 20 [1].

Comparison of the magnitude and the phase characteristics of Z_{in} of the best found approximation circuit and desired function (2) are presented in Fig. 19 and Fig. 20 respectively.

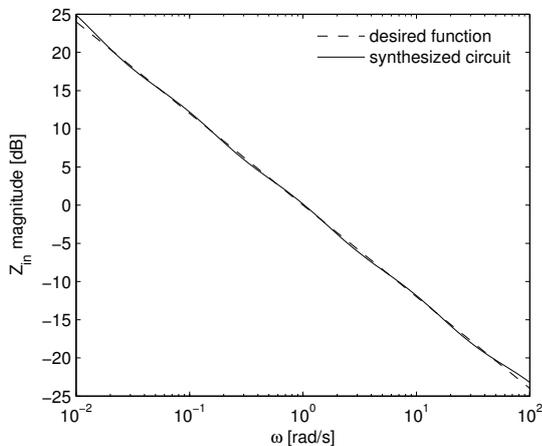


Fig. 19. Comparison of the magnitude of Z_{in} of the best found approximation circuit and (2) [1].

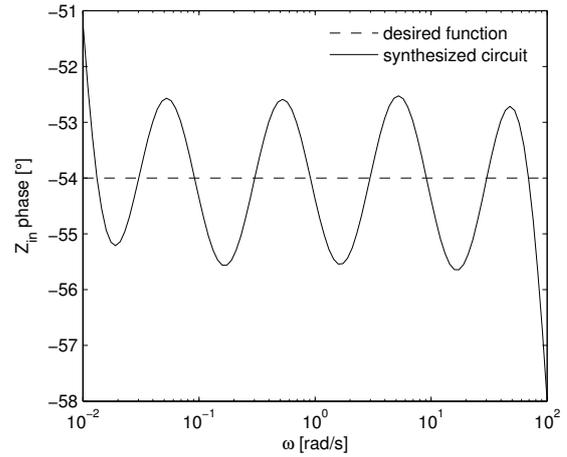


Fig. 20. Comparison of the phase of Z_{in} of the best found approximation circuit and (2) [1].

Absolute values of the deviations of the magnitude and the phase of Z_{in} of the best synthesized circuit are presented in Fig. 21. and Fig. 22 respectively.

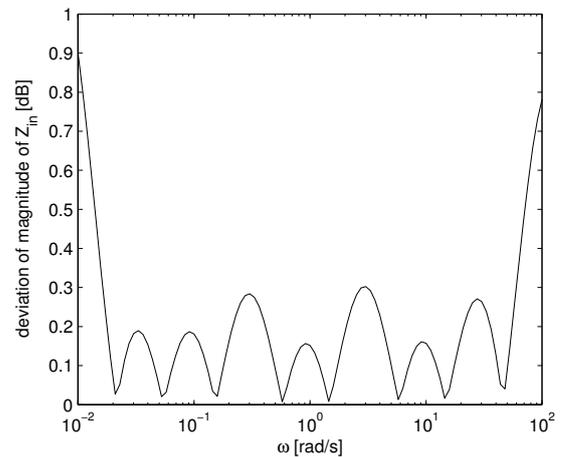


Fig. 21. Deviation of the magnitude of Z_{in} of the best found approximation circuit [1].

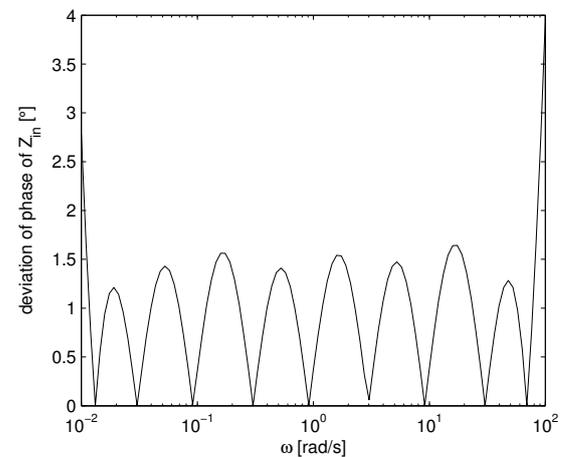


Fig. 22. Deviation of the phase of Z_{in} of the best found approximation circuit [1].

Three highest deviations of the magnitude and the phase characteristics of Z_{in} of the best synthesized circuit are summarized in Tab. 5.

Magnitude			
ω [rad/s]	0.01	100	3.02
Δ_m [dB]	0.9	0.78	0.30
Phase			
ω [rad/s]	0.01	100	17.4
Δ_p [°]	2.78	3.97	1.64

Tab. 5. The highest deviations of the magnitude and the phase of Z_{in} of the best synthesized approximation circuit.

As can be seen in Fig. 19 to Fig. 22 the maximum deviations of the magnitude and phase responses are located at the boundaries of the used frequency range. At these frequencies the unoptimized areas of the frequency response (0 to 10^{-2} rad/s and 10^2 to ∞ rad/s) affect behavior of the circuit in the area where the optimization was performed. The zeros and poles diagram of the synthesized circuit is presented in Fig. 23. All coefficients of the denominator of the approximation function of Z_{in} are positive therefore stability of the synthesized circuits is guaranteed.

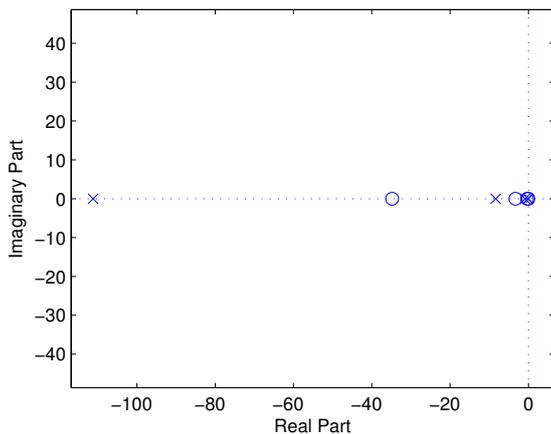


Fig. 23. The zeros and poles diagram of the best synthesized circuit [1].

Although the probability of using of all three component types (resistors, capacitors, inductors) was equal during the synthesis process, none of the circuits presented in Fig. 15 to Fig. 18 include any inductors. As the proposed algorithm was constrained to use only $n_c = 10$ components, it seems that using only capacitors and resistors allows the method to reach lower cost values than in solutions where inductors are included.

10. Comparison of The Results

In the section the best synthesized approximation circuit obtained using the proposed algorithm will be compared to the original approximation circuit designed in [9] by a classical method of the analog circuits design.

Since the proposed evolutionary synthesis method was configured to use the same circuit complexity (10 components at the most) as the original approximation circuit, accuracy of both circuits can be directly compared.

Except the deviations at the boundaries of the used frequency range (as was commented above) for the original approximation circuit the highest deviation of the magnitude is $\Delta_m = 0.61$ dB at angular frequency 0.33 rad/s. For the best solution of the proposed method the highest deviation of the magnitude is $\Delta_m = 0.27$ dB at angular frequency 0.30 rad/s. Thus in terms of deviation of the magnitude the accuracy of the synthesized circuit is more than twice better than the original approximation circuit. Comparison of the deviations of the magnitude of Z_{in} for both circuits is presented in Tab. 6.

original circuit	ω [rad/s]	0.01	100	0.33
	Δ_m [dB]	0.71	0.46	0.61
synthesized circuit	ω [rad/s]	0.01	100	0.30
	Δ_m [dB]	0.93	0.92	0.27

Tab. 6. Comparison of the deviations of the magnitude of Z_{in} of the original approximation circuit and the best synthesized circuit.

The highest phase deviation inside the used frequency range is for original circuit $\Delta_p = 5.2^\circ$ at angular frequency 0.14 rad/s and for the synthesized circuit it is $\Delta_p = 1.5^\circ$ at angular frequency 0.58 rad/s. Thus phase accuracy of the best synthesized circuit is more than three times better than the original approximation circuit. Comparison of the maximum deviations of the phase of Z_{in} is presented in Tab. 7.

original circuit	ω [rad/s]	0.01	100	0.14
	Δ_p [°]	26.3	7.98	5.2
synthesized circuit	ω [rad/s]	0.01	100	0.58
	Δ_p [°]	3.0	4.2	1.5

Tab. 7. Comparison of the deviations of the phase of Z_{in} of the original approximation circuit and the best synthesized circuit.

In [12] the same problem of synthesis of the fractional capacitor circuit was solved using simulated annealing method. The method was able to reach solutions of the same accuracy however the number of required evaluations of the objective function was almost four times higher. Comparison of accuracy of the best solutions and numbers of evaluations of the objective function of the proposed EDA method and simulated annealing method [12] is presented in Tab. 8.

simulated annealing method [12]	best cost	2.45
	evals	440e3
the proposed EDA method	best cost	2.43
	evals	120e3

Tab. 8. Comparison of the proposed EDA method and simulated annealing method presented in [12].

11. Conclusion

Automated analog circuit synthesis approach based on hybrid evolutionary method employing modified UMDA algorithm and a local search algorithm was presented in the paper. Used hybrid approach enables to employ specialized methods for both sub problems of different nature (synthesis of the topology and determination of the parameters).

Synthesis of the topology which is combinational optimization problem was solved using modified UMDA algorithm. Determination of the parameters which is continuous optimization problem was solved using a local search algorithm. The principle of the method is based on mutual interaction of synthesis of the topology phase (modified UMDA algorithm) and determination of the parameters phase (the local search algorithm) of the desired solution. Modification of the UMDA algorithm which allows solving problems with uniteration constrains was proposed in the paper.

The proposed method was verified on the problem of synthesis of the fractional capacitor circuit introduced in [9]. Presented experiments have shown that the proposed algorithm is capable to synthesize solutions with accuracy overperforming solutions obtained using a classical method of the analog circuit design given in [9]. Accuracy of the magnitude of Z_{in} of the best obtained solution was more than twice better than the original approximation circuit. Accuracy of the phase of Z_{in} of the best obtained solution was more than three times better than the original approximation circuit.

In [12] the problem of fractional capacitor circuit realization was solved using simulated annealing method (SA). The accuracy of the circuits synthesized using SA was the same as the solutions produced using the proposed EDA method.

However SA required much higher number of the objective function evaluations. While the proposed EDA method required 120e3 objective function evaluations for synthesis of the same problem SA required 440e3 objective function evaluations.

For demonstration purposes the presented algorithm was verified using nodal analysis circuit simulator implemented in Matlab. Another improvement of the efficiency of the algorithm can be achieved using Model Order Reduction Techniques [13].

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