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FIELD PROGRAMMABLE GATE ARRAYS USAGE IN INDUSTRIAL AUTOMATION SYSTEMS

UŽITÍ PROGRAMOVATELNÝCH HRADLOVÝCH POLÍ V SYSTÉMECH PRUMYSLOVÉ AUTOMATIZACE

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Chapter 1

Introduction

Today’s, industrial automation systems are highly complex networks of embedded systems consisting of many sensors, drives, controllers, and intelligent I/O devices. Recently, Field Programmable Gate Arrays (FPGAs) are used throughout industrial automation systems to add intelligence, flexibility, and high precision control. Their applications include motion control, machine to machine communications, motor drives, diagnosis and fault-tolerant control, smart energy and smart grid, big data analytic, etc.

Generally, when the FPGAs are used in motor drives, they implement complex control algorithms and modulation switching. Additionally, they can provide functions for fault protection of motor such open circuit and short circuit. In other words, the FPGAs usage is limited to motor control and modulation switching, but they are not used to detect the problems of inverter components during the switching process. For example, the monitoring of the IGBT switching process (turn-on, turn-off) in a power inverter may lead to predict and diagnose the faults before the complete degradation occurrence in the drive system.

Mostly, no methods exist for continuous monitoring of inverter switching transistor condition or other parts of power inverter such as DC link capacitance, leakage resistance, or terminals contact resistances etc. Diagnostic methods based on continuous condition monitoring, which were developed for mechanical vibration monitoring or for many other fields - for example ball bearing condition monitoring or partial discharges in motor winding, do not exist for IGBT transistors proper operation. The quality of switching process is possible to observe only on transients, when the transistor switches on or off. Based on the study presented in chapter 2, it could be noted that several factors affect the switching transient in the transistor: transistor switching speed, gate resistance, gate current, gate voltage, DC link capacitance, snubbers capacitance, etc. Among these quantities, which can be measured, are collector-emitter voltage $V_{CE}$, gate-emitter voltage $V_{GE}$ and gate current $I_G$. These quantities are only measurable in the IGBT gate driver in the inverter. Based on the quantities measurements and their quantitative evaluation, the degree of degradation in the power compo-
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Components (IGBT transistors, diodes, capacitors, etc.) may be predicted, where the characteristic of these components change during the degradation. Therefore, the diagnostic methods, which depend on measuring and monitoring the IGBT quantities during the switching process in the gate drive circuits, should lead to predict the critical degree of the components degradation. Accordingly, the maintenance can be scheduled to avoid the failure of the components during the operation.

As long as the IGBT gate driver is used to measure and monitor the required quantities for the diagnosis, a new hardware for the gate driver is required. In addition to its basic functions (turn-on, turn-off), the gate driver should be able to perform measurements, recording, and mathematical analysis during the IGBT switching process. The digital signal processing for the analysis and recording is required. Generally, Fast Fourier Transform (FFT) or Wavelet transform are used for this purpose. Therefore, the implementation of programmable devices, which are placed directly on the gate driver, are required. The programmable devices may be Field Programmable Gate Arrays (FPGAs) or microprocessors.

1.1 Motivation and Objectives

The idea is to integrate the diagnostic functions into the IGBT gate driver circuits. These functions should allow analysis of the required quantities in the IGBT transistor and its gate driver. The purpose is to measure and monitor these signals during the IGBT switching process. The quantitative evaluation of the measured parameters, which are recorded and analyzed using programmable devices, can indicate the degree of the degradation. As a result, the IGBT failure can be predicted and it would be able to plan the targeted service (replacement of specific IGBT, driver, capacitor).

The aim is to design a hardware of the IGBT gate driver, which would allow achieving the previous properties.

The structure of the proposed IGBT gate driver can be summarized as follows:

1. Multiple gate stages outputs for realization of variable gate resistance by sequential switching. It allows realization of linear charging of gate capacitance delayed sequential switching signals are generated in the FPGA and are programmed in HDL language.

2. Programmable devices (FPGAs) for recording and analysis of the digital signals.

3. Multiple power supplies for IGBT gate stages and for FPGA feeding.

4. Driver interface to inverter control system with data exchange capability except standard PWM signal. The insulated SPI interface is used for this purpose.
Chapter 2

Background and State of the Art

The scope of this chapter is focused on the IGBT transistor basics (structure, switching operation, control) [18] [8] [46] [21]. This chapter also reviews the current state of the art of the IGBT transistor faults, fault detection and diagnosis and the fault-tolerant control.

The IGBT turn-on and turn-off are controlled by the gate voltage, and the speed of switching is determined by the gate current. The gate drive circuit feeds the IGBT gate signals. Therefore, it is considered as an interface between the logic signals generated from the controller and the signals of IGBT gate [5]. There are two types of gate drive circuits, namely, voltage drive and current drive. The gate drive circuit generates a positive voltage $+V_{GE}$ during the turn-on, and a negative voltage $-V_{GE}$ during the turn-off. Moreover, the gate drive circuit should control the time change rate $di/dt$ of the IGBT collector current to avoid excessive Electro-Magnetic Interference (EMI), and it should control the time change rate $dV_{CE}/dt$ of the IGBT collector-emitter voltage to avoid the IGBT latch up [24] [25].

Equation 2.1 is used to calculate the peak value of the current flowed to charge and discharge the gate during the IGBT switching.

$$I_{GP} = \frac{+V_{GE} + \mid -V_{GE}\mid}{R_G + R_g}$$  \hspace{1cm} (2.1)

where $R_G$ is the external gate resistor and $R_g$ is the internal gate resistor.

A small gate resistor reduces the switching times and switching losses, but this may cause a high surge voltage. The value of the gate resistor has a significant impact on the turn-on speed of IGBTs, while it barely affects the turn off speed.

The average value of the drive current $I_G$ can be calculated by Equation 2.2.

$$+I_G = -I_G = f_{sw} \times (\mid +Q_g\mid + \mid -Q_g\mid)$$  \hspace{1cm} (2.2)
where $+Q_g$ is the gate charge from 0V to $+V_{GE}$ and $-Q_g$ is the gate charge from $-V_{GE}$ to 0V. The gate drive power $P_{d(on)}$ required to turn on the IGBT is given by

$$P_{d(on)} = f_{sw} \times \left[ \frac{1}{2} \times (|+Q_g| + |-Q_g|) \times (|+V_{GE}| + |-V_{GE}|) \right]$$  \hspace{1cm} (2.3)

supposing that the gate drive power $P_{d(off)}$ required to turn off the IGBT is equal to the power $P_{d(on)}$, then the gate drive power $P_d$ required to drive the IGBT switching is written as the following

$$P_d = P_{d(on)} + P_{d(off)} = f_{sw} \times \left[ (|+Q_g| + |-Q_g|) \times (|+V_{GE}| + |-V_{GE}|) \right].$$  \hspace{1cm} (2.4)

### 2.1 Present State in Inverter Diagnosis

The components of a drive system depend on their function and the place of use. Therefore, the faults and their causes may differ from system to another. The two components most prone to failure in the drive system are electrolytic filtering capacitors [22] and power devices, but 38% of faults in the drive systems occur due to the failure of power devices during the switching operation [26].

The causes of failure in the drive system were briefly discussed in [1].

The IGBT open circuit faults, which are defined as electrical causes, may be caused by the lifting of bonding wires [3] [27], or by the gate driver failure [38] [36]. The open circuit fault is not considered a fatal fault, but it can lead to another fault in healthy parts. Therefore, it is necessary to get rid of these faults to protect the system from the complete failure. Several detection methods for open circuit faults were developed in [17] [30] [41].

The short-circuit (SC) is considered the usual fault mode of semiconductors, because the short-circuit faults are very destructive. Therefore, the protection and diagnosis system requires special measures to turn off the drive system immediately. The IGBTs SC withstand time, which can be in the range of 6$\mu$s to 10$\mu$s, is dependent on their type and structure. If the protection circuit failed to turn off the IGBT during the withstand time, the IGBT will be destroyed.

Generally, all the output stages of the proposed gate drive circuits have a gate resistor that is split into two resistors $R_{G(on)}$ for switching turn-on, and $R_{G(off)}$ for switching turn off. This allows controlling and optimizing the switching turn on and switching turn off separately [11] [10].

The desaturation technique is a common method for detection the fault occurrence in the IGBT device [9] [16]. The detection of SC fault is achieved, if the collector emitter voltage $V_{CE}$ rises above 5-8 volts during the on-state operation. The SC condition indicates that the collector current $I_C$ has exceeded the normal value. This method is simple because it uses only a diode for sensing the fault.

A new IGBT protection circuits are proposed in [14] [42] to accelerate the fault detection time.
All proposed SC protection circuits include a soft turn off technique to reduce voltage spike caused by the high current falling rate, where the soft shutdown method increases the system reliability under the SC conditions [7].

Recently, SC protection circuits based on the gate voltage monitoring were proposed [23] [34].

The IGBT turn-on and turn-off are treated as transient phenomena. During the switching transient of the IGBT devices, the power dissipation and switching stress increase. Therefore, the switching speed is required to reduce the effect of these phenomena on the IGBT performance. In other words, the IGBT protection against the transient surge is required [37] [15] [33].

Recently, the fault detection and diagnosis in drive systems depend on the online monitoring and measurement [29] [45], where the extracted online information can be used for the design of fault tolerant control system (FTCS). Few works have described the ability of online fault detection and diagnosis [2].

The IGBT devices and any power devices used in the drive system are prone to high temperatures during the operation. Therefore, the protection of IGBT against degradation is important. There are variety of methods used for measuring the temperature of the IGBT device [6] [19].

The fault detection and isolation (FDI), fault detection and diagnosis (FDD), and fault-tolerant control (FTC) and the interaction between them are considered a suitable way for improving reliability and flexibility of drive systems. In addition, the cost of repair and maintenance decreases highly.

The FTCS used in IGBT inverters depends on the redundant components. The FTCS improves both the reliability and the safety of technical systems. Additionally, the FTCS reduces the maintenance costs, which are very expensive, and it improves the life time of the drive system. In the literature, several approaches have dealt with the fault tolerant control (FTC) in drive systems that are fed by IGBT inverters [43] [12].

Based on the previous review, it is noted that the control units used in the drive systems play the key role in FDD and FTC. Generally, the control unit is composed of hardware and software. The hardware includes the gate driver, protection and diagnosis circuits, controller, whereas the software includes all algorithms for FDD and FTC. In order to minimize the time between the fault detection and diagnosis, using the field programmable gate arrays (FPGAs) is the new solution for the FTCSs, power electronics, and drive applications [28]. FPGAs can perform networking and control support simultaneously. A single FPGA can do the work of dozens of microcontrollers. Therefore, the microcontroller is going to disappear with the FPGA appearance. The industrial control systems based on the FPGAs design proved their flexibility, reliability, capacity, and fast response in difficult conditions.

Nowadays, complex functions for power electronic systems are implemented using the FPGA controller design. The FPGA controller was used in the application of switching power converters [13]. The use of FPGAs in voltage source inverters fed
induction machines has been discussed in the literature. The proposed digital control
circuit for multilevel multipulse source voltage converter, which is presented in [31]
[35], is based on the FPGA design. Additionally, a lot of researches discussed the
design and implementation of PID controllers using FPGA [47] [47].

Generally, standard drivers are built according to the architecture shown in Figure 2.1.
They include usually an output stage, secondary logic, protection circuits and sec-
ondary part of insulated power source on the secondary side (side of power transis-
tor). Whereas on the primary side, there are primary parts of power source and primary
logic. The control PWM signals and power supply are transferred through the insula-
tion barrier to the secondary side and transistor/driver error signals are transferred to
the primary side.

![Figure 2.1: Standard driver architecture [20].](image)

The Insulation barrier must have high $du/dt$ immunity, low parasitic capacity and
static insulating capability according to the application field of the driver. The insula-
tion barriers are usually realized using opto-couplers or signal transformers. There are
now high speed logic isolators. Since the problem of isolation is still the main issue
for designers and researchers, other techniques for isolation barriers were presented in
the literature, for example the proposed method in [4] discussed the implementation of
an IGBT control signal by wireless transmission, while the proposed method in [39]
used a printed transformer which can insulate a voltage of 10kV.
Chapter 3

Proposed IGBT Gate Driver Architecture

From Figure 2.1 in section 2.1, the development of the gate driver architecture is necessary for purposes of the proposed diagnosis in the developed gate driver. The proposed gate drive circuit architecture is shown in Figure 3.1, where the analog measurements of required quantities are implemented on the secondary side of the proposed gate driver. The measured quantities are $V_{CE}$, $V_{GE}$, and $I_{G}$. Additionally, the load current $I_{L}$ can also be measured. The transients of these quantities can be evaluated. Then, the quality of switching process can be monitored.
3.1 Gate Driver Interface

The data transfer of PWM control signal and back transfer of fault signal are assumed using separate insulated channels, as shown in Figure 3.2. Separate fault signal is not necessary, because the error information is also transferred through the data interface. However, in the case of requirement for switching-off other transistors of inverter simultaneously, it is necessary to separate the fault signals.

The bi-direction data synchronized with the inverter control unit (main controller) require a high communication speed, reliability, and simplicity of implementation. There are many types of serial communication interface, which can be used for this purpose. A Synchronous Peripheral Interface (SPI) is used in the drive system, as shown in Figure 3.2.

3.2 Data Exchange SPI Protocol

Data exchange is realized between the main controller of the inverter and the gate driver FPGA by a simple communication protocol for SPI as shown in Figure 3.3.
### CHAPTER 3. PROPOSED IGBT GATE DRIVER ARCHITECTURE

(a) Data frame for writing parameter into one gate driver memory.

(b) Data frame back reading of parameter or an individual variable.

(c) Data frame for periodic data exchange between driver and inverter controller.

![Figure 3.3: Proposed SPI data transfer protocol.](image-url)
3.3 The proposed IGBT Gate Driver

Figure 3.4 shows the detail of the proposed IGBT gate driver for one channel. The IGBT gate driver for one channel, whether the upper or the bottom, includes the following components:

- **FPGA based controller**: It receives the measured digital signals, such as $I_C$, $V_{GE}$, $I_G$ and $V_{CE}$, from high speed parallel ADCs across buffer functions using a Verilog program.

- **High speed parallel analog digital converters**: High speed (105 MSPS), high resolution (10 bit) ADCs are used in the design. Their analog inputs are the outputs of the dedicated circuits for the quantities which are going to be measured. The ADCs are operated with the internal reference of 1 V or 0.5 V, this depends the configuration. The ADCs clocks are generated by the gate driver FPGA using Verilog code and another tools. The clock frequency range must be from 50 MHz to 105 MHz, this is based on the required sampling rate.

- **Voltage references**.
• Parallel gate drive stages: They are used to control the external gate resistors during the turn on/off.

• Stages control signals: They are used for controlling the parallel stages inputs. A verilog code can be written for generating these control signals which assert delay times between the gate stages during the IGBT switching.

• Insulator: A high speed logic isolator could be used.

• High speed communication: An SPI interface can be used to achieve the exchange data between the main controller and the used FPGAs based controller which are used to analysis the measured digital signals in the gate driver.

• Dedicated circuits: They can be voltage dividers, operational amplifiers, anti-aliasing filters, etc.

• Insulated DC/DC converter: The zero voltage zero current (ZVSZCS) push-pull resonant topology and regulators will be designed for this purpose.

### 3.4 Design of the Proposed IGBT Gate Driver

#### 3.4.1 Design of the Driver Stages of Proposed IGBT Gate Driver

Figure 3.5 depicts the block diagram of the driver stages for the upper and bottom transistor of dual IGBT module. These stages are divided into two channels: Upper channel for the upper transistor, and bottom channel for the bottom transistor. Each

![Block diagram of the parallel driver stages used in the proposed gate drive circuit.](image)
CHAPTER 3. PROPOSED IGBT GATE DRIVER ARCHITECTURE

Channel is composed of three parallel driver stages. The stages output of each channel feeds its own transistor in the dual IGBT module. These stages are responsible for the IGBT switching (turn-on, turn-off) during the operation. Figure 3.6 shows the driver stage structure in each channel where X indicates the stage number. The transistor P-channel MOSFET Q1X is used for the IGBT turning on, while the transistor N-channel MOSFET Q2X is used for the IGBT turning off. The turn-on voltage of the IGBT is approximately $+15\,\text{V}$, and the turn-off voltage is about $-8\,\text{V}$. Accordingly, the voltage drop along the charging/discharging path can be calculated as follows

$$\Delta V_{GE} = +15\,\text{V} - (-8\,\text{V}) = 23\,\text{V}$$

The source pin of the transistor Q1X is connected to the positive supply of 15 V, and the source pin of the transistor Q2X is connected to the negative supply $-8\,\text{V}$. Therefore the Q2X is turned off, if its source becomes more negative than the gate voltage.

The maximum IGBT gate current $I_G$ is determined according to the external resistors, where the external gate resistors $R_{G(on)}$ limit the gate current $I_{G(on)}$ during the turning on, and the resistors $R_{G(off)}$ limit the gate current $I_{G(off)}$ during the turning off. Moreover, the gate driver with this structure can control the $du/dt$ and $di/dt$.

The Q1X switching (turn-on/off) is controlled by the emitter follower (Q3X, Q4X) with single power supply, whereas the Q2X switching is controlled by the emitter follower (Q5X, Q6X). This follower is fed by positive voltage $+15\,\text{V}$ for the collector of the NPN transistor Q5X and from the negative voltage $-8\,\text{V}$ for the collector of the PNP transistor Q6X.

![Figure 3.6: Schematic diagram of single driver stage in one channel.](image-url)
The small signal transistors N-MOSFET Q7X, and P-MOSFET Q8X are considered as an input stage. They are controlled digitally by the FPGA controller. Each stage consists of two transistors controlled by different signals in the FPGA controller, as shown in Figure 3.7. The structure of this gate driver allows controlling the gate resistors $R_{G(on)}$ and $R_{G(off)}$. The digital signals used for switching the small transistors have a delay time $t_d$ which allows controlling the gate resistors sequentially during the IGBT operation (turn-on, turn-off). According to the datasheet of the IGBT module FF1000R17IE4 [40], and based on the Equation 2.1 in chapter 2, the peak value of current, which has to be provided by the first gate stage in each channel, for charging and discharging the gate during the IGBT switching, is

\[
I_{GP(stage)} = \frac{15 + |{-8}|}{5 + 1.5} \approx 3.54 \text{ A}
\]

### 3.4.2 Design of the Power Supply System for the Proposed IGBT Gate Driver

Figure 3.8 illustrates the block diagram of the power supply system used for the proposed IGBT gate driver, where two insulated DC/DC converters are used. Each one...
provides isolated output 16 V/1.6 A. The output of each converter feeds the following regulators:

- Positive regulator with output 15 V/0.4 A.
- Negative regulator with output −8 V/0.4 A.
- Positive regulator with output 5 V/2.5 A for the FPGA controller.

In addition, the proposed gate driver requires a power supply with output voltage 3.3 V, which can be fed from the FPGA controller.

### 3.4.2.1 Design of the Insulated DC/DC Converters

Two ZVSZCS push pull resonant converters are provided in the design, where each converter feeds its own channel in the IGBT gate drive circuit with an output power 25.6 W and a current 1.6 A. Figure 3.9 depicts the schematic circuit of the push pull resonant converters with bridge rectifiers used for the proposed design.

### 3.4.3 The Proposed Analog to Digital Converters Design

As previously mentioned, the important quantities, which are measured during the IGBT switching process (turn-on, turn-off), are $I_G$, $V_{GE}$ and $V_{CE}$. The ADC devices convert the analog signals of the measured quantities to digital signals for analysis.
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and processing. The quantitative evaluation determines the IGBT degree of degradation. Generally, the IGBT switching process is between 2-4 $\mu$s. Therefore, the ADC converters must be fast for digitizing the input signals during the switching process within this period. Figure 3.10 represents the block diagram of the ADC converters (AD9215) interface to the FPGA controller. A simple HDL code can be used to sample ADCs data at FPGA inputs. In addition to HDL code, the User Constraints File (UCF) is required to specify the pins location in the FPGA controller.

Figure 3.9: The schematic circuit of the push pull DC/DC converters used in power supply system.

Figure 3.10: ADC Devices interface to the FPGA controller.
Chapter 4

FPGA Board Design for IGBT Control and Diagnosis

4.1 Proposed FPGA Board Design

Figure 4.1 shows the block diagram of the FPGA board used for the control and the diagnosis during the switching of the IGBT transistor. As can be seen from Figure 4.1 the hardware features are:

- Kintex-7 XC7K70T-FBG484.

Figure 4.1: Block diagram of proposed FPGA design.
CHAPTER 4. FPGA BOARD DESIGN FOR IGBT CONTROL AND DIAGNOSIS

- DDR2 SDRAM (Micron MT47H128M8CF-25).
- SPI PROM (N25Q128 1.8/3.3 V).
- USB to UART Bridge (CP2103).
- Two clock crystal oscillators 150MHz, 3.3 V (TXC 7W-150.000MBB-T OSC).
- Power Supplies 1 V/2.5 A, 1.8 V/1 A, 0.9 V/2.5 A, 3.3 V/1.5 A.
- JTAG.
- Two 2X50 pin 0.8 mm pitch board to board connectors (FX18-100S-0.8SH).
- Two leds.
- 2X9 pin header strip 2 mm pitch connector.
- 2X15 pin header strip 2 mm pitch connector.
- FPGA Reconfiguration push button switch.
- Power connector with switch and status led.

4.1.1 PC Layout of the Proposed FPGA Board

Figure 4.2 shows the printed circuit of the FPGA board (PCB). The number of layers used in the design is six as shown in Figure 4.3. The components are placed on the top and bottom sides. Plated Through Hole (PTH) are used to connect between the layers. The inner layers L3 and L4 are signal layers. They include the DDR2 signals (ADDR(0:13), DQ, DQS, control signals). Single-ended signals and differential pairs were also routed onto these inner layers.

In addition, polygon GND was used for shielding. The outer layer L2 is used as a reference plane (GND system), and it plays a significant role for EMI shielding. The outer layer L5 is used for the power distribution system (PDS). The polygon planes were used to achieve the required power nets which allow carrying heavy power supply currents for the FPGA device.

The power supplies of the FPGA device must not vary more than ±5% [44]. The voltage regulators VRs keep the power supplies constant. These VRs were placed onto the top side. They are placed near the FPGA device to reduce the losses. The polygon planes are provided. This design allows drawing a heavy current between layers into the FPGA device.

In addition, the bypass filters were used to reduce the noise in the current which can be supplied into the FPGA device.
Figure 4.2: Top and bottom view of the proposed FPGA board.

Figure 4.3: The layer stack-up for 6 layers used in the FPGA board.
Chapter 5

Stages Control Signals Generator Design

Figure 5.1 represents the schematic block of the SCS generator for one channel in the proposed IGBT gate driver. A Verilog code is created for this purpose. Six stages control signals are generated for one channel. Two up counters and two comparators are used to generate the required signals, as shown in Figure 5.2. The maximum count value of the counters is determined by the duty cycle of the PWM wave which is generated by the main controller. As can be seen in the Figure 5.2, when the PWM signal of the main controller has a rising edge, the stage control signal SCS_Q71 is asserted by the SCS generator and the first counter begins to count. The count value of the counter1 is compared with the delay time $t_{d1}$. When the count value is greater than the value of $t_{d1}$, the stage control signal SCS_Q72 is asserted, and the stage control signal SCS_Q73 is confirmed when the value of the counter1 is greater than the delay time $t_{d2}$. Accordingly, the external gate resistors are controlled by switching the stages transistors Q71, Q72, and Q73 in sequence with delay times $t_{d1}$ and $t_{d2}$.

On the other hand, the stage control signal SCS_Q81 is asserted and the counter2

1This channel can be upper or bottom channel for the proposed IGBT gate driver.
begins to increase, when the PWM signal of the main controller has falling edge. As a consequence, the stage control signal SCS_Q82 is asserted when the count value of the counter2 is greater than the $t_d3$ and the stage control signal SCS_Q83 is high when the count value of the counter2 is greater than the $t_d4$. This allows controlling the external gate resistors during the IGBT turn-off.

As long as the clock frequency of the SCS generator $f_{clk}$ is 100MHz, the time period $t_{clk}$ is

$$t_{clk} = \frac{1}{f_{clk}} = \frac{1}{100} = 10\text{ns}.$$  \hspace{1cm} (5.1)

Accordingly, the number of clock cycles, which is required to implement a delay time, could be calculated as follows

$$N_{CC} = \frac{\text{delaytime}}{t_{clk}}.$$  \hspace{1cm} (5.2)

Assuming that the IGBT switching frequency $f_{sw}$ is 5kHz, $t_{d1} = t_{d3} = 0.85\mu s$, and $t_{d2} = t_{d4} = 1.5\mu s$\(^2\). The number of clock cycles can be calculated as follows

$$N_{CC_{d1}} = \frac{0.85\cdot10^{-6}}{10\cdot10^{-9}} = 85\text{cycles}.$$

\(^2\)This is only an example,
\[ N_{CC,d2} = \frac{1.5 \cdot 10^{-6}}{10 \cdot 10^{-9}} = 150 \text{cycles}. \]

Figure 5.3 illustrates the stages of assertion of the stages control signals during the operation. The stages control signals of the transistors \(Q7_1, Q7_2\) and \(Q7_3\) are confirmed when the PWM signal is high, where the SCS\_Q72 is asserted after 85 cycles, and the SCS\_Q73 is confirmed after 150 cycles, as shown in Figure 5.3a. On the other hand, the stages control signals of the transistors \(Q8_1, Q8_2\) and \(Q8_3\) are asserted when the PWM signal is low, as shown in Figure 5.3b.

The \(En\) signal is asserted using an external switch which is de-bounced using digital circuits. Figure 5.4 shows all digital signals of the SCS generator and other parts during the operation.
5.1 Experimental Results

The schematic block shown in Figure 5.5 is an assembly of several designs which were tested on the proposed FPGA board. Verilog top level is used to interface to the blocks. This design is used to test the SCS generator. All the components of the design are built using the Verilog language. The structure of SCS generator was mentioned before. The other components are used to generate the PWM signal for testing. The main frequency is 150MHz, it is the input frequency of the clock wizard. The clock wizard generates two frequencies 100MHz and 5MHz. The first one is used by all components whereas the second one is used to control data by two external push buttons. As can be seen from Figure 5.5, the design is composed of inputs and outputs signals. The User Constraint File (UCF) is used to select the location of these signals\(^3\). Generally, ChipScope core is added to the design for monitoring the signals. Figure 5.6 illustrates the digital signals of the SCS generator which are monitored using ChipScope core. As can be seen from Figure 5.6, when the PWM signal has rising edge, the signals SCS\(_{Q71}\), SCS\(_{Q72}\), and SCS\(_{Q73}\) are confirmed sequentially, for controlling the IGBT gate resistors during the turn-on. On the other hand, when the PWM signal has falling edge, the signals SCS\(_{Q81}\), SCS\(_{Q82}\) and SCS\(_{Q83}\) are also asserted sequentially, for controlling the IGBT gate resistors during the turn-off.

Additionally, the power supplies of the IGBT gate driver FPGA and the internal temperature of the FPGA device can be monitored during the SCS generator operation. As can be seen from Figure 5.7, the current Die temperature of the FPGA device is always 37.5\(^{\circ}\)C, the current value of VCCIN and VCCBRAM are 0.996V, and the present value of VCCAUX is 1.796V. This means that all the values are in the acceptable range.

\(^3\)Xilinx PlanAhead software is used for this purpose.
Figure 5.5: Schematic block of the Verilog top level for testing
Figure 5.6: Monitoring of internal digital signals in the FPGA board using ChipScop core
Figure 5.7: Monitoring of powers supplies and Die temperature in the FPGA board during the SCS generator operation using ChipScop core
Chapter 6

Conclusion

The usage of Field Programmable Gate arrays (FPGAs) in industrial automation systems of factories are very wide. However, their usage are limited in the control applications and drive systems, and few research are concerned with the FPGAs usage in the diagnosis and fault detection. Therefore, the thesis is focused on the FPGAs usage in the fault diagnosis of inverter IGBT transistors during the switching process. A new IGBT gate driver architecture is developed to integrate the diagnostic functions. These functions allow analyzing the IGBT quantities $I_G$, $V_{GE}$ and $V_{CE}$ during the switching process. For this purpose, high speed parallel ADC converters are proposed. Multiple gate stages are designed for realization of variable gate resistance by sequential switching. Three parallel gate driver stages are used for one transistor in the power inverter. The usage of these parallel driver stages allows controlling the external IGBT gate resistors during the IGBT switching process. Driver interface to inverter control system with data exchange is designed, where the insulated SPI interface is used for this purpose.

FPGA board was designed and integrated to the IGBT gate driver. The FPGA device used in the design has two types of I/O Banks, high-performance (HP) and high-range (HR) I/O Banks. One of HP I/O Banks is used to interface a DDR2SDRAM memory to the FPGA device with a voltage 1.8 V. The HR I/O Banks are designed to support a range of I/O standards with voltages from 1.2 V to 3.3 V. These Banks are used to interface the high speed parallel ADCs of the IGBT gate driver to the FPGA device. The FPGA board includes differential signals and single signals which can be provided from board to board connectors. The proposed FPGA board supports two configuration modes: JTAG/boundary-scan configuration mode and Master Serial Peripheral Interface (SPI) flash configuration mode (x4). These modes are used to download the designed software on the FPGA device. Two clock sources are used to clocking the FPGA device. The clocks frequency is 150MHz. The FPGA device has also an integrated XADC which is composed of a dual 12 bit,1MSPS, ADCs. These ADCs can be configured to sample in continuous or event driven modes. Additionally, the XADC is used to monitor the power sources of FPGA banks and it can also be used to monitor the power system of the IGBT gate driver stages. An USB to UART bridge
device is used to interface the PC to the FPGA device. The FPGA board was tested and the signals outputs were proper.

In addition to control the IGBT transistor switching, the FPGA board acquires the data from the ADCs converters during the switching event, where the FPGA device contains all the DSP tools for analyzing and quantitative evaluation.

Multiple power supplies for IGBT gate stages and for FPGA feeding were designed. Two insulated DC/DC converters are used to feed the drive system, where regulators are used to adjust the DC/DC converters outputs.

The Stages Control Signals (SCS) were generated using Verilog code. The designed generator generates six signals which are synchronized with the PWM signal which is generated by the main controller of the drive system. The input frequency of the generator is 100 MHz. The clocking wizard which is provided by the IP cores of FPGA devices is used to generate the generator frequency from the external clock source. Global reset is used to reconfigure the entire software when an error occurs. Additionally, an enable signal is used to activate the generator. When the PWM signal has rising edge, three signals are generated sequentially with predefined delays\textsuperscript{1}, for controlling the gate driver stages during the IGBT transistor turn-on, and when the PWM signal has falling edge, three signals are also generated sequentially for controlling the gate driver stages during the IGBT transistor turn-off.

The SCS generator is designed to generate six signals for three gate driver stages. This gate driver can control one IGBT transistor switching during turn-on/off, but the capability of HDL language (Verilog, VHDL) allows building at least 12 SCS generators which can be used in the fault-tolerant applications or in another applications of industrial automation.

6.1 Future Work

The author of the doctoral thesis suggests to explore the following:

- It would be interesting to develop the IGBT gate driver with integrated diagnostic functions to include three phase inverter with diagnosis and fault-tolerant control.

- It would be important to develop the FPGA board to include differential clock source which accelerates the speed of analyzing during the process.

- The implementation of mentioned steps above, requires the development of software to interface the inverter with drivers FPGAs to the main controller.

\textsuperscript{1}These delays can be set in accordance to the requirements of used IGBT.


## Curriculum Vitae

**Ing. Ziad Nouman**

<table>
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<tr>
<th>Phone</th>
<th>00420773260963</th>
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<tr>
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### ACADEMIC EDUCATION

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<th>Since</th>
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<tbody>
<tr>
<td>2010</td>
<td>Brno University of Technology – Czech Republic</td>
<td>Ph.D. student</td>
</tr>
</tbody>
</table>
| 2004 – 2005 | Tishreen University - Lattakia | Higher Study Diploma in Electrical Engineering  
The field of (electrical power systems) |
| 2000 – 2004 | Tishreen University - Lattakia | Degree of Electrical Engineer.  
Section of Power Engineering. |
| 1998 - 2000 | Industrial Institute of Electricity and Mechanics – Damascus | |

### LANGUAGES

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<td>English</td>
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### SPECIAL KNOWLEDGE

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</tr>
<tr>
<td>Languages of Programming</td>
<td>C, HDL (Verilog, VHDL), Matlab.</td>
</tr>
<tr>
<td>Software of Design</td>
<td>Altium Designer, Cadence, Microcontroller Design, FPGA Design.</td>
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### PLACES OF INTEREST

Reading, Sport, learning languages, Tourism
Abstract

This doctoral thesis deals with the usage of Field Programmable Gate Arrays (FPGAs) in a diagnosis of power inverters which use the IGBTs transistors as switching devices. It is focused on the IGBT gate drives and their structures. As long as the transient phenomena and other quantities such as $I_G$, $V_{GE}$, $V_{CE}$ shows the IGBT degradation during the switching process (turn-on, turn-off), a new IGBT gate driver architecture is proposed for measuring and monitoring these quantities. Quick measurements and monitoring during the IGBT switching process require high sampling frequencies. Therefore, high speed parallel ADC converters (> 50MSPS) are proposed.

The thesis is focused on the FPGA design (hardware, software). A new FPGA board is designed for desired functions implementation such as IGBT driving using multiple stages, IGBT monitoring and diagnosis, and interfacing to inverter controller.

Abstrakt

Tato disertační práce se zabývá využitím programovatelných hradlových polí (FPGA) v diagnostice měničů, využívajících spínaných IGBT tranzistorů. Je zaměřena na budoucí těchto výkonových tranzistorů a jejich struktury. Přechodné jevy veličin, jako jsou $I_G$, $V_{GE}$, $V_{CE}$ během procesu přepínání (zapnutí, vypnutí), mohou poukazovat na degradaci IGBT. Pro měření a monitorování těchto veličin byla navržena nová architektura budiče IGBT. Rychlé měření a monitorování během přepínacího děje vyžaduje vysokou vzorkovací frekvenci. Proto jsou navrhovány paralelní vysokorychlostní AD převodníky (> 50MSPS).

Práce je zaměřena převážně na návrh zařízení s FPGA včetně hardware a software. Byla navržena nová deska plošných spojů s FPGA, která plní požadované funkce, jako je řízení IGBT pomocí vícenásobných paralelních koncových stupňů, monitorování a diagnostiku, a propojení s řídící jednotkou měniče.