FGMOS Based Voltage-Controlled Grounded Resistor

Rishikesh PANDEY[1], Maneesha GUPTA[2]

[1]Dept. of Electronics and Communication Engineering, Thapar University, Patiala, Punjab-147004, India
[2]Dept. of Electronics and Communication Engineering, Netaji Subhas Institute of Technology, New Delhi-110078, India

riship23@gmail.com, maneeshapub@gmail.com

Abstract. *This paper proposes a new floating gate MOSFET (FGMOS) based voltage-controlled grounded resistor. In the proposed circuit FGMOS operating in the ohmic region is linearized by another conventional MOSFET operating in the saturation region. The major advantages of FGMOS based voltage-controlled grounded resistor (FGVCGR) are simplicity, low total harmonic distortion (THD), and low power consumption. A simple application of this FGVCGR as a tunable high-pass filter is also suggested. The proposed circuits operate at the supply voltages of ±0.75 V. The circuits are designed and simulated using SPICE in 0.25-μm CMOS technology. The simulation results of FGVCGR demonstrate a THD of 0.28% for the input signal 0.32 V_{pp} at 45 kHz, and a maximum power consumption of 254 μW.*

Keywords

Floating gate MOSFETs, low-voltage, voltage-controlled grounded resistor, SPICE.

1. Introduction

Lowering power supply voltage is the most efficient method to reduce power dissipation and raise system reliability. Some of the low voltage techniques used to reduce supply voltages are level shifters, self-cascode MOSFETs, sub-threshold MOSFETs, bulk-driven MOSFETs, and floating gate MOSFETs (FGMOS) [1], [2]. Out of these FGMOS presents a unique advantage of programmability of threshold voltage, which can be lowered from its conventional value, thus makes it suitable for low voltage applications [3], [4]. FGMOS is compatible with standard double-poly CMOS process technology and has been used to develop digital-to-analog (D/A) and analog-to-digital (A/D) converters [5], resistors [6]-[9], electronic programming [10], neural networks [11], and operational transconductance amplifier [12], etc. Motivated by the unique characteristics of the FGMOS, a FGVCGR is presented in this paper.

The voltage-controlled resistors find applications in the area of analog signal processing such as filters [13-15], oscillators [16], [17], and amplifiers [18], etc. The paper presents FGVCGR and its simple application as tunable high-pass filter operating at supply voltage of ±0.75 V. The operations of the proposed circuits have been simulated using SPICE in 0.25-μm CMOS technology.

2. Operation of FGMOS

A cross section of a typical *n*-channel, *N*-input FGMOS is shown in Fig. 1. The FGMOS differs from a conventional MOSFET in that it has one more gate called the floating gate, which is completely isolated within the oxide.

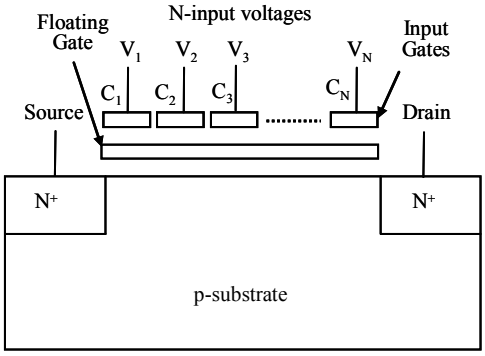


Fig. 1. Structure of an *N*-input FGMOS.

The voltage on the floating gate V_{FG} of Fig. 1 is expressed as [19]:

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i + C_{fd} V_{DS} + C_{fs} V_{SS} + C_{fb} V_{BS} + Q_{FG}}{C_T} \quad (1)$$

and the total capacitance C_T of the floating-gate is

$$C_T = \sum_{i=1}^{N} C_i + C_{fd} + C_{fs} + C_{fb} \quad (2)$$

where C_1, C_2, C_3, ….. , C_N are the input capacitances between control gate and floating gate, $\sum_{i=1}^{N} C_i$ is the sum of *N*-input capacitances, C_{fd} is the overlap capacitance between floating-gate and drain, C_{fs} is the overlap capacitance between floating-gate and source, C_{fb} is the parasitic capacitance between floating gate and substrate, V_i is the input voltage at the i^{th} input gate, V_{DS} is the drain-to-source voltage, V_{SS} is the source voltage, V_{BS} is the

substrate-to-source voltage, C_T is the total capacitance of the floating-gate and Q_{FG} is the residual charge which can be neglected during the fabrication process using the method suggested in [20]. Therefore equation (1) reduces to:

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i + C_{fd} V_{DS} + C_{fs} V_{SS} + C_{fb} V_{BS}}{C_T}. \quad (3)$$

If $\sum_{i=1}^{N} C_i >> C_{fd}$, C_{fs}, C_{fb}, then equations (2) and (3) are modified as $C_T = \sum_{i=1}^{N} C_i$, and $V_{FG} = \sum_{i=1}^{N} C_i V_i / C_T$.

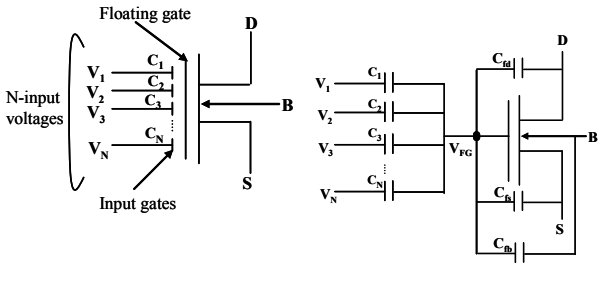
The drain current equations for the *n*-channel FGMOS have been obtained by modifying the conventional *n*-channel MOSFET equations. The drain currents I^{o}_{DS} and I^{S}_{DS} in the ohmic and saturation region respectively, are:

$$I_{DS}^{o} = K_n \left\{ \left[\left(\frac{\sum_{i=1}^{N} C_i V_i}{C_T} \right) - V_{SS} - V_T \right] V_{DS} - \frac{1}{2} V_{DS}^2 \right\}, \quad (4)$$

$$I_{DS}^{S} = \frac{K_n}{2} \left\{ \left(\frac{\sum_{i=1}^{N} C_i V_i}{C_T} \right) - V_{SS} - V_T \right\}^2 \quad (5)$$

where $K_n = \mu_n C_{ox} (W/L)$ is the transconductance parameter, μ_n is the electron mobility, C_{ox} is the gate-oxide capacitance per unit area, (W/L) is the aspect ratio of the transistor, and V_T is the threshold voltage of FGMOS. The symbol and equivalent circuit model for an *N*-input FGMOS are shown in Figs. 2(a) and (b) respectively, where V_i (for $i = 1, 2, \ldots, N$) are the control inputs and D, S and B are the drain, source and substrate, respectively.

3. Proposed Voltage-Controlled Grounded Resistor



(a) (b)

Fig. 2. FGMOS: (a) Symbol. (b) Equivalent circuit model.

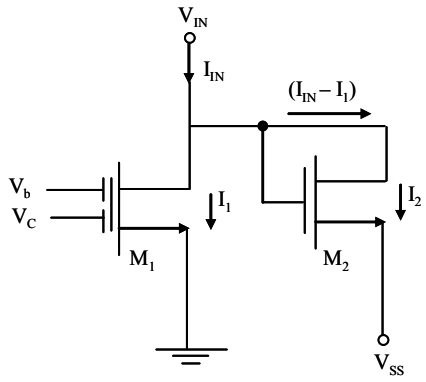


Fig. 3. Voltage- controlled grounded resistor.

In Fig. 3 the transistors M_1 and M_2 are connected in parallel where M_1 and M_2 are operating in the ohmic and saturation region respectively. Using (4), we can express the drain currents I_1 as:

$$I_1 = K_{n1} \left\{ \left[k_{11}(V_b - V_{SS}) + k_{12}(V_C - V_{SS}) - V_{Tn1} \right] V_{IN} - \frac{V_{IN}^2}{2} \right\}. \quad (6)$$

The drain current I_2 is given as:

$$I_2 = \frac{K_{n2}}{2} (V_{IN} - V_{SS} - V_{Tn2})^2 \quad (7)$$

where V_{IN} in the input voltage, K_{n1} and K_{n2} are the transconductance parameters, V_{Tn1} and V_{Tn2} are the threshold voltages of the transistors M_1 and M_2 and $k_{11} = C_1/C_T$, $k_{12} = C_2/C_T$ are the capacitive coupling ratios of the transistor M_1. From Fig. 3, it can be seen that the input current of the circuit is the sum of both drain currents I_1 and I_2, i.e.

$$I_{IN} = I_1 + I_2 . \quad (8)$$

By choosing $K_{n1} = K_{n2}$ in (8), the squared terms of input voltage V_{IN} is cancelled out, (since $k_{11} + k_{12} = 1$) and we get:

$$I_{IN} = K_{n1} V_{IN} \left[(k_{11} V_b + k_{12} V_C - V_{Tn1}) - (V_{SS} + V_{Tn2}) \right] + I_{offset} \quad (9)$$

where $I_{offset} = (V_{SS} + V_{Tn2})^2$. From (9), it is observed that a linear relationship can be obtained if I_{offset} is eliminated from the equation. Fig. 4 shows the proposed FGVCGR in which the offset component is eliminated by adding another transistor M_3 (perfectly matched with M_2 i.e. $K_{n2} = K_{n3}$, $V_{Tn2} = V_{Tn3}$) and a simple current mirror formed by the transistors M_4 and M_5 to the circuit shown in Fig.3.

Hence, the simulated resistance from (9) is

$$R_{equ} = V_{IN} / I_{IN} = \left\{ K_{n1} \left[(k_{11} V_b + k_{12} V_C - V_{Tn1}) - (V_{SS} + V_{Tn2}) \right] \right\}^{-1} \quad (10)$$

From (10), it can be seen that the proposed circuit behaves as voltage-controlled grounded resistor and the value of the equivalent resistance R_{equ} is tuned by control voltage V_C. The input voltage range for the transistor M_1 to

operate in the ohmic region may be derived as $0 \le V_{IN} < (k_{11}V_b + k_{12}V_C - V_{Tn1})$.

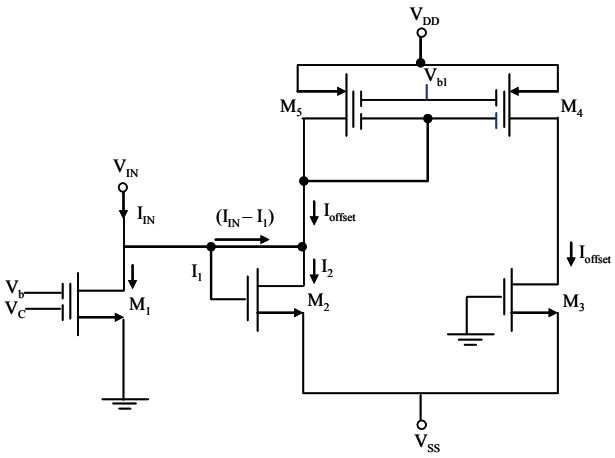


Fig. 4. Proposed voltage-controlled grounded resistor (FGVCGR).

4. Proposed Tunable High-Pass Filter

The proposed FGVCGR can be used in communication systems and analog signal processing applications. However in this paper we have used it for the realization of tunable high-pass filter shown in Fig. 5.

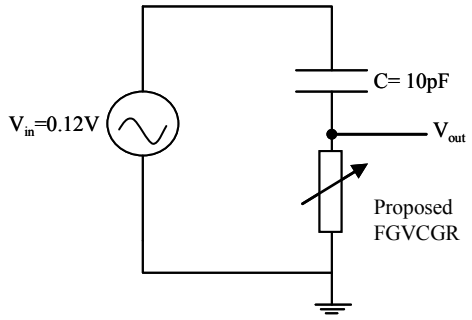


Fig. 5. Proposed tunable high-pass filter.

5. Simulation Results

All the proposed circuits have been simulated using SPICE in 0.25-μm CMOS technology. The SPICE model parameters and the aspect ratios are listed in Tab. 1 and 2 respectively. Fig. 6 shows the current/voltage characteristics of the proposed FGVCGR for $V_C = 0.75$ V while V_{IN} varies from 0 V to 0.32 V. Tab. 3 shows the equivalent resistance for various values of control voltage V_C. The simulation results are consistent with the theoretical results calculated by (10). The calculated error was found to be less than ±2%. The distortion analysis of the proposed FGVCGR has been performed and the total harmonic distortion (THD) was found to be 0.28% (for the input signal 0.32 V_{pp} at 45 kHz). Tab. 4 shows a comparison of the various parameters of the FGVCGR proposed in this paper with those of the voltage-controlled grounded resistor reported in [13] and [15]. The total power dissipation of the proposed FGVCGR is 0.254 mW. Fig. 7 shows the frequency response of the proposed tunable high-pass filter.

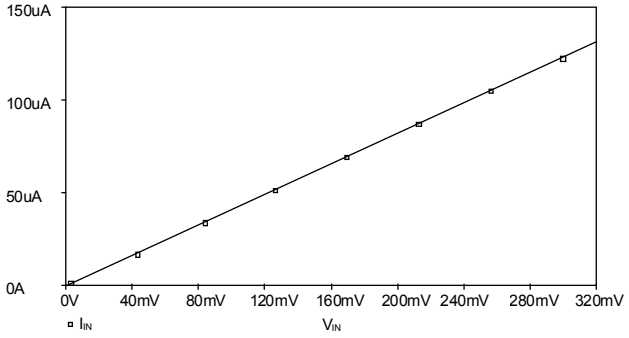


Fig. 6. I-V characteristics of the proposed FGVCGR.

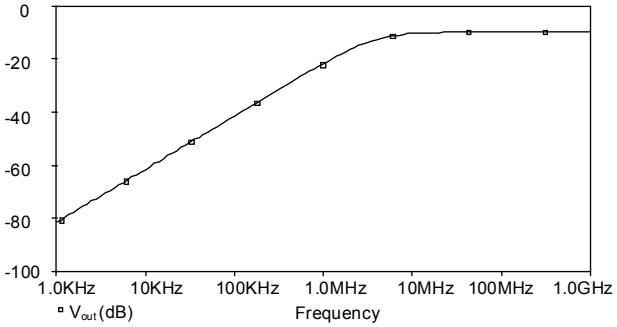


Fig. 7. Frequency response of proposed tunable high-pass filter.

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.MODEL CMOSN NMOS (                    LEVEL  = 3
+ TOX   = 5.7E-9       NSUB  = 1E17    GAMMA =        +
0.4317311    PHI   = 0.7   VTO   = 0.4238252   DELTA = 0
+ UO    = 425.6466519  ETA   = 0   THETA = 0.1754054
+ KP    = 2.501048E-4  VMAX  = 8.287851E4  KAPPA =  +
0.1686779  RSH   = 4.062439E-3  NFS   = 1E12  TPG   = 1
+ XJ    = 3E-7  LD    = 3.162278E-11  WD    = 1.232881E-8
+ CGDO  = 6.2E-10      CGSO  = 6.2E-10   CGBO  = 1E-10
+ CJ    = 1.81211E-3   PB    = 0.5       MJ    = 0.3282553
+ CJSW  = 5.341337E-10  MJSW  = 0.5)

.MODEL CMOSP PMOS (                    LEVEL  = 3
+ TOX   = 5.7E-9   NSUB  = 1E17    GAMMA = 0.6348369
+ PHI   = 0.7      VTO   = -0.5536085   DELTA = 0
+ UO    = 250      ETA   = 0       THETA = 0.1573195
+ KP    = 5.194153E-5  VMAX  = 2.295325E5          +
KAPPA = 0.7448494  RSH   = 30.0776952   NFS   = 1E12
+ TPG   = -1   XJ    = 2E-7    LD    = 9.968346E-13
+ WD    = 5.475113E-9  CGDO  = 6.66E-10  GSO   = 6.66E-10
+ CGBO  = 1E-10 CJ    = 1.893569E-3   PB    = 0.9906013  +
MJ    = 0.4664287 CJSW  = 3.625544E-10  MJSW  = 0.5)
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Tab. 1. SPICE Model parameters of 0.25-μm CMOS technology.

M_1	M_2 and M_3	M_4 and M_5
8Δ: 2 Δ	8Δ: 2 Δ	40Δ: 2 Δ

Tab. 2. W/L ratio of the transistors used in FGVCGR (Δ = 0.25 μm).

V_C (Volts)	R_{equ} (KΩ) Simulation results	R_{equ} (KΩ) Theoretical results	% Error (±)
0.10	4.020	4.077	-1.39
0.20	3.507	3.537	-0.84
0.30	3.173	3.122	1.63
0.40	2.835	2.795	1.43
0.50	2.548	2.530	0.71
0.60	2.318	2.310	0.35
0.70	2.127	2.126	0.05
0.75	2.045	2.044	0.04

Tab. 3. Equivalent resistance for different values of V_C.

Proposed voltage-controlled grounded resistor	Voltage-controlled grounded resistor suggested in [13]	Voltage-controlled grounded resistor suggested in [15]
Supply Voltages V_{DD}=V_{SS}= 0.75V	Supply Voltages V_{DD}=V_{SS}=5V	Supply Voltages V_{DD}=V_{SS}=5V
Power Dissipation = 0.254mW	--	--
Calculated error is less than 2 %	Error is 0.6%	--
THD is 0.28% for input signals of 0.32V_{PP}	--	THD is 0.4% for input signals of 1V_{PP} and 1% for input signals of 4V_{PP}

Tab. 4. Comparison between different circuits.

6. Conclusions

A simple voltage-controlled grounded resistor (FGVCGR) is proposed that incorporates an effective cancellation of the nonlinearity of the I_{DS}-V_{DS} characteristics of the FGMOS. This FGVCGR has wide input range, low power dissipation and fairly low THD. A simple application as tunable high-pass filter is also presented. The simulation results validate the effectiveness of the proposed circuits and these circuits are expected to be useful in low voltage analog circuits.

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About Authors ...

Rishikesh PANDEY (1977) received his M.Sc. (Electronics) degree at D.D.U. Gorakhpur University,

Gorakhpur in 2000 and M. Tech. (Electronics Design & Technology) at U.P. Technical University in 2003. He was Lecturer in Electronics & Communication Engineering Department at B.I.T. Muzaffarnagar from 2003 to 2004, and College of Engineering & Technology, Moradabad from 2004 to 2007. From 2007 to June 2009, he was working as Assistant Professor at College of Engineering & Technology, Moradabad and was on leave from August 2006 to June 2009 for pursuing Ph. D. at Netaji Subhas Institute of Technology, New Delhi. Presently he is working as Assistant Professor at Thapar University, Patiala. His teaching and research interests are in the areas of Analog & Digital Signal Processing, VLSI design, Analog & Digital Integrated Circuits, and Microprocessors.

Maneesha GUPTA (1960) received her B.E. (Electronics & Communication Engineering) degree in 1981, M.E. (Electronics & Communication Engineering) degree in 1983, both at Government Engineering College, Jabalpur, and Ph.D. (Electronics Engg. - Analysis, Synthesis & Applications of Switched Capacitor Circuits) at Indian Institute of Technology, Delhi in 1990. She is currently working as Assistant Professor in Electronics & Communication Engineering (ECE) Department of Netaji Subhas Institute of Technology, New Delhi. Her teaching and research interests are Switched Capacitors Circuits and Analog Signal processing. She has co-authored over 20 research papers in the above areas in various international/national journals and conferences.