DVCCs Based High Input Impedance Voltage-Mode First-Order Allpass, Highpass and Lowpass Filters Employing Grounded Capacitor and Resistor

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Abstract. *A voltage-mode high input impedance first-order allpass, highpass and lowpass filters using two differential voltage current conveyors (DVCCs), one grounded capacitor and one grounded resistor is presented. The allpass, highpass and lowpass allpass signals can be obtained simultaneously from the circuit configuration. The suggested filter uses a canonical number of passive components without requiring any component matching condition. The simulation results confirm the theoretical analysis.*

Keywords

Current conveyors, first-order, allpass filter, analog circuit design.

1. Introduction

Current conveyors (CCs) are receiving much attention for their potential advantages such as inherent wider signal bandwidths, simpler circuitry and larger dynamic range. Voltage-mode active filters with high input impedance are of great interest because they can be directly connected in cascade to implement higher order filters [1]-[2]. Besides the use of only grounded capacitor and resistor they are beneficial from the point of view of integrated circuit fabrications [3], [4]. Several voltage-mode first-order allpass filters using various active components have been reported. Some circuits use two second-generation current conveyors (CCIIs) to realize such a first-order allpass filter function with high input impedance [5], [6]. However, the passive components they used are not canonical. Some circuits use one CCII and three or more passive components [7]-[10]. However, the passive components they used are not all grounded. Some circuits use one CCII, one grounded capacitor and two or three resistors [11], [12]. However, these circuits have not the advantage of high input impedance. Ibrahim et al. [13] and Horng et al. [14] each proposed one voltage-mode first-order allpass filters using one differential difference current conveyor (DDCC), one capacitor and one resistor. However, these circuits still have not the advantage of high input impedance. In 2004, Ibrahim et al. proposed four first-order allpass filter circuits using inverting-type second-generation current conveyors (ICCIIs) [15]. However, the capacitors they used are not grounded. In 2006, Chen and Wu proposed a first-order allpass filter using one DDCC, one resistor and one grounded capacitor [16]. However, the input impedance is low. Two first-order allpass filters each using one operational transconductance amplifier, one unity gain differential amplifier and one grounded capacitor with high input impedance were presented in [17], [18]. However, only allpass filter can be obtained in the circuit configuration. Several current differencing buffered amplifier based first-order allpass filters were presented in [19]-[21]. However, the capacitors they used are not all grounded.

Differential voltage current conveyor (DVCC) was introduced in [22]. The applications using DVCCs as active elements have received considerable attention [23]-[26]. Several high input impedance voltage-mode first-order allpass filters with grounded passive components using two DVCCs were presented in [24], [25]. However, the passive components they used are not canonical. Moreover, passive components matching conditions are required in the realizations. In 2010, Minaei and Yuce present a first-order allpass filter using two DVCCs, one floating resistor and one grounded capacitor [26]. However, the resistor used is floating.

In this paper, a new voltage-mode first-order allpass filter using two DVCCs, one grounded capacitor and one grounded resistor is presented. The first-order allpass, highpass and lowpass filters can be simultaneously obtained from the circuit configuration. The proposed circuit has the advantages of high input impedance and without requiring any element matching condition.

2. Proposed Circuit

The DVCC [22], [27] can be characterized by the following matrix equation:

$$\begin{bmatrix} i_{y1} \\ i_{y2} \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_{y1} \\ v_{y2} \\ i_x \\ v_z \end{bmatrix} \tag{1}$$

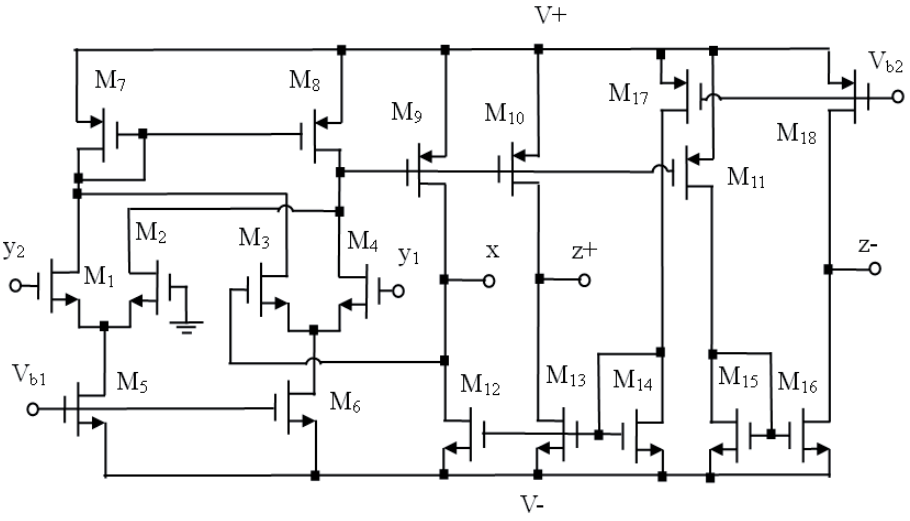

Fig. 1. CMOS realization of the DVCC [27].

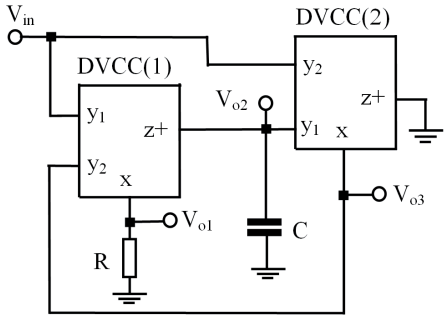

Fig. 2. The proposed DVCCs based first-order filters.

The CMOS implementation of DVCC is shown in Fig. 1, which is obtained from Fig. 5 of [27]. The proposed voltage-mode first-order highpass, lowpass and allpass filters using two plus-type DVCCs, one grounded capacitor and one grounded resistor is shown in Fig. 2. The voltage transfer functions can be expressed as

$$\frac{V_{o1}}{V_{in}} = \frac{2sC}{sC+G}, \tag{2}$$

$$\frac{V_{o2}}{V_{in}} = \frac{2G}{sC+G}, \tag{3}$$

$$\frac{V_{o3}}{V_{in}} = \frac{-sC+G}{sC+G}. \tag{4}$$

From (2)-(4) it can be seen that a first-order highpass response is obtained from V_{o1}, a first-order lowpass response is obtained from V_{o2}, and a first-order allpass response is obtained from V_{o3}. Because the input terminal of the proposed first-order allpass filter is connected directly to the y terminals of the DVCCs, the input terminal has the advantage of high input impedance. Because the V_{o3} output terminal is taken from the x terminal of the second DVCC and the z+ terminal of the second DVCC is grounded, the V_{o3} output terminal has the advantage of low output impedance. Voltage followers may be needed at the V_{o1} and V_{o2} output terminals of the proposed circuit to buffer the outputs and avoid the effects of load capacitances or resistances changing the responses of the filters.

3. Non-Ideality Analysis of the DVCCs

Taking into consideration the DVCC non-idealities, the port relations in (1) can be expressed as

$$v_x = \beta_1 v_{y1} - \beta_2 v_{y2} \text{ and } i_z = \pm\alpha i_x \tag{5}$$

where $\beta_j = 1 - \varepsilon_{vj}$ and $\alpha = 1 - \varepsilon_i$ for j = 1, 2, where ε_{vj} ($|\varepsilon_{vj}| << 1$) denotes the voltage tracking errors of the DVCC and ε_i ($|\varepsilon_i| << 1$) denotes the current tracking error from the x terminal to the z terminal of the DVCC. Re-analysis of the filter circuit in Fig. 2 yields the following modified transfer functions:

$$\frac{V_{o1}}{V_{in}} = \frac{sC(\beta_{11}+\beta_{12}\beta_{22})}{sC+G\alpha_1\beta_{12}\beta_{21}}, \tag{6}$$

$$\frac{V_{o2}}{V_{in}} = \frac{G\alpha_1(\beta_{11}+\beta_{12}\beta_{22})}{sC+G\alpha_1\beta_{12}\beta_{21}}, \tag{7}$$

$$\frac{V_{o3}}{V_{in}} = \frac{-sC\beta_{22}+G\alpha_1\beta_{11}\beta_{21}}{sC+G\alpha_1\beta_{12}\beta_{21}}. \tag{8}$$

The cutoff frequency is obtained by

$$\omega_c = \frac{\alpha_1\beta_{12}\beta_{21}}{CR}. \tag{9}$$

The active and passive sensitivities are low and obtained as $S_{C,R}^{\omega_c} = -1$; $S_{\alpha_1,\beta_{12},\beta_{21}}^{\omega_c} = 1$.

4. Influence of Parasitic Elements

A non-ideal DVCC model is shown in Fig. 3 [4]. It is shown that the real DVCC has parasitic resistors and ca-

pacitors from the *y* and *z* terminals to the ground, and also, a series resistor at the input terminal *x*. Taking into account the non-ideal DVCCs and assuming the circuits are working at frequencies much lower than the corner frequencies of $\alpha(s)$ and $\beta_k(s)$, namely, $\alpha \approx \beta_k \approx 1$.

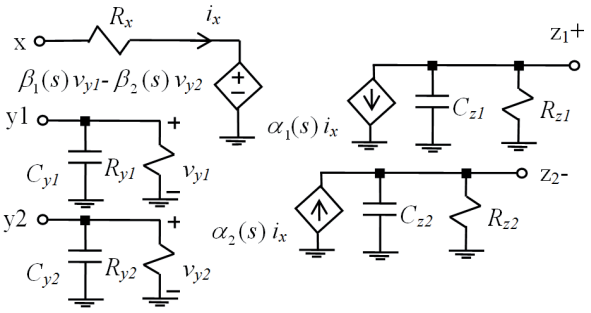

Fig. 3. The non-ideal DVCC model [4].

The transfer functions of Fig. 2 become

$$\frac{V_{o1}}{V_{in}} = \frac{+G_a(2G_{x2}+G_{y12})}{\begin{array}{l}s^2C'C_{y12}+s[C'(2G_{x2}+G_{y12})+C_{y12}G_a]\\ +G'G_{x2}+G_a(G_{x2}+G_{y12})\end{array}} * \frac{R}{R+R_{x1}}, \quad (10)$$

$$\frac{V_{o2}}{V_{in}} = \frac{sC_{y12}G'+G'(2G_{x2}+G_{y12})}{\begin{array}{l}s^2C'C_{y12}+s[C'(G_{x2}+G_{y12})+C_{y12}G_a]\\ +G'G_{x2}+G_a(G_{x2}+G_{y12})\end{array}}, \quad (11)$$

$$\frac{V_{o3}}{V_{in}} = \frac{-sC'G_{x2}+G'G_{x2}-G_aG_{x2}}{\begin{array}{l}s^2C'C_{y12}+s[C'(G_{x2}+G_{y12})+C_{y12}G_a]\\ +G'G_{x2}+G_a(G_{x2}+G_{y12})\end{array}}, \quad (12)$$

where $C' = C + C_{y21} + C_{z1}$, $R' = R + R_{x1}$, $G_a = G_{y21} + G_{z1}$.

In equations (10) to (12), undesirable factors are yielded by the non-idealities of the DVCCs. The effect of capacitance C_{y12} becomes non-negligible at very high frequencies, the conductance G_a becomes non-negligible at very low frequencies. To minimize the effects of the DVCCIIs' non-idealities, the operation angular frequency should restricted to the following conditions

$$\omega << \min\left\{\frac{2G_{x2}+G_{y12}}{C_{y12}}, \sqrt{\frac{G'G_{x2}+G_a(G_{x2}+G_{y12})}{C'C_{y12}}}, \frac{C'(2G_{x2}+G_{y12})+C_{y12}G_a}{C'C_{y12}}\right\} \quad (13)$$

$$\omega >> \frac{G_a(2G_{x2}+G_{y12})}{C'(2G_{x2}+G_{y12})+C_{y12}G_a}. \quad (14)$$

5. Simulation Results

HSPICE simulations were carried out to demonstrate the feasibility of the proposed circuit in Fig. 2 using 0.18 μm, level 49 MOSFET from TSMC. The model parameters are given in [28]. The DVCC was realized by the CMOS implementation in Fig. 1 with the NMOS and PMOS transistor aspect ratios *W/L*=4.5u/0.9u and *W/L*=9u/0.9u, respectively.

Fig. 4(a), (b) and (c) represent the magnitude and phase responses of the first-order highpass, lowpass and allpass filters, respectively, designed with f_c =397.89 kHz: C = 80 pF and R = 5 kΩ. The power supply was ± 1.25 V. The bias voltages are V_{b1} = -0.53 V and V_{b2} = 0.53 V. The DVCC has parasitic resistor from the *z* terminal to the ground (R_z [4]). When the *z* terminal load of the DVCC is a capacitor (C), it introduces a pole produced by R_z and C at low frequency. This can explain why Fig. 4(a) has non-ideal phase responses at low frequencies. This effect can be minimized by using larger loading capacitor or operating the filter in high frequencies.

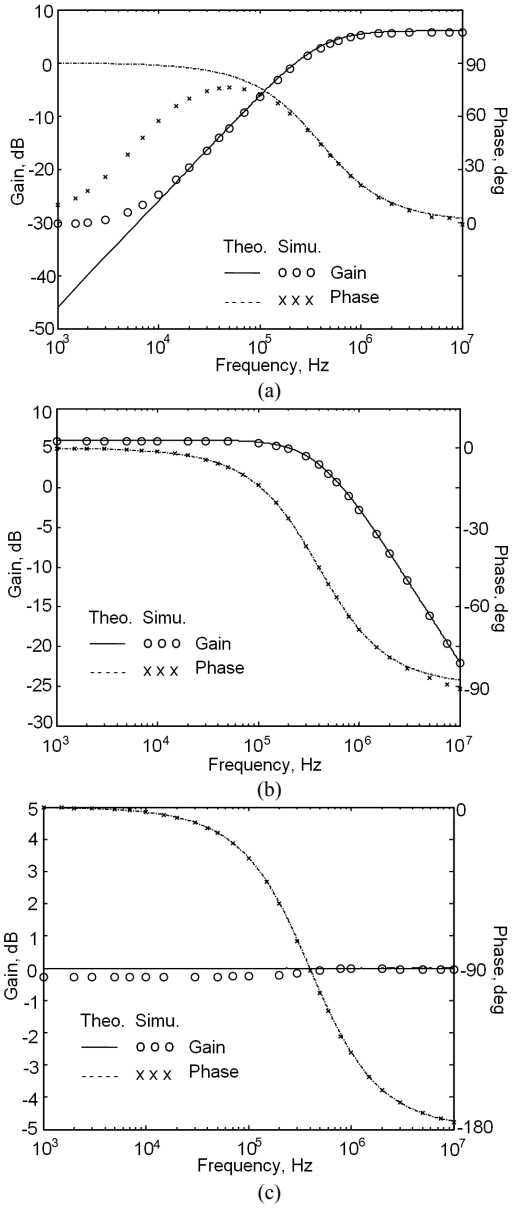

Fig. 4. Simulation results of the proposed circuit. (a) Highpass filter; (b) Lowpass filter; (c) Allpass.

6. Conclusions

A new voltage-mode first-order filter configuration using two DVCCs, one grounded capacitor and one grounded resistor is presented. The first-order allpass, highpass and lowpass filters can be simultaneously obtained from the same circuit configuration. The proposed circuit has the advantages of high input impedance, using grounded passive components and without requiring any element matching condition.

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