An Ultra-Low-Voltage and Ultra-Low-Power 2.4 GHz LNA Design

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Abstract. *In this paper, ultra-low-voltage and ultra-low-power circuit techniques are presented for CMOS RF front-ends. By employing a modified current-reused architecture, the low-noise amplifier (LNA) can operate at a very low supply voltage with microwatt power consumption while maintaining reasonable circuit performance at 2.4 GHz. Using a TSMC 0.18 um CMOS process, from the simulation results, the fully integrated LNA exhibits a gain of 14.4 dB and a noise figure of 1.6 dB at 2.4 GHz, operated at a supply voltage of 0.9 V, the input matching (S11) is –18.1 dB while consumes only 960 μW. example.*

Keywords

Low-noise amplifier, low power, low voltage, low noise.

1. Introduction

The increasing demands upon portable wireless devices have motivated the development of CMOS radio frequency integrated circuits (RFIC). These devices require low power dissipation to maximize battery lifetime. Some low power applications, such as wireless medical telemetry, require the portable devices to operate at low supply voltage with a small battery or environment energy, so the power and supply voltage constriction is a crucial issue for these designs [7]. Being the first stage of the receiver, the design of a low noise amplifier (LNA) involves a trade-off between several goals. These include providing a stable 50 Ohms input impedance to the output of the filter following the antenna, minimizing the noise figure and supplying gain that must be high enough to lower the noise contribution of the following blocks without degrading linearity. Further-more, in portable systems, the power and supply voltage constraint makes such optimization more complicated.

The low-voltage and current-reused design is an effective method to decrease the power consumption. Several low-power LNA designs [1]-[13] have been reported. A cascode amplifier is widely used for the LNA designs [1]-[6]. With the current-reused topology, the desirable gain can be achieved with relatively low current consumption. However, due to the use of a stack of multi-transistors, it increases the required supply voltage, which is not suitable for low supply voltage operation. In order to lower the supply voltage, a folded topology has been proposed [7], [8]. The required supply voltage is reduced by one transistor compared with that of the cascade amplifiers. Unfortunately, the total current consumption of the CMOS LNA may not be minimized as there is more than one gain stage. For the low voltage and low power applications, a current-reused two-stage common source topology has been proposed for the RF front-end circuits [9]-[13]. It can provide sufficient gain while the supply voltage and power consumption is low, but the noise is slightly higher. To address the above mentioned problems, we present a modified current-reused two-stage common source topology in this paper. Compared to the previously presented current-reused two-stage common source topologies, we mainly modify the input matching circuit architecture for better noise figure and gain, as shown in Fig. 1. This LNA topology will be demonstrated in the following to have 1.6 dB NF (noise figure) and extremely high FOM (figure of merit).

This paper is organized as follows. The matching methods and the circuit topology are discussed in Sec. 2, and their effect on the gain and NF of the LNA is also presented in Sec. 2. Sec. 3 presents the simulation results of the LNA, which is followed by the conclusion.

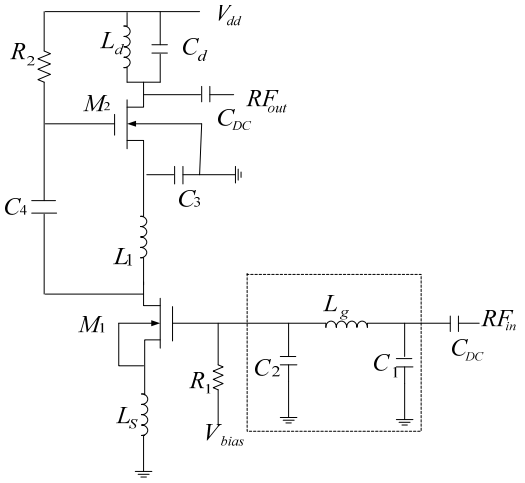


Fig. 1. Complete circuit schematic of the proposed LNA.

2. Circuit Implementation

2.1 LNA Topology

The passive network located before the LNA for power matching purposes plays an important role in the overall performance of the circuit in terms of gain, noise figure, and linearity [17]. The source inductive de-generation matching method is widely used, as shown in Fig. 2(a). For this matching topology, power and noise mat-ching cannot be done simultaneously with low current bias, thus the noise figure could potentially be high for low power applications. To address the problems above, we use a modified input matching topology in this paper, as shown in Fig. 2(b), with the addition of capacitors to the gate node of the input transistor. When designing a LNA with a fixed current consumption, we can decrease L_s to improve the voltage gain and lower NF, while adjusting L_g, C_1 and C_2 to maintain the input matching. Therefore, in this paper a modified current-reused two-stage common source topology with this matching network is presented, as shown in Fig. 1.

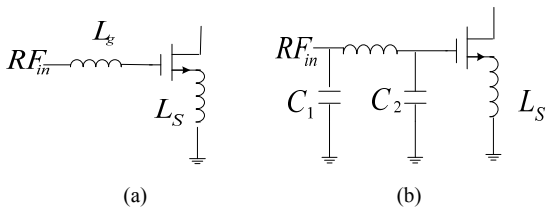


Fig. 2. (a) Conventional input matching topology. (b) The modified input matching topology.

In Fig. 1, the common-source MOS transistors M_1 and M_2 represent the first and the second stage, respectively. They share the same DC bias current flowing through L_1 to reduce the power consumption. The amplified RF signal from M_1 is directed to the gate node of M_2 through the coupling capacitor C_4. The capacitor C_3 is presented as a RF bypass capacitor for M_2. The capacitor C_{DC} at input and output is used as a DC blocking capacitor. In order to ob-tain simultaneous power and noise matching for the input stage, L_g, C_1, C_2 and the inductive source degeneration L_s are adopted. On the other hand, output matching is pro-vided by L_d and C_d. The LC network L_1 - C_4 between the gain stages is used for inter-stage matching.

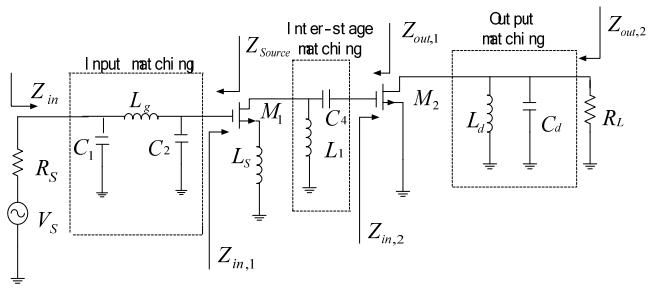


Fig. 3. Circuit schematic of an equivalent two-stage cascaded amplifier.

Note that the proposed LNA topology is basically a two-stage CS amplifier, as illustrated in Fig. 3, so it can work at a very low supply voltage and consume very low power. The overall transconductance of the LNA is equal to the multiplication of the individual transconductance of M_1 and M_2. Therefore, it has comparable power gain to the cascaded CS topology.

2.2 Input Matching Network

The input of the LNA needs to be matched to the output of the filter following the antenna to minimize reflections between the LNA and the antenna. To reach input matching, the conditions are given by [7]:

$$Z_{source} = Z^*_{in,1}, \tag{1}$$

$$Z_{out,1} = Z^*_{in,2}, \tag{2}$$

$$Z_{out,2} = Z^*_{L} \tag{3}$$

where Z_{source} is the impedance seen at the gate of M_1 when looking towards the antenna as illustrated in Fig. 3, $Z_{in,1}$ is the input impedance of M_1, and Z_L is the load impedance.

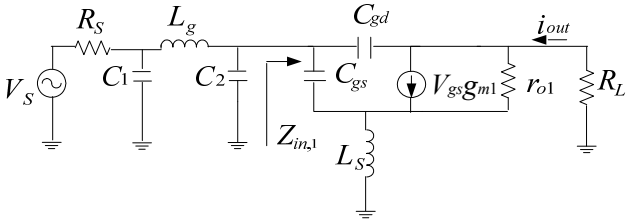


Fig. 4. The small-signal equivalent circuit of M1.

A simple small-signal equivalent circuit of the first gain stage is illustrated in Fig. 4, where R_s is the source impedance, R_L is the load impedance, and g_{m1} and C_{gs} represent the transconductance and gate-to-source capacitance of the M_1, respectively. C_{gd} is gate-to-drain capacitance of the M_1, and r_{o1} is the output impedance of MOSFETs. Assuming that C_{gd} is relatively small, which is generally the case in practical designs, a simplified expression of the input impedance of M_1 $Z_{in,1}$ is given by

$$Z_{in,1} \approx jw_0 L_s + \frac{1}{jw_0 C_{gs}} + \frac{g_{m1}}{C_{gs}} L_s \tag{4}$$

where w_0 is the operating frequency. The Z_{source} equation is given by $Z_{source} = R_{source} + jw_0 L_{source}$. Therefore, we can obtain R_{source} and L_{source} as:

$$R_{source} = \frac{\alpha}{(1 - w_0^2 C_1 C_2 L_g R_s)^2 + (\beta w_0)^2}, \tag{5}$$

$$L_{source} = \frac{-(\beta R_s + \alpha L_g C_2)}{(1 - w_0^2 C_1 C_2 L_g R_s)^2 + (\beta w_0)^2} \tag{6}$$

where α and β are expressed as $\alpha = R_s + L_g + w_0^2 C_1^2 R_s^2 L_g$ and $\beta = R_s C_2 + R_s C_1 + L_g C_2$, respectively. With the matching conditions specified in (1) - (3), we can obtain:

$$\mathrm{R}_{source} = \frac{g_{m1}L_s}{C_{gs}}, \tag{7}$$

$$jw_0 L_{source} = -jw_0 L_s - \frac{1}{jw_0 C_{gs}}. \tag{8}$$

From (7) and (8), the operating frequency w_0 can be derived as

$$w_0 = \sqrt{\frac{1}{(L_{source} + L_s)C_{gs}}}. \tag{9}$$

From the input matching conditions (1) - (3), the effective transconductance of the first stage $G_{m1.eff}$ is written as [16]:

$$G_{m1,\,eff} = \frac{i_{out}}{v_s}$$

$$\approx \frac{g_{m1}}{jw_0 C_{gs}(jw_0 L_s + jw_0 L_{source} + R_{source}) + 1 + jw_0 g_m L_s}. \tag{10}$$

From (7) - (10), one obtains

$$G_{m1} = \frac{g_{m1}}{2w_0 C_{gs1} R_{source}} \tag{11}$$

where G_{m1} is expressed as $G_{m1}=|G_{m1.eff}|$. From (1) - (3), we can also know the effective transconductance of the second stage G_{m2} as

$$G_{m2} = \frac{g_{m2}}{2w_0 C_{gs2}\,\mathrm{Re}(Z_{in,\,2})}. \tag{12}$$

The overall effective transconductance is equal to multiplication of the individual transconductance of M_1 and M_2. From (10) - (12), it is clear that the effective transconductance of the gain stages is strongly influenced by the transistor overdrive voltage [9]. Therefore, two cascaded stages are employed in the proposed LNA topology to boost the amplifier gain for ultra-low-voltage operations.

2.3 Noise Figure Analysis

As the first active building block in a RF receiver, the LNA is required to provide sufficient gain such that the noise contributed from the following stages can be effectively suppressed [10]. In a cascade amplifier, the total noise figure can be expressed as [18]

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_2 G_1} + \ldots \tag{13}$$

where NF_n and G_n are the noise figure and the gain of n-th stage. According to (13), the noise figure and gain of the first stage are both very important for the total noise figure contribution. Thus, the first stage should be carefully designed to achieve good input matching and to make a trade-off among gain, noise figure and power consumption.

The noise factor of a two-port network, such as the LNA, can be expressed as [1]

$$F = F_{\min} + \frac{G_n}{R_{source}}\left|Z_{source} - Z_{opt}\right|^2 \tag{14}$$

where G_n is the equivalent noise conductance, F_{min} is the minimum noise factor, R_{source} is the real part of Z_{source}, and $Z_{opt}=R_{opt}+jX_{opt}$ is the optimum source impedance [1]. F_{min} can be minimized by properly choosing the width of MOSFETs, but for a constant DC current, it is not a good choice. Therefore, to minimize the NF, NF = 10 log F (dB), it is very important to design the matching network of the LNA such that the second term in equation (14) is close to zero, which means that Z_{source} should be very close to Z_{opt}.

The matching conditions for minimum noise figures of the cascaded gain stages are given by [17]

$$Z_{source} = Z_{opt,\,1}, \tag{15}$$

$$Z_{out,\,1} = Z_{opt,\,2}. \tag{16}$$

With the matching conditions specified in (1) - (3) and (15), we can obtain

$$Z_{source} = Z^*_{in,\,1} = Z_{opt}. \tag{17}$$

From (17), this yields

$$R_{source} = R_{in,\,1}, \tag{18}$$

$$R_{opt} = R_{source}. \tag{19}$$

The source inductive degeneration matching topology is shown in Fig. 2(a). In this case, Z_{source} is written as

$$Z_{source} = R_s + jw_0 L_g \tag{20}$$

where R_s is the characteristic impedance of the system which is usually 50 Ω. From (19) and (20), its NF can be minimized at a desired frequency only if R_{opt} of the CS device is close to R_s. Therefore, for a given frequency of operation and DC current consumption, the width of the CS device must be adjusted so that the characteristic impedance is close to 50 Ω. However, it may increase the power consumption.

According to the definition of matching topology, noise and power matching of the LNA are achieved when (19) and (20) are satisfied. Therefore, when $R_{in,\,1}$ is smaller than R_{opt}, there is a trade-off between NF and S11. S11 less than –10 dB is adequate for the LNA in most applications [1]. Therefore, even when $R_{in,\,1}$ of the MOSFET is smaller than R_{opt}, R_{source} could be brought closer to R_{opt} by adjusting the values of L_g, C_1 and C_2 for better noise matching. However, as shown in the previous section, if $R_{in,\,1}$ is much smaller than R_{opt}, then the C_1, C_2 (or L_g) value that is needed to bring R_{source} closer to R_{opt} might not be suitable to satisfy the input matching requirements of the LNA. Therefore, we add an inductive source degeneration L_s. It can facilitate the input matching to 50 Ω, and provides

good linearity and high reverse-isolation, which helps with the amplifier stability.

2.4 Simulation Results

The circuit simulations of the proposed design are completed in the environment of ADS (Advanced Design System). The simulation S-parameters are shown in Fig. 5(a-c). The maximal power gain is 14.4 dB at 2.4 GHz, S11 is –18.1 dB and S22 is –12.7 dB at 2.4 GHz. The noise figure reaches 1.6 dB at 2.4 GHz, and IIP3 of the LNA is –9.0 dBm. The complete layout of the LNA is shown in Fig. 5(d); the total area is 0.472 mm^2 (0.80 mm×0.59 mm). The DC power consumption of the LNA is only 0.96 mW from a 0.9 V supply. These simulation results show that the input and output stage of the LNA achieve good matching, and meanwhile the NF and power consumption are also very small, which satisfies the requirements of a RF circuit very well.

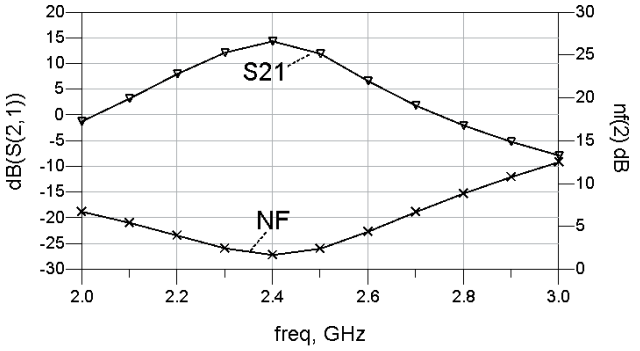
A commonly used figure of merit (FOM) for low-power LNAs is the ratio of power gain to DC power consumption ($Gain/P_{dc}$). To compare the overall performance of amplifiers, we have used an additional FOM which includes the effect of amplifier gain, noise figure, linearity (IIP3), operation frequency (f_0) and DC power consumption (P_{dc}) as follows [16].

$$FOM = 10 \cdot \lg\left(100 \cdot \frac{Gain[dB]}{(F-1) \cdot P_{dc}[mW]} \cdot \frac{IIP3[mW]}{P_{dc}[mW]}\right) + 10 \lg\left(\frac{f_0}{1GHz}\right) \quad (21)$$

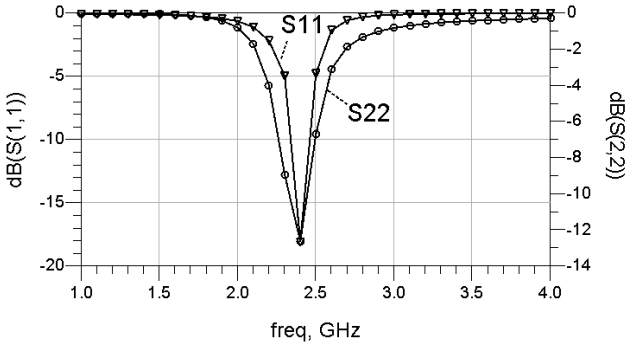
Data from other low power CMOS LNAs are also provided in Tab. 1. The comparison shows that this ultra low power LNA can provide better overall performance than other circuits in terms of gain, noise figure, linearity, DC power consumption and frequency of operation.

3. Conclusion

An ultra-low-voltage and ultra-low-power CMOS Low Noise Amplifier (LNA) in a standard 0.18 μm CMOS technology is designed and implemented. To substantially reduce the DC power consumption, we present a modified current-reused two-stage common source architecture. At DC power consumption of only 960 μW with 0.9 V power supply. This 2.4 GHz LNA has a simulation gain of 14.4 dB and noise figure of 1.6 dB. Under this bias condition, the simulation IIP3 is –9 dBm, and the S11 and S22 are better than –12 dB. These simulation results show that the LNA has the best overall figure of merit (FOM) among recently published low power CMOS LNAs.



(a)



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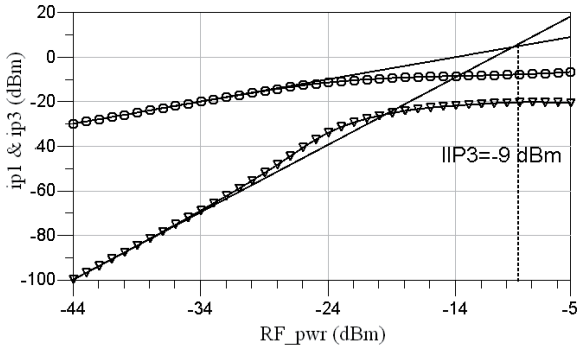
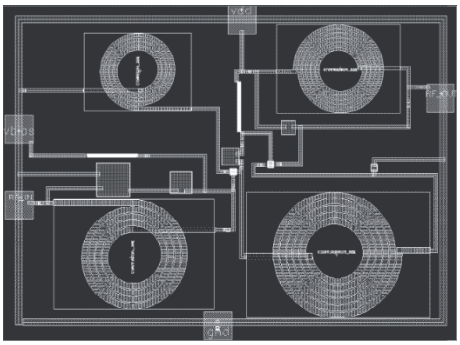


(c)



(d)

Fig. 5. Simulation results of the LNA. (a) S21 and NF. (b) S11 and S22. (c) IIP3. (d) The layout of the LNA.

Reference	Gate length (um)	Frequency (GHz)	S11 (dB)	S22 (dB)	S21 (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	FOM (MHz)
[6]	0.18	5.7	-14	-17	11.45	3.4	-8	3.96	18.0
[11]	0.18	24	-11.9	-13	14	4.9	-10.8	7.9	22.6
[15]	0.18	2.4	-10.37	-12.47	11.79	3.89	-3.0	13.5	18.7
[18]	0.13	5.0	-20	-31	14.3	2.93	-16	0.64	25.0
This work	0.18	2.4	-18.1	-12.7	14.4	1.6	-9.0	0.96	30.3

Tab. 1. Performance comparison.

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