

Decomposed Implicit Models of Piecewise - Linear Networks

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Abstract

The general matrix form of the implicit description of a piecewise-linear (PWL) network and the symbolic block diagram of the corresponding circuit model are proposed. Their decomposed forms enable us to determine quite separately the existence of the individual breakpoints of the resultant PWL characteristic and their coordinates using independent network parameters. For the two-diode and three-diode cases all the attainable types of the PWL characteristic are introduced.

Introduction

In recent papers [1],[2],[3] several methods of piecewise-linear (PWL) network synthesis have been introduced as well as a new approach based on an implicit description of the whole system [4],[5],[6]. The corresponding circuit model usually contains an active linear transformation block loaded by ideal diodes as basic PWL elements. However, none of these methods provides the possibility of determining and realizing all attainable types and shapes of the resultant PWL characteristic including all special cases; in other words no systematic synthesis of the PWL networks has been published yet. The present contribution suggests how to achieve that by using the generalization and modification of the procedure introduced in [4],[5],[6].

Global implicit model

Consider a structure consisting of a linear active transformation $(m+n)$ -port and a nonlinear loading n -port (Fig.1a). The transformation block can be realized by $(m+n)$ multiple voltage controlled voltage sources (MVCVSs), $(m+n)$ linear resistors, and one independent voltage source U (Fig.1b). Loading block is represented by n separate ideal diodes whose A-V characteristics are of simple rectangular shape (Fig.4b). The double-line symbols

in Fig.1 represent sets of network elements [6]. Similarly,

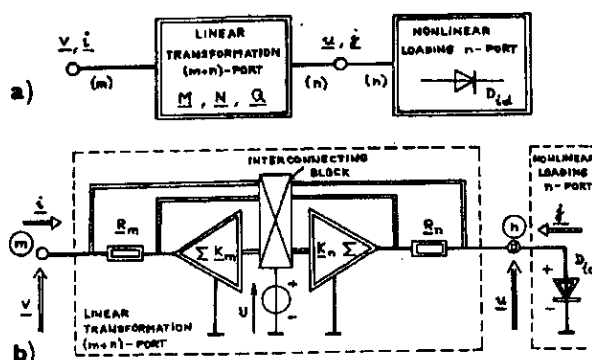


Fig.1. General form of the symbolic representation of PWL network. a) Block diagram. b) Circuit model containing MVCVSs and ideal diodes

the double lines and the full lines symbolize sets of zero-current and nonzero-current connections, respectively. Denoting the vectors of the external variables as

$$\mathbf{v} = [v_1, \dots, v_m]^T, \mathbf{i} = [i_1, \dots, i_m]^T \quad (1)$$

and those of the internal variables as

$$\mathbf{u} = [u_1, \dots, u_n]^T, \mathbf{j} = [j_1, \dots, j_n]^T \quad (2)$$

the nonlinear loading block can be then described by

$$\mathbf{u}, \mathbf{j} < 0, \mathbf{j}^T \cdot \mathbf{u} = 0 \quad (3)$$

and the linear transformation block generally by

$$\mathbf{M}[\mathbf{v}, \mathbf{u}]^T + \mathbf{N}[\mathbf{i}, \mathbf{j}]^T + \mathbf{Q} = 0 \quad (4)$$

As the configuration of the nonlinear block (set of ideal diodes) is chosen, the synthesis of the required PWL characteristic is then reduced to that of the linear transforma-

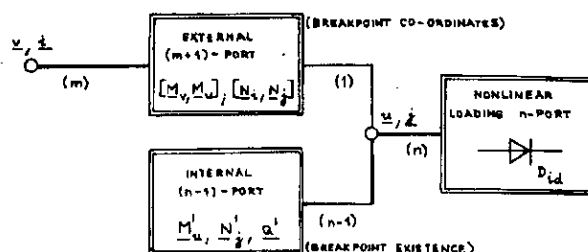


Fig.2a. Decomposed form of the symbolic representation of PWL network, block diagram

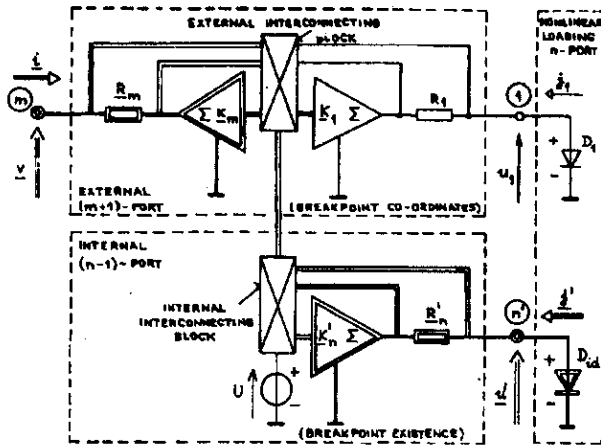


Fig. 2b. Decomposed form of the symbolic representation of PWL network, circuit model containing MVCVSs and ideal diodes

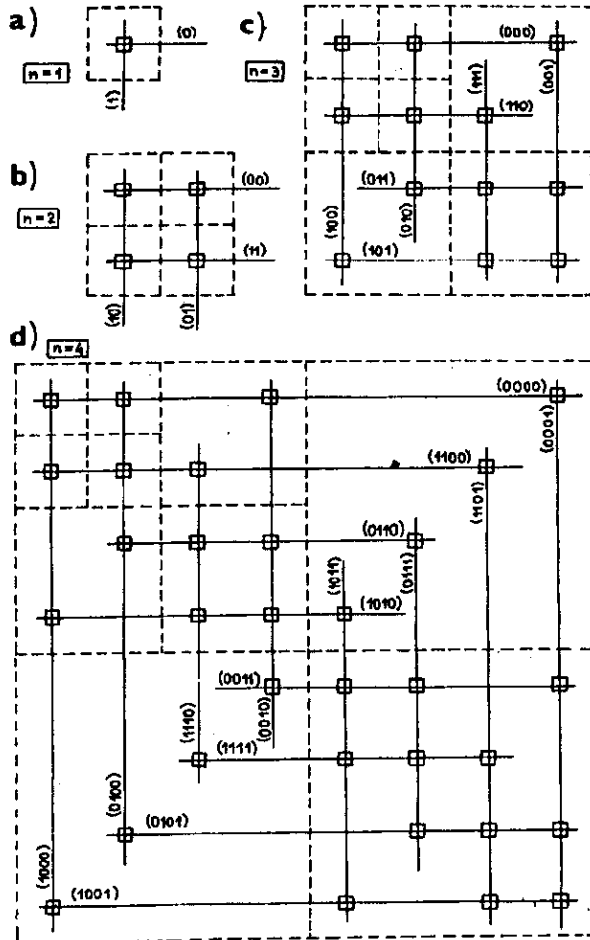


Fig. 3. Symbolic representation of all the possible diode-state combinations. a) to b) One diode to four diodes case

tion block. After finding the matrices M , N , Q (Fig. 1a) the corresponding MVCVS gain matrices K_m , K_n (Fig. 1b) can easily be derived [6]. Each MVCVS can be realized by one op. amp. and linear resistors [7].

Decomposed implicit model

The global implicit description (4) can be rewritten into the submatrix form

$$\begin{bmatrix} M_v & M_u \\ 0 & M'_u \end{bmatrix} \begin{bmatrix} v \\ u \end{bmatrix} + \begin{bmatrix} N_i & N_j \\ 0 & N'_j \end{bmatrix} \begin{bmatrix} i \\ j \end{bmatrix} + \begin{bmatrix} 0 \\ Q' \end{bmatrix} = 0 \quad (5)$$

which corresponds to the decomposed form of the symbolic representation of any PWL network. While formula (4) represents $(m + n)$ equations describing the whole transformation $(m + n)$ -port, the individual rows in formula (5) describe separately the external $(m + 1)$ -port and the internal $(n - 1)$ -port (Fig. 2). Such a block configuration enables us to decide quite separately the existence of the individual breakpoints of the resultant PWL characteristic and to adjust their co-ordinates by using the independent network parameters. Any of the n loading ideal diodes can be either in "off" state (symbol "0") or in "on" state (symbol "1") - see Fig. 4b, and therefore the total number of all possible diode-state combinations is generally 2^n (the synthesis procedure developed in [4],[5],[6] utilizes only $(n + 1)$ of these combinations.). Each breakpoint of the resultant PWL characteristic corresponds to such a transient state between two adjoining combinations when only one diode changes its state ($u_k = 0, j_k = 0$) while the remaining $(n - 1)$ diodes are either in "off" or in "on" state so that just $(n - 1)$ internal variables have nonzero values. As the internal block is described by $(n - 1)$ equations expressing the relations among the internal variables only, i.e.

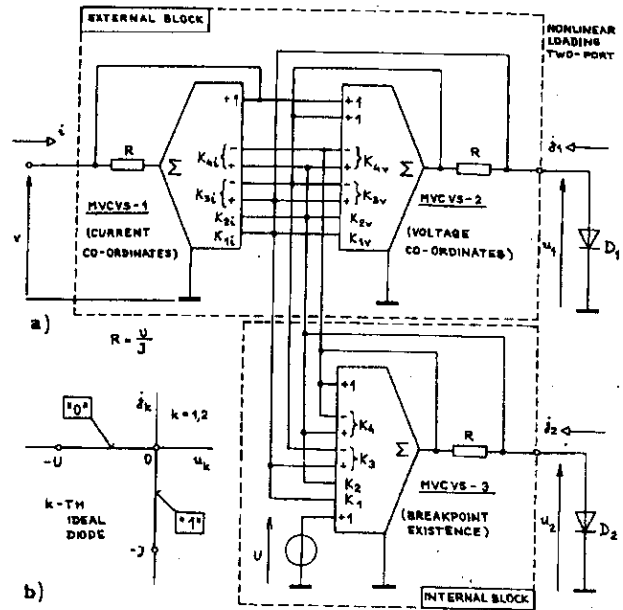


Fig. 4. Two diodes PWL network. a) Complete circuit model. b) Rectangular A-V characteristics of ideal diodes

$$M'_u u + N'_j j + Q' = 0 \quad (6)$$

it evidently determines the existence of the individual breakpoints of the resultant PWL characteristic. Then the initial step of the systematic synthesis of PWL network consists in derivation of submatrices M'_u , N'_j and Q' corre-

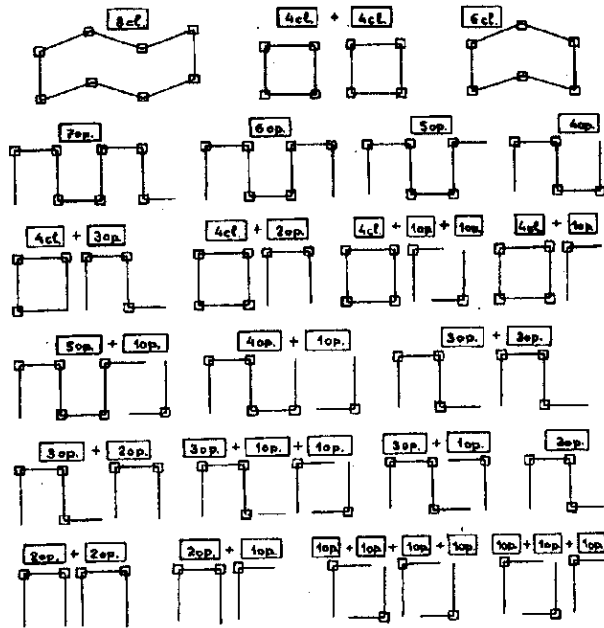


Fig. 5. Complete survey of all attainable types of PWL characteristics for three diodes case

Tab. 1 Complete solution for a two diodes network. a) 4 breakpoints (closed), b) 3 breakpoints (open).

TYPE OF PWL CHAR.:	CO-ORDINATES OF CHOSEN POINTS :	SYMBOLIC DIAGRAM:
a) 4 - CLOSED	$\mathbf{P1} : - [V_1; I_1]$ $\mathbf{P2} : - [V_2; I_2]$ $\mathbf{P3} : - [V_3; I_3]$ $\mathbf{P4} : - [V_4; I_4]$	
IMPLICIT DESCRIPTION OF THE TRANSFORMATION 3-PORT: $\begin{bmatrix} & I_1 & I_2 \\ U & V_1 & V_2 \\ & 1 & 1 \end{bmatrix} \begin{bmatrix} v \\ u_1 \\ u_2 \end{bmatrix} U^{-1} + \begin{bmatrix} J & I_3 & I_4 \\ & V_3 & V_4 \\ & 1 & 1 \end{bmatrix} \begin{bmatrix} i \\ j_1 \\ j_2 \end{bmatrix} J^{-1} + \begin{bmatrix} & \\ & \\ & \\ & \\ 1 \end{bmatrix} = \mathbf{Q}$		
b) 3 - OPEN	$\mathbf{P1} : - [V_1; I_1]$ $\mathbf{P2} : - [V_2; I_2]$ $\mathbf{P3} : - [V_3; I_3]$ $\mathbf{P4} : - [V_4; I_4]$	
IMPLICIT DESCRIPTION OF THE TRANSFORMATION 3-PORT: $\begin{bmatrix} & I_1 & I_2 \\ U & V_1 & V_2 \\ & 1 & 1 \end{bmatrix} \begin{bmatrix} v \\ u_1 \\ u_2 \end{bmatrix} U^{-1} + \begin{bmatrix} J & I_3 & I_4 \\ & V_3 & V_4 \\ & 1 & 1 \end{bmatrix} \begin{bmatrix} i \\ j_1 \\ j_2 \end{bmatrix} J^{-1} + \begin{bmatrix} & \\ & \\ & \\ & \\ 1 \end{bmatrix} = \mathbf{Q}$		
CO-ORDINATES OF DEPENDENT POINTS: $\mathbf{P5} = V_3 + V_4 - V_1$ $\mathbf{P6} = I_3 + I_4 - I_1$		

sponding to the required type of PWL characteristic. Although this problem has not been solved completely and generally yet, some principles of this procedure have been developed. The results for the two-diode and the three-diode case are available.

After finding submatrices M_u , N_j and Q we can substitute the values of the internal variables u, j for the individual breakpoints into the $(m + 1)$ equations describing the external block, i.e.

$$[M_u, M_u] [v, u]^T + [N_i, N_j] [i, j]^T = 0 \quad (7)$$

Tab. 1 Complete solution for a two diodes network. c) 2 breakpoints (open), d) 2 times 1 breakpoints (open).

TYPE OF PWL CHAR.:	CO-ORDINATES OF CHOSEN POINTS :	SYMBOLIC DIAGRAM:
c) 2 - OPEN	$\mathbf{P1} : - [V_1; I_1]$ $\mathbf{P2} : - [V_2; I_2]$ $\mathbf{P3} : - [V_3; I_3]$ $\mathbf{P4} : - [V_4; I_4]$	
IMPLICIT DESCRIPTION OF THE TRANSFORMATION 3-PORT: $\begin{bmatrix} & I_1 & I_2 \\ U & V_1 & V_2 \\ & 1 & 1 \end{bmatrix} \begin{bmatrix} v \\ u_1 \\ u_2 \end{bmatrix} U^{-1} + \begin{bmatrix} J & I_3 - I_2 & I_4 - I_1 \\ & V_3 - V_2 & V_4 - V_1 \\ & 1 & 1 \end{bmatrix} \begin{bmatrix} i \\ j_1 \\ j_2 \end{bmatrix} J^{-1} + \begin{bmatrix} & \\ & \\ & \\ & \\ 1 \end{bmatrix} = \mathbf{Q}$		
d) 1 - OPEN + 1 - OPEN	$\mathbf{P1} : - [V_1; I_1]$ $\mathbf{P2} : - [V_2; I_2]$ $\mathbf{P3} : - [V_3; I_3]$ $\mathbf{P4} : - [V_4; I_4]$	
IMPLICIT DESCRIPTION OF THE TRANSFORMATION 3-PORT: $\begin{bmatrix} & I_1 & I_2 - I_1 \\ U & V_1 & V_2 - V_1 \\ & 1 & 1 \end{bmatrix} \begin{bmatrix} v \\ u_1 \\ u_2 \end{bmatrix} U^{-1} + \begin{bmatrix} J & I_3 & I_4 - I_1 \\ & V_3 & V_4 - V_1 \\ & 1 & 1 \end{bmatrix} \begin{bmatrix} i \\ j_1 \\ j_2 \end{bmatrix} J^{-1} + \begin{bmatrix} & \\ & \\ & \\ & \\ 1 \end{bmatrix} = \mathbf{Q}$		
CO-ORDINATES OF DEPENDENT POINTS: $\mathbf{P5} = V_3 + V_4 - V_1$ $\mathbf{P6} = I_3 + I_4 - I_1$		

The values of the external variables v, i correspond to the coordinates of these breakpoints and then we can derive or choose the parameters of the submatrices in formula (7). It is worth nothing that the number of free parameters is only $(n + 2)$.

Attainable types of PWL characteristics

The procedure suggested above enables us not only to utilize all the possible diode-state combinations but also (for a given number of n ideal diodes) to derive all the attainable types of the resultant PWL characteristics. The symbolic representation introduced in Fig.3 ($n = 1$ to 4) is very useful for this purpose because every next diagram can easily be derived from the previous one by the systematic hierarchical procedure. It is evident that maximum two breakpoints of the possible n can exist on each segment.

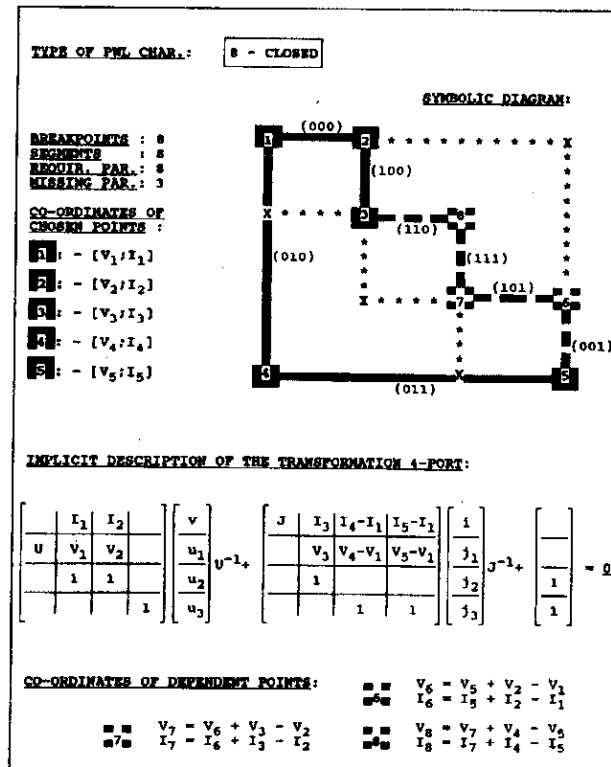
The complete universal circuit model for the simplest case ($m = 1, n = 2$) is introduced in Fig.4a which gives a possibility to realize all four attainable types of the resultant

A-V characteristic. It includes the closed (cl.), open (op.), and decomposed cases in accordance with Tab.1. Further details, including the corresponding values of the individual MVCVS gains, can be found in ref. [8]. For the multi-diode case the number of attainable types rapidly increases (for $n = 3$ it is 21 - see Fig.5). For a better survey the shapes of PWL characteristics introduced in Fig.5 are shown only symbolically. An example of the PWL characteristic for the case of three diodes (8 breakpoints, closed shape) is shown in its complete form in Tab.2.

Conclusions

Decomposed implicit model provides the following new possibilities in the synthesis of PWL networks:

Tab.2. Complete solution for a three diodes network (8 breakpoints closed)



- to utilize all the possible diode-state combinations
- to derive all attainable types of PWL characteristics
- to choose separately the existence of any breakpoint
- to adjust independently the co-ordinates of the chosen breakpoints.

The closed characteristic can be used, for example, in a simple nonharmonic generator synthesis while the decomposed characteristic in multi-stable network synthesis or modelling of bifurcations. In monothematic paper [9] some other details and complete solutions for all the attainable PWL characteristics ($n = 2, n = 3$) will be presented, i.e. the complete forms of the M, N, Q matrices, the values of the MVCVS gains in the corresponding circuit models, etc.

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