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Fractional-Order Oscillator Design Using Unity-Gain Voltage Buffers and OTAs

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Abstract In this study, a new voltage-mode fractional-order oscillator using two unity-gain voltage buffers, two operational transconductance amplifiers, one resistor, and two capacitors is presented. The design procedure of integer-order as well as fractional-order oscillator employing in total 20 MOS transistors is discussed. Effects of fractional-order capacitors on amplitude, phase, condition of oscillation, and frequency of oscillation are shown. Various case examples are given while SPICE simulations using TSMC 0.35 μm level-3 CMOS process parameters with ±1.65 V supply voltages verify their operation and compare with theoretical ones.

Keywords fractional-order circuit; fractional-order oscillator; flipped voltage follower; FVF; operational transconductance amplifier; OTA; voltage buffer; voltage-mode.

I. INTRODUCTION

Over the years several techniques for designing fractional-order oscillators have been introduced [1], [2]. The implementation of such oscillators evidently requires the use of a fractional-order capacitor (FoC), which brings to researchers several design features such as possibility of changing the frequency of oscillation (FO) and condition of oscillation (CO), as will be demonstrated in this study. In open literature, the FoC is implemented using RC network, via active emulator, or by fabricated chemical chips [3]-[8]. As our comparative study given in Table I shows, the previous works in this area are mainly focused on fractional-order oscillator design derived from classical active elements-based structures such as opamps and with their equivalent macro models containing two or more energy storage elements [9]. Particularly, the studied quadrature or multiphase oscillators are the classic ones such as the Wien-bridge oscillator [10], Colpitts oscillator [1] and Hartley oscillator [11]. Their behavior was investigated theoretically and also experimentally. On the other hand, this study aims to present the new fractional-order oscillator using compact CMOS active building blocks (ABBs) with reduced transistor count and shows the effect of fractional-orders on FO, CO, phase, and amplitude. Although class-AB cells are nonlinear, they can be modified as linear circuits with different combinations [12]-[15]. Beside this, due to their characteristics such as low output impedance, low quiescent power consumption, low voltage with large current sinking and high driving capability, they are more developed voltage followers compared to conventional ones. Some of them even have almost unity voltage gain on neglecting short-channel effects [15]. Therefore, they are mainly used in analogue and mixed-signal designs such as oscillators, filters, or communication applications. One of the most recently developed class-AB cell is the flipped voltage follower (FVF), which was introduced by Torralba et al. in 2002 [12]. This compact FVF is based on two complementary differential flipped voltage followers. Another high-performance ABB used in this study is the basic CMOS transconductor, which has a voltage to current (V–I) conversion capability and uses only two CMOS transistors and two control voltages [16], [17]. SPICE simulation results using TSMC 0.35 μm level-3 CMOS process parameters and with ±1.65 V supply voltages are given to verify the theoretical analysis based on using RC trees emulating the fractional operators $s/\alpha$. The paper is organized as follows: After this introductory part, used compact cells and integer- as well as fractional-order oscillator design procedure are briefly introduced. Section III presents the simulation results and the last two sections discussion of the results, concluding this study.

II. CIRCUIT DESCRIPTION

A. Voltage Buffer Using Flipped Voltage Follower (FVF)

The CMOS implementation of unity-gain voltage buffer based on class-AB flipped voltage follower, i.e. $V_{out} = V_{in}$, is shown in Fig.1(a) [12]. As it is evident, it uses two complementary differential flipped voltage followers (DFVFs)

![CMOS implementation of active blocks: (a) voltage buffer, (b) transconductor.](image-url)
TABLE I. COMPARATIVE STUDY OF FRACTIONAL-ORDER OSCILLATORS.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>No. of ABBs</th>
<th>No. of trans.</th>
<th>No. of R / C / L</th>
<th>Orders</th>
<th>Power supplies</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>-</td>
<td>1 BJT</td>
<td>1 gr. / 2 gr. / 1 fl.</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>[2]</td>
<td>3 opamp</td>
<td>-</td>
<td>9 fl. / 3 gr. / -</td>
<td>1.5</td>
<td>±15 V</td>
</tr>
<tr>
<td>[9]</td>
<td>1 opamp</td>
<td>-</td>
<td>3 fl. / 2 gr. / 1 fl. / -</td>
<td>1.8</td>
<td>-</td>
</tr>
<tr>
<td>[10]</td>
<td>1 opamp</td>
<td>-</td>
<td>1 fl. / 1 gr. / 1 gr. / -</td>
<td>1.7</td>
<td>-</td>
</tr>
<tr>
<td>[11]</td>
<td>1 opamp</td>
<td>-</td>
<td>2 fl. / 1 gr. / 2 fl. / -</td>
<td>2.6, 2.7</td>
<td>±2 V</td>
</tr>
<tr>
<td>Our</td>
<td>- 20 CMOS</td>
<td>1fl. / 1 fl.</td>
<td>1 gr. / -</td>
<td>1; 1.5; 2</td>
<td>±1.65 V</td>
</tr>
</tbody>
</table>

$m_{1p} - m_{3p}$ and $m_{1n} - m_{3n}$ with quiescent currents $i_{b1}$ and $i_{b2}$, respectively. When the input voltage signal $v_{in}$ increases with respect to the output voltage $v_{out}$, then $v_{GS(MP)}$ increases while $v_{GS(MN)}$ decreases. Similarly, current through $m_{1p}$ increases and $m_{3n}$ decreases. This generates a positive output current that charges the load capacitance and increases the output voltage $v_{out}$ until it reaches a value $v_{in}$. This buffer operates in class AB, resulting in transient currents of the output transistors much larger than their corresponding quiescent currents $i_{b1}$ and $i_{b2}$. Theoretically, the input and output impedance of this buffer are infinite and zero, respectively.

B. Operational Transconductance Amplifier (OTA)

The CMOS implementation of single-input differential-output transconductor is shown in Fig. 1(b). Assuming square-law behavior for the current–voltage relationship of the MOS transistors $m_{1p}$ and $m_{1n}$ and ignoring channel-length modulation effect, their drain currents will be given as in [16], [17], and, thus, the current–voltage relationship of the transconductor can be approximated by the linear expression: $I_{out} = g_{m1}v_{in}$, where $g_{m1} = k_{n}v_{OD}$. This linear behavior is achieved under the assumptions: $k_{p} @ k_{N}$ and $v_{GS} @ v_{DD} + v_{th,n} - v_{in,p}$, where $v_{th,n}$ and $v_{th,p}$ are the threshold voltages of the NMOS and PMOS transistors. In order to keep the transistors in saturation region, the constraints $v_{DD} + v_{th,n}$, $v_{DD} + v_{th,p}$ should be satisfied, where $v_{DD}$ is the (common) drain voltage of transistors $m_{1p}$ and $m_{1n}$, respectively.

Interconnecting the transconductor with unity-gain current follower (see $m_{2p} - m_{4p}$ and $m_{2n} - m_{4n}$ in Fig. 1(b) [18]) the current–voltage relationship of the transconductor can be characterized with the equation $I_{m1} = g_{m1}v_{in}$.

C. Integer-Order Oscillator Design

The proposed voltage-mode oscillator with unity-gain voltage buffers based on flipped voltage followers, two transconductors, one resistor, and two capacitors is shown in Fig. 2. Assuming both capacitors are ideal with capacitance $C$ and used ABBs are also ideal, i.e., ignoring parasitic effects, the characteristic equation (CE) of this oscillator is as follows:

$$CE: \ s^{2}RC_{2} + s(g_{m1}RC_{1} - g_{m2}RC_{2}) + g_{m2} = 0, \quad (1)$$

from which the CO and FO can be evaluated as:

$$CO: \ C_{2} \left( \frac{g_{m2}}{g_{m1}} \right) \cdot \left( \frac{1}{RC_{2}} \right) \cdot \left( 1 - \left( \frac{g_{m2}}{g_{m1}} \right) \cdot \left( \frac{1}{RC_{2}} \right) \right) \cdot \left( \frac{g_{m1}}{g_{m2}} \right) \cdot \left( \frac{1}{RC_{2}} \right) \cdot \left( \frac{1}{RC_{1}} \right) = 0 \quad (2),(3)$$

therefore, the FO can be controlled by adjusting the value of the resistor $R$ without affect of CO.

D. Fractional-Order Oscillator Design

Replacing in the oscillator in Fig. 2 the ideal capacitors $C_{i}$, $i = \{1, 2\}$, by FOCs ($C_{1} \Rightarrow C_{\alpha}, C_{2} \Rightarrow C_{\beta}$) with impedance $a(s) = 1/(s^{\alpha}C_{a})$, $\rho(s) = 1/(s^{\beta}C_{\beta})$, the fractional-order system can be described as:

$$\left( \frac{d^{\alpha}v_{o1}}{dt^{\alpha}} \right) = \frac{1}{RC_{\alpha}} \left( \frac{g_{m1}}{C_{\alpha}} + 1 \right) \left( \frac{g_{m1}}{C_{\alpha}} \right) \left( v_{o1} \right) - \left( \frac{1}{RC_{\alpha}} \right) \left( \frac{g_{m1}}{C_{\alpha}} \right) \left( \frac{1}{RC_{\beta}} \right) \left( \frac{g_{m2}}{C_{\beta}} \right) \left( v_{o2} \right) \quad (4)$$

hence, the CE from (1) takes the following general form:

$$CE: \ s^{2}RC_{2} + s^{\alpha}g_{m1} + \left( \frac{g_{m1}}{C_{\alpha}} \right) + \left( \frac{g_{m2}}{C_{\alpha}} \right) + \left( \frac{g_{m2}}{C_{\beta}} \right) = 0 \quad (5)$$

By solving (5) the CO and FO of fractional-order oscillator can be obtained as:

$$CO: \ \frac{w^{\alpha}g_{m1}}{2} + \frac{g_{m1}}{C_{\alpha}} = \frac{g_{m2}}{C_{\beta}} + \left( \frac{g_{m1}}{C_{\alpha}} \right) + \left( \frac{g_{m2}}{C_{\beta}} \right) \Rightarrow 0$$

$$FO: \ \frac{w^{\alpha}g_{m1}}{2} + \frac{g_{m1}}{C_{\alpha}} = \frac{g_{m2}}{C_{\beta}} + \left( \frac{g_{m1}}{C_{\alpha}} \right) + \left( \frac{g_{m2}}{C_{\beta}} \right) \Rightarrow 0$$

(6a,b)

Fig. 2. Proposed voltage-mode oscillator.
The phase difference $\phi$ between the two outputs $V_{o1}$ and $V_{o2}$ is calculated as:

$$f = f_{o1} = \frac{p[1 - \text{sign}(a_{12})]}{2} = \frac{p[1 - \text{sign}(a_{21})]}{2} = f_{o2},$$

(7)

where

$$f_{o1} = \tan^{-1} \frac{w^\sigma \sin(0.5 \alpha p)}{w^\rho \cos(0.5 \alpha p)} - a_{11}, \quad f_{o2} = \tan^{-1} \frac{w^\delta \sin(0.5 \beta p)}{w^\rho \cos(0.5 \beta p)} - a_{22}.$$  

(8)

### III. Simulation Results

The behavior of voltage buffer, transconductor, and proposed voltage-mode integer- and fractional-order oscillators have been verified by SPICE simulations. In the design, transistors are modeled by the TSMC 0.35 $\mu$m level-3 CMOS process parameters ($V_{th,N} = 0.545$ V, $V_{th,P} = -0.714$ V, $\mu_C = 436.26$ cm$^2$/V s, $\mu_F = 212.23$ cm$^2$/V s, $t_{ox} = 7.9$ nm). In simulations, the DC power supply voltages of given structures were set equal to +$V_{DD} = -V_{SS} = 1.65$ V and the aspect ratios of MOS transistors were 15 $\mu$m/0.5 $\mu$m and 5 $\mu$m/0.5 $\mu$m for all PMOS and NMOS, respectively. The bias currents in voltage buffers were set $I_{B1} = I_{B2} = 250$ mA, which results in DC voltage gain 0.957 with $f_{3dB}$ frequency of 1.644 GHz. Similarly, the transconductance gains $g_{m1}$ ($I_{sat}/V_{th}$) and $g_{m2}$ ($I_{sat}/V_{th}$) are computed as 1.639 mA/V and 1.778 mA/V, respectively, and their $f_{3dB}$ frequency is found to be 3.83 GHz and 47.63 GHz. Hence, the maximum operating frequency of transconductors are $f_{max} = \min\{g_{m1}, f_{3dB2}\} = 3.83$ GHz.

As a first step, the performance of the proposed integer-order oscillator ($\alpha = \beta = 1$) was evaluated. In this case, both capacitances have been chosen as: $C_1 = 55$ nF, $C_2 = 100$ nF, while the resistor was: $R = 1$ k$\Omega$; according to (3), the theoretical value of the oscillation frequency was $f_0 = 2.86$ kHz. Figure 4(a) shows the simulated output waveforms with frequency of oscillation 1.63 kHz.

As a second step, the fractional-order oscillator with an order of $s^{0.5}$ has been implemented. For this purpose, the capacitors of the integer-order oscillator in Fig. 2 were replaced with their fractional-order equivalents which were realized using the second-order RC tree shown in Fig. 3. Note that the values of $g_{m1,2}$ have been kept the same with the previous case. Considering that $\alpha = 0.9$ and $\beta = 0.6$, their equivalent pseudo-capacitance values will be as follows: $C_1 = 136.3$ nF $s^{-0.1}$ ($C_1 = 55$ nF @ f0) and $C_2 = 3.78$ nF $s^{-0.4}$ ($C_2 = 100$ nF @ f0). Also, the resistor $R$ will equal to 1.64 k$\Omega$. Computed component values are given in Table II. During simulations, in order to start up the oscillations, the resistor was set 3.4 k$\Omega$ and the obtained FO was $f_0 = 0.741$ kHz. The simulated output waveforms are shown in Fig. 4(b).

Fig. 3. RC tree realization of FoC.

Fig. 4. Simulated output waveforms of the proposed voltage-mode oscillator: (a) $\alpha = \beta = 1$, (b) $\alpha = 0.9$, $\beta = 0.6$, (c) $\alpha = \beta = 0.5$.

Fig. 5. Simulated frequency spectrum of outputs.

**TABLE II. COMPONENT VALUES USED IN SPICE SIMULATIONS**

<table>
<thead>
<tr>
<th>Variables</th>
<th>Orders</th>
<th>$a = 0.5$</th>
<th>$a = 0.8$</th>
<th>$a = 0.6$</th>
<th>$a = 0.5$</th>
<th>$a = 0.8$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_1$ [k$\Omega$]</td>
<td>10.6</td>
<td>5.9</td>
<td>98.6</td>
<td>80.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_2$ [k$\Omega$]</td>
<td>508</td>
<td>279.4</td>
<td>39.5</td>
<td>161.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_1$ [nF]</td>
<td>24.3</td>
<td>44.2</td>
<td>48</td>
<td>54.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_1$ [k$\Omega$]</td>
<td>3.5</td>
<td>1.9</td>
<td>85.6</td>
<td>1.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_2$ [nF]</td>
<td>6.4</td>
<td>115.8</td>
<td>14.4</td>
<td>97.3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:** $\alpha$ and $\beta$ are order parameters of the proposed fractional-order oscillator.
V. Conclusion

This paper demonstrates that a fractional-order oscillator with two different pseudo-capacitances can still sustain sinusoidal oscillations. In addition, it was shown that the condition and the frequency of oscillations are functions of the fractional-order. Clear advantage of the proposed compact fractional-order oscillator, compared to opamp-based counterparts presented in [1], [2], [10], and [11], is its simplicity, owing to the fact that employs only 20 MOS transistors.

REFERENCES