Tuning Range and Power Handling Analysis of DTC-based Matching Networks for Reconfigurable High Power RF Circuits

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Submitted December 23, 2016 / Accepted July 19, 2017

Abstract. *This paper presents the analysis of tuning range and power handling of digitally tunable capacitors (DTCs) in reconfigurable high power RF circuits. The proposed scheme can be applied to reconfigurable RF system design e.g. smart antenna, Software Defined Radio (SDR) and Cognitive Radio (CR) systems. The power handling of the DTC can be enhanced by connecting the DTC in series with a fixed capacitor. The combination of a DTC and a fixed capacitor leads to modified tuning range of the total capacitance. Both the power handling and the tuning range are described in this paper by empirical equations in such a way, that a proper combination of DTCs and fixed capacitors can be determined for the design of any reconfigurable RF system. As an example of applications, a frequency band reconfigurable power amplifier was designed and fabricated. The reconfigurable input and output matching networks utilize DTCs and fixed capacitors as tuning elements.*

Keywords

DTC, power handling, reconfigurable RF circuits, matching network, Software Defined Radio

1. Introduction

Standards of current wireless communication systems in order to meet the market demands require adaptive data transmission, high data rate, flexible network configuration and low cost. In case of RF frontends, there is a design trend in providing the flexibility for various wireless standards. Such agile wireless systems range from multi-standard antenna matching, beamforming, phase locking, powering and filtering [1]. In case of hybrid circuits, a single hardware can be reconfigured to serve several standards and applications. For example, a power amplifier can be configured to a high efficiency mode or a high linearity mode [2]. In case of integrated circuits, a reconfigurable IC is attractive since it can serve many applications as the reconfiguration can simply be carried out using the control pins of the chip to select the operating frequency or mode [3–4]. For Software Defined and Cognitive Radio, this implies additional degrees of freedom for the system with a limited number of components. Consequently, tunable matching networks are required to match various impedances of different operating modes to the reference impedance e.g. 50 Ohm. Mostly, reconfigurable RF circuits are based on tunable capacitors. For filtering, numerous publications proposed frequency tunable filters using tunable capacitors based on MEMs and varactor diodes [5–8]. A wide capacitive tuning range allows a large variety of impedances which can be matched. In addition, the tunable capacitors must be able to withstand the peak power of the system whereas the self-resonant frequency must be higher than the operating frequency. A systematic scheme for tunable matching network design in order to fulfill such system requirements would be beneficial for acceleration of the design process while reducing losses due to damage of the devices.

Tunable capacitors based on microelectro-mechanical system (MEMs) and Barium Strontium Titanate (BST) can offer superior quality factor, but their package sizes are relatively large. In addition, the costs of MEMs and BST-tunable capacitors are relatively high. An overview of tunable capacitor technologies with their pros and cons was presented in [1] and [9]. Tuning the capacitance value with varactor diodes requires analog bias voltages across the diodes resulting in a complicated capacitor tuning circuit and increased size of the entire system. Moreover, the major drawbacks of varactor diodes are their small power

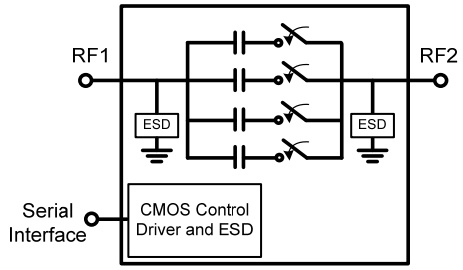

Fig. 1. Circuit diagram of a DTC. This figure was reproduced according to [13].

handling and limited tuning range. Compared to varactor diodes, capacitor tuning using PIN diodes is less complicated since only the control voltages for switching on and off the PIN diodes are required. To adjust the capacitance value, the PIN diodes act as switches to connect or disconnect each capacitor of the capacitor bank to the ground and sequentially vary the overall capacitance value. A more convenient way to vary the capacitance value is the use of DTCs since the tuning is executed using a digital control signal. Instead of PIN diodes, switching the capacitors in the capacitor bank of the DTC is carried out by digital CMOS logics so that the capacitance value can be varied using serial interface control. Other advantages of DTCs also include their low cost and small size. After being launched into the market, tunable bandpass filters using DTCs as tuning elements are gradually reported in the literature [10–11]. In addition, DTCs can also be used for reconfigurable matching networks as reported in [12]. Figure 1 depicts capacitance tuning in a DTC. In this paper, various combinations of DTCs or combination of DTCs with fixed capacitors are thoroughly analyzed in terms of capacitive tuning range and power handling in order to provide a design guide for reconfigurable matching networks of high power RF circuits.

The paper is organized as follows: a tuning element of high power RF circuits using a DTC connected in series with a fixed capacitor is described in Sec. 2 with elaboration on enhancement of the power handling. The modified tuning range of the total capacitance is discussed in Sec. 3. In Sec. 4, self-resonant frequency shift caused by a series fixed capacitor is analyzed. Section 5 provides a selection guide for DTCs and fix capacitors in the tunable matching network design. As a design example, a frequency reconfigurable power amplifier (PA) is presented in Sec 6. The PA designed using DTCs as the tuning elements in the input- and output matching networks has been fabricated and measured. Also, experiment results on the power handling of a tuning element are shown and discussed. An idea for future work regarding tuning elements with multiple DTCs is introduced in Sec. 7 following by the conclusions in Sec. 8.

2. Power Handling of the DTC Tuning Element

Although tunable capacitors can provide the required

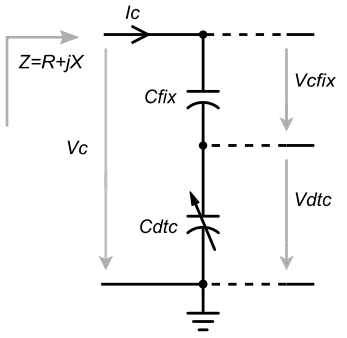

Fig. 2. Capacitive tuning element with a fix series capacitor and a DTC.

degrees of freedom for system reconfiguration, their power handling is much lower compared to fixed capacitors. In general, the voltage drop over the tunable capacitor is limited to prevent it from being damaged by an excess voltage. At the expense of tuning range, the power handling of a reconfigurable network can be enhanced by a combination of tunable and fixed capacitors. A series circuit consisting of a tunable and a fixed capacitor forms a capacitive voltage divider where the voltage drop over the entire capacitive circuit is distributed among the tunable and the fixed capacitor. Consequently, the voltage drop over the tunable capacitor can be reduced while the power handling can be increased. This technique can be applied to any kind of tunable capacitors as described in [14], specifically for the case of BST tunable capacitors according to [15] and for MEMS tunable capacitors as reported in [16]. In this paper, a similar concept is applied to DTCs. Figure 2 shows a simplified circuit of the capacitive voltage divider.

The current I_c flows through both capacitors resulting in the voltage drop V_{cfix} across the series capacitor C_{fix} and the voltage drop V_{dtc} across the DTC with the capacitance C_{dtc}. Thus, the relative voltage rating of the capacitive circuit compared to the DTC without the series fixed capacitor can be expressed as

$$\frac{V_c}{V_{dtc}} = 1 + \frac{C_{dtc}}{C_{fix}}. \tag{1}$$

The power handling of the DTC is defined as P_{dtc} whereas the power handling of the entire series circuit is defined as P_c. Since the power P is proportional to V^2, the relative power handling p_{TE} of the capacitive tuning element compared to the DTC without the series capacitor is

$$p_{TE} = \frac{P_c}{P_{dtc}} = \left(\frac{V_c}{V_{dtc}}\right)^2 = \left(1 + \frac{C_{dtc}}{C_{fix}}\right)^2. \tag{2}$$

Alternatively, the relative power handling can also be expressed in dB as

$$p_{TE,dB} = 10\log\left(\frac{P_c}{P_{dtc}}\right) = 20\log\left(\frac{V_c}{V_{dtc}}\right). \tag{3}$$

From (2), the relative power handling in case of a very large C_{fix} is approximately one, so that the power handling is not improved compared to a single DTC. If $C_{fix} = C_{dtc}$,

the power handling can be four times the power handling of the DTC. By further decrease of C_{fix}, the voltage drop over C_{fix} and the total power handling are increased. Theoretically, the power handling of the entire circuit can be increased up to the power handling of the fixed capacitor which is normally much larger than that of the DTC. Since C_{dtc} can be varied, the total power handling also depends on the DTC state. Lower value of C_{dtc} leads to lower power handling compared to the case with a higher C_{dtc}. Thus, $C_{dtc,min}$ –the minimum tunable capacitance of the C_{dtc}– determines the power handling of the series circuit. By prohibiting some of the low states, the power handling of the series tuning element can be increased. In addition, power handling enhancement of the capacitive tuning element can only be realized at the cost of tunable range of the total capacitance. The effect of the series fixed capacitor on the tunable range will be described in the next section.

3. Modified Tuning Range

In general, the tuning range of the DTC can be found in the data sheet of the component. In this work, DTCs from Peregrine Semiconductor are chosen. The total capacitance of the series capacitive circuit from Fig. 2 is calculated to

$$C_{total} = \frac{C_{fix} \cdot C_{dtc}}{C_{fix} + C_{dtc}}. \tag{4}$$

Notwithstanding that a small C_{fix} leads to a high power handling, the tunable range of the total capacitance is small in this case. If C_{dtc} is much larger than C_{fix}, the total capacitance is then almost equal to C_{fix}. If the highest state of DTC provides a capacitance of $C_{dtc,max}$, the tuning rate TR representing a ratio of the maximum total capacitance C_{max} to the minimum total capacitance C_{min} is then calculated to

$$TR = \frac{C_{max}}{C_{min}} = \frac{C_{fix} \cdot C_{dtc,max}}{C_{fix} + C_{dtc,max}} \cdot \frac{C_{fix} + C_{dtc,min}}{C_{fix} \cdot C_{dtc,min}} \tag{5}$$

or

$$TR = \frac{C_{fix} \cdot C_{dtc,max} + C_{dtc,min} \cdot C_{dtc,max}}{C_{fix} \cdot C_{dtc,min} + C_{dtc,max} \cdot C_{dtc,min}}. \tag{6}$$

From this equation, if C_{fix} is very small, then the tuning rate is 1, implying that the entire circuit cannot be used as a tuning element. In contrast, if C_{fix} is very large, then the tuning rate is near to $C_{dtc,max}/C_{dtc,min}$ which is the tuning rate of the DTC without the series capacitor. In order to validate this analysis, a PE64906 DTC and a fixed capacitor are connected in series according to Fig. 2. The input reactance X of the series circuit was measured at 2.1 GHz for three cases with C_{fix} = 0.5 pF, 2 pF and 4 pF. The measurement results are plotted in Fig. 3 as functions of the DTC state number. As expected, the value of X can be varied in a wide range in case of a DTC without a fixed capacitor. By adding C_{fix} in series to the DTC, the tuning

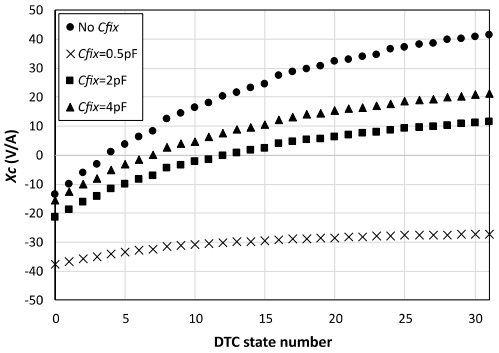

Fig. 3. Measured input reactance at 2.1 GHz of the circuit from Fig. 2 with a PE64906 DTC and varied C_{fix}.

range of X is decreased in such a way that, the smaller value of C_{fix} the smaller is also the tuning range of the input reactance X. Besides the modification of the tuning range, it can also be observed that the DTC worked as a tunable capacitor only from state 0 to state 3. From state 4 to 31, the DTC acted as a tunable inductor with positive reactance values. The reason for this phenomenon is the self-resonance of the DTC which will be described in the next section. By connecting the DTC with a small C_{fix} capacitance value, the self-resonance effect can be compensated. In this experiment with C_{fix} = 0.5 pF, all states from 0 to 31 provide negative input reactance and the circuit from Fig. 2 represents a tunable capacitor as it should.

4. Self-Resonance

The behavior of a DTC is described so far with a simple model that assumes a linear dependence of C_{dtc} on the state number. This model is accurate only at low frequencies. By increasing the operating frequency, the linear dependence between the capacitance and the state number is ceased by the self-resonance of the device. From the product specification of the DTC [13], this nonlinear dependence can especially be observed at higher DTC states and high operating frequency which explains the positive reactance of the DTC shown in Fig. 3. In order to precisely predict the behavior of the DTC in a wide range of frequency, device model of the DTC is provided by the manufacturer for circuit simulations. For determination of the self-resonant frequency, the capacitance values of the PE64909 DTC at different states are swept over the frequency range from 0.05 to 10 GHz. The simulation result is presented in Fig. 4(a). The highest resonant frequency of the DTC is 9.5 GHz for state 0. The resonant frequency is decreased with increasing state number. For state 31, the resonant frequency is at 3 GHz. Self-resonance determines the limit of DTC's operating frequency. Especially at the highest DTC state, the resonant frequency $f_{res,dtc}$ is the lowest. The self-resonance can be shifted to a higher frequency by connecting a fixed capacitor in series with the DTC according to Fig. 2. A fixed capacitor with a higher resonant frequency $f_{res,Cfix}$ compared to the highest state of DTC can compensate the inductance in the DTC model so that the resonance of the tuning element can be shifted to

a higher frequency $f_{res,TE}$. As an example, the DTC from Fig. 4(a) is connected in series with a 2.4 pF fixed capacitor GQM1555C2D2R4BB01. This fixed capacitor can withstand 200 V DC voltage drop and the self-resonance of this device shows up at 6 GHz [17]. For both capacitors, device models provided by the manufacturer are used in the simulation. The frequency is swept from 0.05 to 10 GHz. The simulation result in Fig. 4(b) shows that the resonant frequency is modified compared to a single DTC.

For state 0, $f_{res,TE}$ is 8.2 GHz whereas for state 31, resonance occurs at 4.1 GHz. Even though $f_{res,TE}$ at state 0 is decreased compared to a single DTC—since the resonant frequency of the fixed capacitor at 6 GHz is less than that of the DTC at state 0—but the resonant frequency of state 31 is increased since the resonant frequency of the fixed capacitor is higher than the resonant frequency of the DTC at state 31. In this case, $f_{res,Cfix}$ lies between resonances of the lowest and the highest DTC states. As a consequence, the variation of resonant frequency is reduced compared to the case with a single DTC. In case of a fixed capacitor from the same manufacturer and process, it is known that the self-resonant frequency decreases with increasing capacitance value [18]. Therefore, a small C_{fix} can push the resonance of the series circuit to a higher frequency compared to a larger C_{fix} which confirms the measurement results from Fig. 3. By selecting a fixed capacitor with $f_{res,Cfix}$ higher than $f_{res,dtc}$ of every DTC state, then $f_{res,TE}$ at every state is higher than $f_{res,dtc}$.

5. DTC and Fixed Capacitor Selection

As described in previous sections, the power handling and the tuning rate of the series capacitive tuning circuit can be determined by C_{fix}. Since there is a tradeoff between these requirements, the value of C_{fix} must carefully be chosen. In order to address this issue in a closer look, an example of the series capacitive tuning element is described as follows. The tuning element consists of a fixed capacitor C_{fix} and a DTC with the part number PE64906 [13]. This CMOS-based DTC can operate in the frequency range from 100 to 3,000 MHz. For simplicity, typical capacitance value for the operating frequency of 100 MHz is chosen in this example. Due to a low operating frequency, it is assumed here that there is no self-resonance as described in Sec. 4 and the capacitance of the DTC is a linear function of the state number. The tuning rate $C_{dtc,max}/C_{dtc,min}$ of this DTC is 5.10:1 with a capacitance step size of 0.119 pF, $C_{dtc,min}$ of 0.9 pF (state 0) and $C_{dtc,max}$ of 4.6 pF (state 31) at this operating frequency. The peak voltage drop across both RF pins of this device is 30 V as per product specifications. The influence of the series capacitor C_{fix} on the tuning rate and the power handling is shown in Fig. 5.

On the horizontal axis, the value of C_{fix} is normalized by a division over $C_{dtc,min}$. The relative power handling described at the beginning of Sec. 2 and the tuning rate described in Sec. 3 are then plotted over this normalized

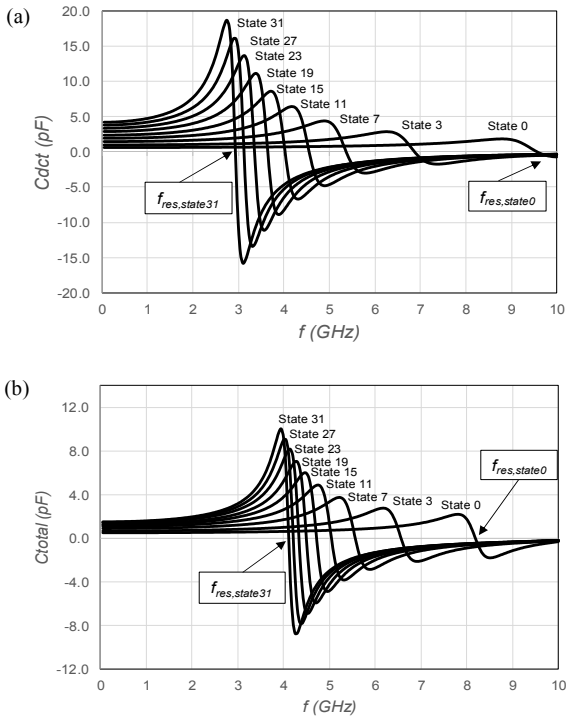

Fig. 4. Simulated capacitance at different states as functions of the operating frequency: (a) PE64909 (DTC), (b) PE64909 (DTC) and GQM1555C2D2R4BB01 (C_{fix}) connected in series.

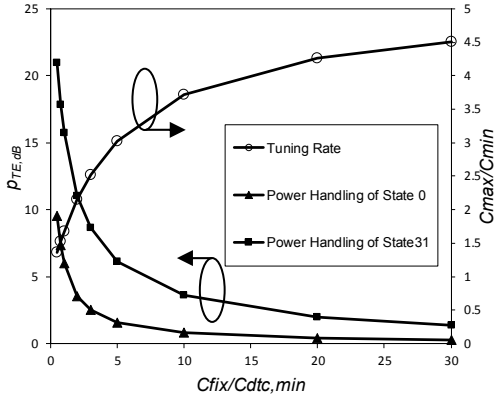

Fig. 5. Power handling and tuning rate of the capacitive tuning element comprising a DTC and a series capacitor as functions of normalized fixed series capacitance.

capacitance. From the figure, it is obvious that the power handling of state 31 is higher than that of state 0. For other states between 0 and 31, the power handling curves lie between the curves of state 0 and state 31. Consequently, the power handling can also be increased by avoiding some of the low states. However, leaving out some lower states leads to a decreased tuning rate due to increased $C_{dtc,min}$. Therefore, only the power handling of the DTC at its lowest state is considered in this paper. The first data point in this figure represents the normalized capacitance $C_{fix}/C_{dtc,min}$ of 0.5 or $C_{fix} = 0.45$ pF. The relative power handling of the tuning element is around 9.5 dB. However, the tuning rate of the capacitance is reduced to 1.37:1 compared to 5.10:1 in case of the DTC without the series ca-

pacitor. The maximum value of $C_{fix}/C_{dtc,min}$ in this figure is 30. The power handling in this case is around 0.3 dB, whereas the tuning rate of 4.50:1 is provided.

6. Design Example

To fulfill requirements of reconfigurable high power RF systems, tuning elements must carefully be designed. Tunable range, power handling and operating frequency of the tuning element must be considered. As discussed in previous sections, the tuning element can be realized with appropriate combinations of fixed and digitally tunable capacitors. For certain operating modes, look up table for the control signal of the DTCs should be developed to define limitations on frequency, power and tunable range of the designed tuning element. As an example, a band reconfigurable PA was designed and fabricated using DTCs in the tuning elements of the matching networks. Although there are other PA design concepts in the literature using fixed matching networks which can cope with multiple operating frequencies including wideband and dual-band PAs [19], but the PA design in the following example aims to serve other purpose than providing amplification at different frequencies only. The utilization of DTCs in the matching networks provides the advantages of high flexibility and agility to react to any kind of load modification. The fact that DTCs can be tuned using electrical control signals allows a fast changing load to be rematched to 50 Ohm almost in real time. The same design concept can also be applied for other systems, e.g. smart antennas or filters as well as in reconfigurable integrated circuits. The major design challenge of a band-reconfigurable PA is the design of reconfigurable input- and output matching networks. The input matching network requires for a specific operating frequency an appropriate tunable range of the tuning element to match the reference impedance to the impedance required at the input side of the power device. In case of output matching, power handling is also a critical design parameter due to the high output power of the amplifier.

The design goal of the reconfigurable PA is concluded in Tab. 1 and its block diagram is shown in Fig. 6. Main components of the PA are the power device, reconfigurable input and output matching as well as the bias networks. After considering the required specifications, the power transistor of the PA was chosen to be CGH27015F GaN HEMT in order to cope with the required bandwidth and the output power. The input and output matching networks have been designed in a way that they can match 50 Ohm at the source and the load side to Z_S and Z_L to achieve maximum gain and output power. The impedances seen at the input and output of the power device are Z_{in} and Z_{out}, respectively.

The design process of each operating frequency started from a large signal S-parameter simulation at the input side where a conjugate match was provided at the gate of the device at this step. Then, a load pull simulation

Design goals	Tuning element type
Operating frequencies	2.1/2.45 GHz
Bandwidth	80 MHz
Output power	37 dBm
Operating class	AB (V_{dd} = 28 V, I_{dq} = 1.06 A)
Power device	Discrete GaN HEMT

Tab. 1. Design goals of the band reconfigurable power amplifier.

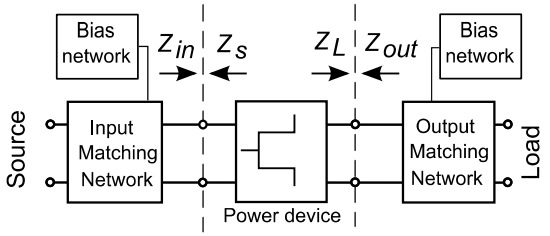

Fig. 6. Block diagram of a power amplifier (figure modified from [2]).

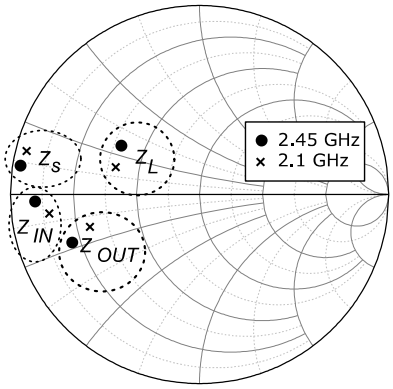

Fig. 7. Source-, load-, input and output impedance for the input and output matching of the power amplifier.

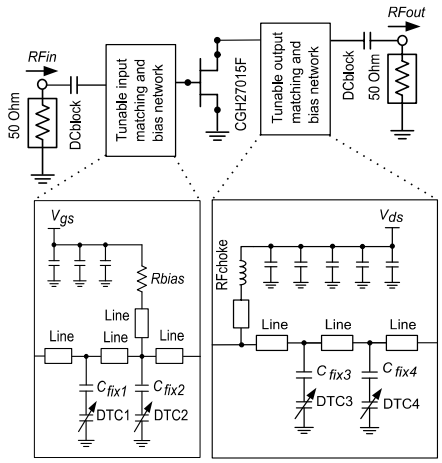

Fig. 8. The proposed 2.1/2.45 GHz band reconfigurable PA design with tunable input and output matching networks. (Figure modified from [2]).

was performed for the output matching in order to determine the optimal impedance presented to the drain side so that the highest gain and output power can be obtained [2]. The impedances are simulated and plotted into the Smith chart in Fig. 7 for optimized matching conditions providing

the highest gain and output power. It is noticeable from the figure that the matching networks' impedances are not the exact conjugates of the device's impedances.

The tunable matching networks designed for this reconfigurable PA are depicted in Fig. 8. The PA was fabricated on an ARLON25N substrate. A photograph of the fabricated PA is shown in Fig. 9. The capacitive parameters of the tuning elements in this PA are configured according to Tab. 2.

Special care of the tuning element at the output side must be taken since it carries higher power than the input side. The input and output matching are verified by the measurement of S_{11} and S_{22} for both frequencies as shown in Fig. 10.

The output power P_{out}, gain and power added efficiency (*PAE*) are plotted as functions of the input power P_{in} for both frequencies in Fig. 11. The measurement was carried out up to $P_{in} = 20$ dBm due to power limitation of the measurement system. With $P_{in} = 20$ dBm, the maximum output power measured was at 38.85 dBm and 35.18 dBm at 2.1 and 2.45 GHz, respectively. Simulation and measurement results agree well as shown in Fig. 11.

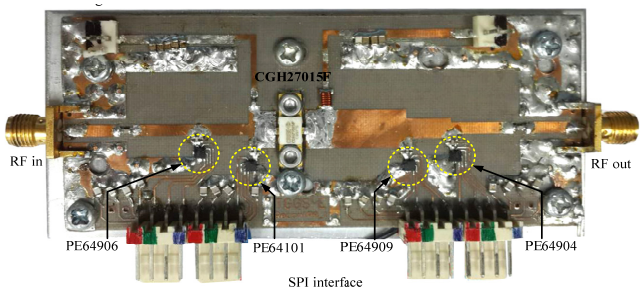

Fig. 9. Photograph of the fabricated PA.

Freq. (GHz)	DTC1 PE64906 (State) $C_{fix1} = 2$ pF	DTC2 PE64101 (State) $C_{fix2} = 12$ pF	DTC3 PE64909 (State) $C_{fix3} = 1.5$ pF	DTC4 PE64904 (State) $C_{fix4} = 2.7$ pF
2.1	(0)	(23)	(4)	(20)
2.45	(0)	(11)	(2)	(3)

Tab. 2. Capacitive parameters for each frequency setting (see Fig. 8).

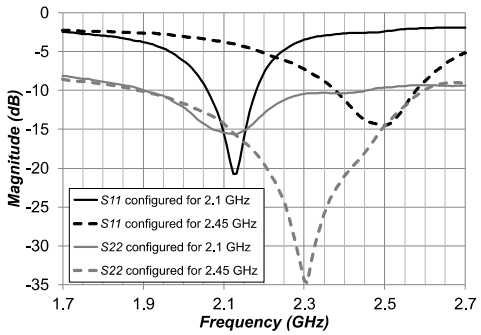

Fig. 10. Measured S_{11} and S_{22} at both frequencies showing good matching conditions provided by the reconfigurable matching networks.

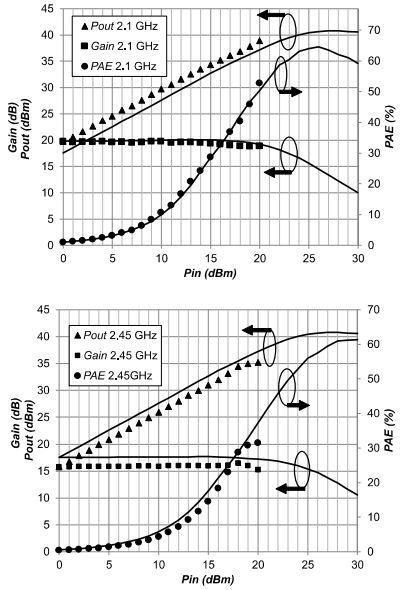

Fig. 11. Power sweep simulation (solid lines) and measurement results (data points) of the proposed PA with output power, gain and *PAE* for both frequencies.

In order to confirm the proposed concept by an experiment, the PA output is now fed to a short 50 Ohm series microstrip line terminated with a 50 Ohm load. The center of the line is connected with a parallel resonator designed for a resonant frequency of 2.1 GHz. The capacitor of the parallel resonator is a DTC PE64102 (state 0) for test configuration 1. For test configuration 2, a fixed capacitor and PE64102 (state 0) connected in series represent the parallel capacitor of the resonator. Figure 12 depicts both test configurations with all parameters. In configuration 1, C_{dtc} can be calculated from 2.1 GHz resonant frequency and a parallel inductance of 1.1 nH to 5.2 pF. In configuration 2 with $C_{fix} = 8.2$ pF connected in series with C_{dtc}, a parallel inductance of 1.8 nH was selected in order to maintain the resonant frequency of 2.1 GHz. The power handling can be enhanced by 4.2 dB according to (2) and (3). In the experiment, the power fed to the test configuration was varied from 0 dBm to 36 dBm and the power P_L was measured at the load after the steady state was reached. Since the nominal power handling of PE64102 is 26 dBm, P_L cannot be significantly increased after the PA output power $P_{out,PA}$ reached 25 dBm. In contrast, test configuration 2 still allowed 30 dBm to be transferred to the load with a 1 dB insertion loss (see Fig. 13). Therefore, improvement of the power handling by adding a series fixed capacitor to the DTC has been confirmed. The experimental value of power handling enhancement in Fig. 13 agrees well with the calculation and the graph in Fig. 3.

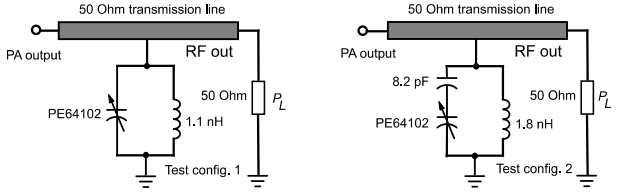

Fig. 12. Test configurations for power handling.

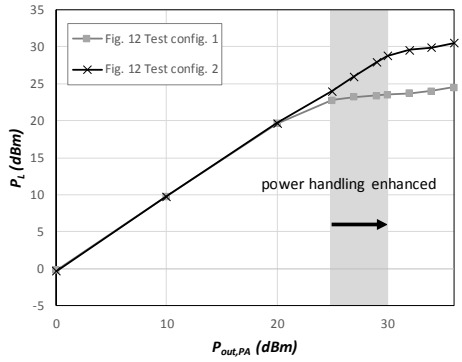

Fig. 13. Power handling of configuration 1 and 2 from Fig. 12.

7. Tuning Element with Multiple DTCs

The combination of a fixed series capacitor and a DTC cannot increase the power handling while maintaining the tuning rate. However, a combination of two identical DTCs connected in series can overcome this limitation. In Fig. 2, if C_{fix} is replaced by another DTC in a way that the tuning element consists of two identical DTCs connected in series which are synchronously controlled, the relative power handling compared to a single DTC is 6 dB according to (3). In order to increase the power handling while keeping the minimum and maximum tunable capacitance, parallel DTCs can be added. Figure 14 depicts a tuning element with a combination of series and parallel DTCs with m series elements, where each series element consists of n parallel DTCs.

If all DTCs are identical and controlled synchronously, the total capacitance of the tuning element is then

$$C_{\text{total}} = \frac{n}{m} \cdot C_{\text{dtc}}. \tag{7}$$

As a result, the power handling can be increased with the factor m^2. The tuning rate $TR = C_{\text{total,max}}/C_{\text{total,min}}$ is equal to that of a single DTC. The maximum capacitance

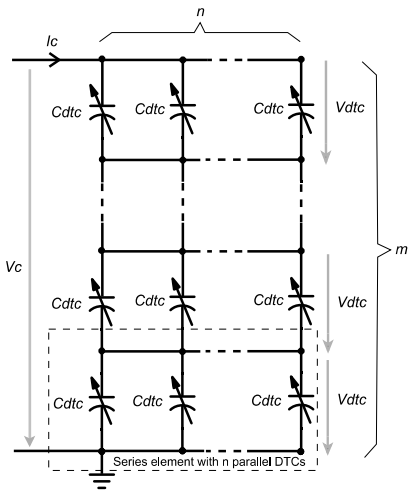

Fig. 13. Capacitive tuning element with combination of series and parallel DTCs.

of the tuning element $C_{\text{total,max}}$ is equal to $(n/m)C_{\text{dtc,max}}$. In the same way, the minimum capacitance $C_{\text{total,min}}$ of the tuning element is $(n/m)C_{\text{dtc,min}}$. On the one hand, the advantage of this tuning element is the flexibility to adjust the power handling and the range of tunable capacitance. On the other hand, using several DTCs leads to a higher hardware cost. Moreover, multiple DTCs and complex interconnection due to several control bus lines can lead to an increased size of the circuit. Considering the footprint of the DTC provided in the data sheet, the control bus can occupy up to approx. 50% of the area of the entire tunable circuit. Moreover, additional layers are also required for the clock signal, ground and supply voltage. This tuning element concept will be verified in the future work.

8. Conclusions

Critical issues of the capacitive tuning elements in reconfigurable RF circuits are the operating frequency, power handling and tunable range. In this work, all the issues are thoroughly analyzed for tuning elements using DTCs. A series fixed capacitor connected to the DTC can increase the power handling while compromising the tuning range. The self-resonance can also be shifted to a higher frequency compared to a single DTC by adding a series fixed capacitor. The proposed analysis has been verified by measurement experiments.

As a design example, a 2.1/2.45 GHz frequency band reconfigurable PA has been developed. The input and output matching networks of the PA utilize combinations of DTCs, fixed series capacitors and transmission line sections as tuning elements. The fabricated PA can provide small signal gain of 20 dB at 2.1 GHz and 15 dB at 2.45 GHz. The maximum output power could not be determined due to 20 dBm power limit of the measurement system. The highest output power measured was at 38.85 and 35.18 dBm at 2.1 and 2.45 GHz, respectively. This design concept of capacitive tuning element can be applied for the design of smart antennas as well as reconfigurable RF integrated and hybrid circuits.

Acknowledgments

This research was funded by King Mongkut's University of Technology North Bangkok, Contract no. KMUTNB-GOV-58-28. Also, this work has been supported by the Thailand Research Fund under the TRF Senior Research Scholar Program with the contract number RTA5780010.

References

[1] MORANDINI, Y., GLORIA, D., QUEMERAIS, T., et al. Digitally tuning capacitor : from RF to millimeter wave applications in advanced CMOS technologies. In *Workshop Novel Materials,*

Devices and Technologies for High Performance On-chip RF Applications. Bordeaux (France), 2012.

[2] JANTARACHOTE, V., SIRIVECH, N., CHALERMWISUTKUL, S. Frequency band and operating class reconfigurable GaN HEMT power amplifier for sustainable wireless communications and energy applications. In *Proceedings of The 20th Asia-Pacific Conference on Communication (APCC2014)*. Pattaya (Thailand), 2014, p. 156–160. DOI: 10.1109/APCC.2014.7091623

[3] ANDREWS, C., MOLNAR, A. C. A passive mixer-first receiver with digitally controlled and widely tunable RF interface. In *IEEE Journal of Solid-State Circuits*, 2010, vol. 45, no. 12, p. 2696 to 2708. DOI: 10.1109/JSSC.2010.2077151

[4] WU, W., LONG, J. R., STASZEWSKI, R. B., et al. High-resolution 60-GHz DCOs with reconfigurable distributed metal capacitors in passive resonators. In *Digest of Papers - 2012 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. Montreal (Canada), 2012, p. 91–94. DOI: 10.1109/RFIC.2012.6242239

[5] ISLAM, M. F., ALI, M., MAJLIS, B. Y. Tunable bandpass filter using RF MEMS variable capacitors. In *Proceedings of 2008 Asia-Pacific Microwave Conference (APMC)*. Hong-Kong (China), 2008, 4 p. DOI: 10.1109/APMC.2008.4958449

[6] CHANDRAHALIM, H., BHAVE, S. A. Digitally-tunable MEMS filter using mechanically-coupled resonator array. In *Proceedings of the IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*. Wuhan (China), 2008, p. 1020–1023. DOI: 10.1109/MEMSYS.2008.4443832

[7] CHO, Y. H., REBEIZ, G. M. Two-and four-pole tunable 0.7-1.1-GHz bandpass-to-bandstop filters with bandwidth control. *IEEE Transactions on Microwave Theory and Techniques*, 2014, vol. 62, no. 3, p. 457–463. DOI: 10.1109/TMTT.2014.2304360

[8] DJOUMESSI, E. E., WU, K. Reconfigurable RF front-end for frequency-agile direct conversion receivers and cognitive radio system applications. In *Digest of Papers - 2010 IEEE Radio and Wireless Symposium (RWS)*. New Orleans (LA, USA), 2010, p. 272–275. DOI: 10.1109/RWS.2010.5434205

[9] GRANT, P. D., DENHOFF, M. W., MANSOUR, R. R. A comparison between RF MEMS switches and semiconductor switches. In *2004 International Conference on MEMS, NANO and Smart Systems (ICMENS)*. Banff (Canada), 2004, vol. 27, no. 1, p. 33–39. DOI: 10.1109/ICMENS.2004.1509004

[10] JASCHKE, A., TESSEMA, M., SCHÜHLER, M., et al. Digitally tunable bandpass filter for cognitive radio applications. In *2012 IEEE 17th International Workshop on Computer Aided Modeling and Design of Communication Links and Networks (CAMAD)*. Barcelona (Spain), 2012, p. 338–342. DOI: 10.1109/CAMAD.2012.6335363

[11] CHUMA, E. L. Digitally tunable band-pass filter. *QEX(The Forum for Communications Experimenters)*, Jan./Feb. 2016, p. 3–8.

[12] WHATLEY, R., RANTA, T., KELLY, D. CMOS based tunable matching networks for cellular handset applications. In *IEEE MTT-S International Microwave Symposium Digest*. Baltimore (MD, USA), 2011. DOI: 10.1109/MWSYM.2011.5972913

[13] Product Specification PE64906, 2013. [Online]. Cited 2017-3-25. Available at: www.psemi.com/pdf/datasheets/pe64906ds.pdf

[14] TIGGELMAN, M. P. J. Thin film barium strontium titanate capacitors for tunable RF front-end applications. *Ph.D. Thesis*. University of Twente, The Netherlands, 2009.

[15] ABRECHT, M., FINK, T., BIGLER, W. Variable power capacitor for RF power applications. Patent no. WO 2016/034241, 2016.

[16] YAMAZAKI, H., IKEHASHI, T., SAITO, T., et al. A high power-handling RF MEMS tunable capacitor using quadruple series capacitor structure. In *2010 IEEE MTT-S International Microwave Symposium*. Anaheim (CA, USA), 2010, p. 1138–1141. DOI: 10.1109/MWSYM.2010.5518185

[17] MURATA. *GQM1555C2D2R4BB01 Capacitor Datasheet*. 2016. [Online]. Cited 2017-3-25 Available at: http://psearch.en.murata.com/capacitor/product/GQM1555C2D2R4BB01%23.html.

[18] MURATA. *The Effect of Non ideal Capacitors*. [Online]. Cited 2017-3-25 Available at: http://www.murata.com/~/media/webrenewal/products/emc/emifil/knowhow/12to14.ashx.

[19] MAKTOOMI, M. A., HASHMI M. S., GHANNOUCHI, F. M. A T-section dual-band matching network for frequency-dependent complex loads incorporating coupled line with DC-block property suitable for dual-band transistor amplifiers. *Progress in Electromagnetics Research C*, 2014, vol. 54, p. 75–84, 2014. DOI: 10.2528/PIERC14090403

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