# VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ
BRNO UNIVERSITY OF TECHNOLOGY

## FAKULTA ELEKTROTECHNIKY A KOMUNIKAČNÍCH TECHNOLOGIÍ
FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

## ÚSTAV RADIOELEKTRONIKY
DEPARTMENT OF RADIO ELECTRONICS

# AUDIO ZESILOVAČ VE TŘÍDĚ D PRO LABORATORNÍ VÝUKU
CLASS D AUDIO AMPLIFIER FOR LABORATORY MEASUREMENTS

BAKALÁŘSKÁ PRÁCE
BACHELOR'S THESIS


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# Bakalářská práce

bakalářský studijní obor **Elektronika a sdělovací technika**
Ústav radioelektroniky

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***Ročník:*** 3 ***Akademický rok:*** 2017/18

**NÁZEV TÉMATU:**

## Audio zesilovač ve třídě D pro laboratorní výuku

**POKYNY PRO VYPRACOVÁNÍ:**

V teoretické části práce navrhněte blokovou a obvodovou strukturu audio zesilovače ve třídě D, který by integroval vstupní analogové obvody, budič spínaných tranzistorů a koncový stupeň ve třídě D (výkon hlavních kanálů do cca 10 W / 4 nebo 8 ohmů). Zvolte řešení zesilovače s vnějším LC filtrem vyššího řádu, který by umožňoval demonstraci vlivu řádu filtru na výstupní signál zesilovače. Zadáním je požadován návrh audio zesilovače pro měření v laboratorní výuce předmětu Nízkofrekvenční a audio elektronika.

V praktické části práce vytvořte kompletní konstrukční podklady k realizaci návrhu (schéma zapojení, návrh desky plošného spoje, rozložení a soupiska součástek, atd.). Navržený audio zesilovač realizujte formou funkčního prototypu a experimentálním měřením v laboratoři nízkofrekvenční elektroniky ověřte jeho činnost. Výsledky měření zpracujte formou standardního protokolu a vytvořte kompletní podklady pro laboratorní úlohu.

**DOPORUČENÁ LITERATURA:**


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***Vedoucí práce:*** prof. Ing. Tomáš Kratochvíl, Ph.D.

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ
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# ABSTRACT

Bachelor's thesis delves into a field of Class-D audio amplifiers. Keystone part of the work summarizes theoretical knowledge focused on measuring techniques of low-frequency amplifiers and audio amplifier design. A deeper insight into building blocks of a general Class-D amplifier is also presented. Gained erudition is applied in the second part, which is devoted to a construction of the device. Exceptional attention is drawn to the design of robust external driver and sophisticated output analog filter. Blueprints required for a PBC layout are provided as well as outputs of performance measurements taken of a fabricated prototype.



# KEYWORDS

Audio amplifier performance measurements, power classes, Class-D amplifier, low-pass filter design, shoot-through protection circuits, PCB layout



# ABSTRAKT

Bakalárska práca sa zameriava na oblasť audio zosilňovačov pracujúcich v triede D. Významná časť práce sumarizuje teoretické poznatky z oblasti meracích techník nízkofrekvenčných audio zosilňovačov a návrhu zosilňovačov. Práca tak isto ponúka hlbší náhľad na stavebné bloky obecného zosilňovača v triede D. Získané poznatky sú aplikované v druhej časti, ktorá je zameraná na konštrukciu zosilňovača. Veľká pozornosť je venovaná návrhu robustného externého budiča a prepracovaného výstupného analógového filtra. Podklady potrebné k zhotoveniu DPS sú poskytnuté ako aj výsledky merania parametrov zhotoveného prototypu.



# KĽÚČOVÉ SLOVÁ

Meranie parametrov audio zosilňovačov, triedy zosilňovačov, zosilňovač v triede D, návrh dolnej priepusti, ochranné obvody proti shoot-through efektu, návrh DPS

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# PROHLÁŠENÍ

Prohlašuji, že svou bakalářskou práci na téma Audio zesilovač ve třídě D pro laboratorní výuku jsem vypracoval samostatně pod vedením vedoucí/ho bakalářské práce a s použitím odborné literatury a dalších informačních zdrojů, které jsou všechny citovány v práci a uvedeny v seznamu literatury na konci práce.

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V Brně dne **16. května 2018** ....................................

(podpis autora)

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I would like to express my sincere gratitude to my supervisor prof. Ing. Tomáš Kratochvíl, Ph.D., who guided me throughout the course of entire Bachelor’s thesis. I honestly appreciate the time professor dedicated to me during consultations and all the suggestions and comments he made concerning design of the device.

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# INTRODUCTION

Bachelor’s thesis is devoted to a construction of Class-D audio amplifier. The objectives are to design a mid-power audio amplifier that will serve laboratory purposes. It is not insisted on the quality of sound or power output level, but rather on demonstrativeness and device's robustness.

The thesis is divided into two major parts. First part is devoted to theoretical knowledge of audio amplifiers. Its aim is mainly to explain fundamental approaches to the design and performance measurements of an amplifier. Second part presents construction process of the device. Problems encountered during the design and particular solutions to them can be found in this section. Besides few alternative solutions and the reasons why they were not applied are presented as well.

By the agreement with supervisor, English was chosen as the language of the thesis.

# 1 INTRODUCTION TO AMPLIFIERS

Designing audio power amplifier implies both a science and an art. Since the very beginning of sound reproduction systems there has always been a tireless endeavor to build an amplifier with a purest sound, highest efficiency and cheapest price. First audio amplifiers introduced valves, whose popularity quickly spread and remains till nowadays. Thanks to their warm and ear-pleasing sound valves will never become obsolete. Arrival of bipolar transistors paved the way for an entirely new approach to amplifiers. Low price, high longevity and uncompromising parameters make these devices perfect choice for a vast majority of various applications. From low-power mobile amplifiers through mid-power automotive audio systems to high-power amplifiers installed in auditoriums. They can be fitted anywhere.

The purpose of power amplifiers is to convert the line-level signal to a large signal that can be fed into a loudspeaker. The line-level signal typically attains values from 1 V to 3 V and is not supposed to supply much current to the power stage. The output of power amplifier typically produces tens of volts and is expected to drive a heavy load or a loudspeaker. Usual gain of the system is on the order of 20 to 30. The working principle is presented in the Figure 1.1.

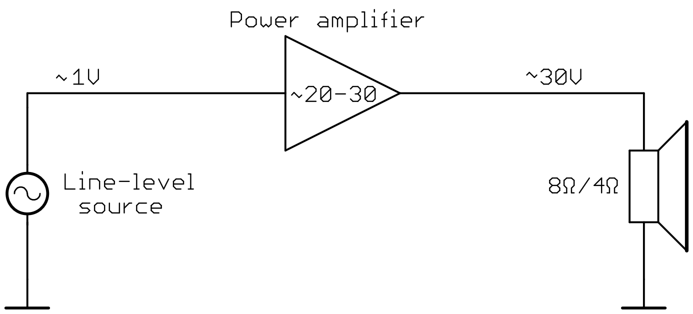



Figure 1.1: Power amplifier in a circuit

# 2 PERFORMANCE REQUIREMENTS

Audio system measurements are taken so as to determine the performance of an equipment. This way can designers and customers ensure that audio systems are working according to the specification and any defect of an audio path is within acceptable bounds. The main goal of a measurement is to specify device's performance in an audible spectrum from 20 Hz to 20 kHz. Although the outer bounds of the spectrum are inaudible for most people, precise comparison of devices requires to gauge broader spectral area [1].

## 2.1 Power output

One of the most important parameters of an amplifier is its power output. It defines the maximum electric power an amplifier can deliver to a loudspeaker. In applications where high efficiency is required, Class-D or Class-T amplifiers are used. Particularly in low-power portable devices lifetime of battery is limited and so cannot be wasted in heat losses. High-power amplifiers must work with high efficiency as well, otherwise hundreds of watts would be turned into heat. Middle-power applications are mainly occupied by “classic” types of amplifiers because heat-sinks need not to be very large and power supplies can be of a conventional toroid-and-bridge-rectifier arrangement. This design is considerably cost saving.

While discussing amplifier power output one fact needs to be taken into consideration. The nature of a human hearing causes that in order to increase subjective loudness twice, the power of an amplifier cannot be merely doubled or even quadrupled. It has to be elevated at around 10 times. Practically speaking, 30 W Class-B amplifier will not sound much louder that its 15 W Class-A cousin.

Maximum output power $P_{max}$ is by convention stated for 8 Ω or 4 Ω load. It can be measured by applying continuous sine wave signal of nominal frequency 1 kHz and varying amplitude. The maximum amplitude of non-clipped sine wave $V_{max}$ is acquired by TRMS voltmeter and inserted into following formula:

$$P_{max} = \frac{V_{max}^2}{R_{LOAD}} \tag{2.1}$$

where $R_{LOAD}$ represents loudspeaker characteristic resistance [1].

## 2.2 Efficiency

Efficiency η very closely corresponds to amplifier's power output. It defines a ratio at which power supply's energy is converted into energy of output signal driving a loudspeaker. The better conversion, the higher efficiency, the smaller heat-sink dimensions. Calculation can be done using the following formula:

$$\eta = \frac{P_{max}}{V_S \cdot I_S} \tag{2.2}$$

where $V_S$ and $I_S$ represent power supply voltage and power supply current. $P_{max}$ stands for amplifier's maximum power output [1].

## 2.3 Output impedance

Another important amplifier's parameter is an output impedance. It expresses the amount of frequency response change an amplifier may generate when driven by a specific reactive loudspeaker. Usually lower output impedance is considered better as the sound is more consistent regardless of the load it drives. Despite, in valve amplifiers, high output impedance is rather desired as it can excessively roll off high frequency components, what consequently results in its typical sound. Usually 100 mΩ or less in a whole audio bandwidth is satisfactory. Amplifiers with output filters tend to have higher values of output impedance. Typical relationship between output impedance $Z_{OUT}$ and frequency f is shown in the Figure 2.1 [1].

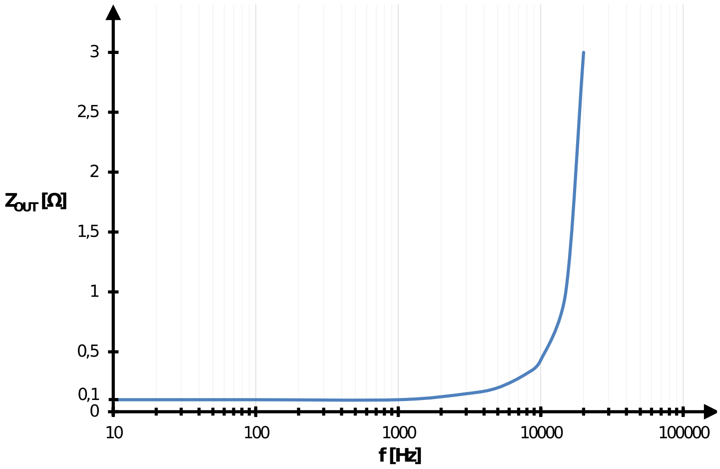



Figure 2.1: Output impedance vs. frequency

In order to define output impedance $R_{OUT}$ in a whole audio bandwidth, amplifier needs to be fed with a constant-amplitude continuous sine wave of an altering frequency. Output voltage needs to be measured with load connected $V_2$ as well as with a load disconnected $V_{20}$. Considering $R_{LOAD}$ as load impedance, amplifier's output impedance can be calculated according to the following formula:

$$R_{OUT} = R_{LOAD}\frac{V_{20}}{V_2} \tag{2.3}$$

## 2.4 Damping factor

Damping factor specification indicates how well a power amplifier suppresses resonances caused by mechanical motion of a loudspeaker cone. In many applications higher number is generally considered to be better. Therefore, negative feedback is set in order to lower effective output impedance of an amplifier and increase its damping factor. The endeavor to achieve very high value of damping factor may be unnecessary, because DC resistances of connecting cables usually nullify the benefits [1].

If amplifier's output impedance $R_{OUT}$ has already been measured and loudspeaker impedance $R_{LOAD}$ is known too, damping factor D can be acquired using formula:

$$D = \frac{R_{LOAD}}{R_{OUT}} \tag{2.4}$$

## 2.5 Frequency response

Frequency response determines how well an amplifier reproduces signal without any further boosting or attenuation of particular frequencies. Ideal shape of frequency response is flat within the range from 20 Hz to 20 kHz. Outside this range, frequencies should be attenuated to zero voltage level. In real world scenarios, ideal characteristic cannot be acquired, therefore a variation of ± 0.5 dB in an entire audio passband is acceptable. An ideal shape of frequency response is presented in the Figure 2.2.

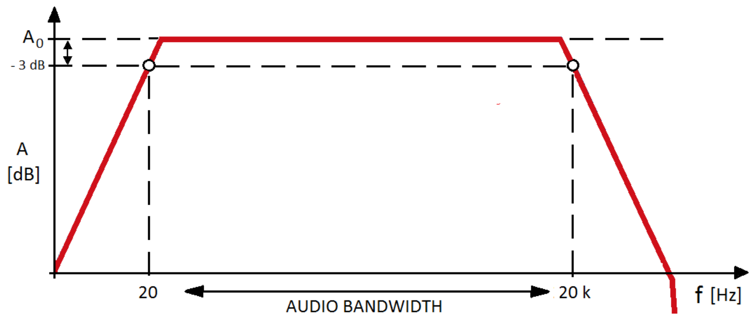



Figure 2.2: Ideal frequency response

In order to measure frequency response of an amplifier, sine wave signal of a constant amplitude but varying frequency must be fed in. The output signal is measured by TRMS voltmeter and voltage gain is then calculated by a given formula:

$$A = 20\log\frac{V_2}{V_1} \tag{2.5}$$

where A stands for amplifier's gain, $V_2$ and $V_1$ are voltages of output/input signal.

Finally, gain is calculated for different frequencies of an audio passband and plotted in a graph. Note that, in case of stereo amplifier both channels should be measured so as to ensure there is no variation between them [1].

## 2.6 Harmonic distortion

In order for an amplifier to generate harmonic distortion, its transfer characteristic needs to be bent. In practice, neither transistor nor valve amplifiers have perfectly linear transfer characteristic, see Figure 2.3, so they produce distortion. Whilst distortion introduced by transistor amplifiers is generally believed to degrade a quality of the sound, distortion of valve amplifiers accounts for the root of their fame. While amplifying an input signal, valves bring in plenty of second and fourth order harmonics what is perceived by a human hearing as a warmer, richer sound [4].

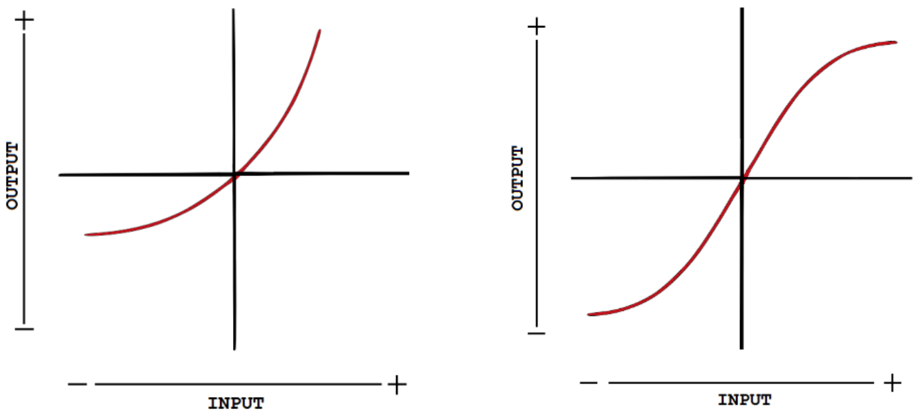



Figure 2.3: Distortion caused by even (a) and odd (b) order harmonics

Generally harmonic distortion measurements are held so as to objectively gauge a quality of reproduced signal. Initially, sine wave of constant amplitude and nominal 1 kHz frequency is fed into amplifier inputs. At the output, notch filter set on 1 kHz frequency is installed. Ideally, there would be no voltage measured at band stop filter output. Although, amplifier's harmonic distortion and nonzero level of noise in an output signal will cause TRMS voltmeter to measure a little voltage known as “Total Harmonic Distortion + Noise“ [9].

# 3 POWER CLASSES

This section will be devoted to most common power classes used in audio amplifiers. Power classes basically differentiate amplifier output stages according to working principle they utilize in order to amplify an audio signal. The choice of a power class will always represent a compromise between circuit's performance parameters. There are few other power classes that are not covered in this section, but their working principle is more-or-less the same.

## 3.1 Class-A

Design of Class-A power amplifiers dates back to the very beginning of sound-reproduction history mainly because of modest requirements it imposed on components used. Bias point of the circuit is placed right in the middle of linear part of transfer characteristic, see Figure 3.1, so that an output current is constantly flowing through all the output devices for an entire cycle. No matter current value of input signal, output devices will never become fully turned off and so related nonlinearities, particularly crossover distortion, will never be generated.

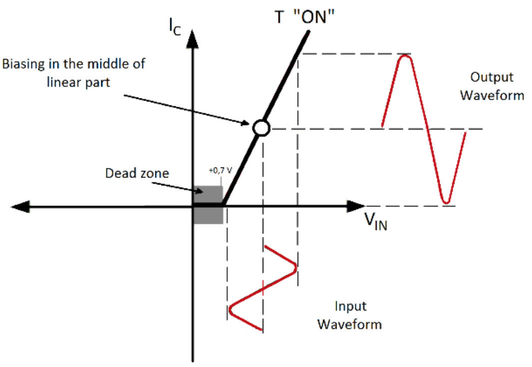



Figure 3.1: Class-A transfer characteristic

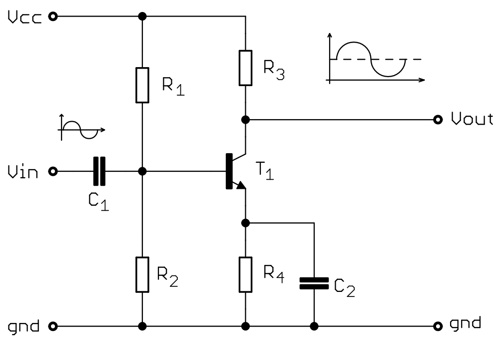



Figure 3.2: Basic Class-A amplifier

Working principle can be explained on a very basic circuit presented in the Figure 3.2. Resistors $R_1$ and $R_2$ create a robust voltage divider, which precisely sets bias point of transistor $T_1$. It is recommended to choose divider's biasing current at least 10 times larger than input current flowing to transistor's base. Regarding the load line, bias point will be placed in the center, thus quiescent voltage on collector will match half of the supply voltage. Resistor $R_3$ represents the load. Resistor $R_4$ is usually chosen from one-tenth to one-third of $R_3$ and introduces negative feedback. Since the resistor $R_4$ significantly influences final circuit gain, capacitor $C_2$ must be used. It introduces a bypass path for AC signal, thus negative impact of resistor $R_4$ on amplifier's gain can be omitted. Capacitor $C_2$ should be large enough to be considered as a short for frequencies as low as 20 Hz.

Class-A power amplifiers, besides giving the best possible distortion performance of all amplifier classes, suffer from very poor efficiency. Nowadays they are only employed in high fidelity valve amplifiers and few mid-power transistor amplifiers where sound reproduction quality is at first place. Despite, Class-A amplifiers widely serve as building blocks of many other circuits, such as voltage pre-amps of Class-AB or Class-D amplifiers. In these applications power loss dissipated by them is negligible compared to the power of output signal.

Theoretically highest efficiency achievable by Class-A amplifiers is 25 % in case of resistive load and 50 % if the load is replaced by a transformer. However, in practice efficiency of these amplifiers remains at around 5-20 %. Total harmonic distortion usually does not exceed 0.1 % [1].

## 3.2 Class-B

Class-B power amplifiers came into production so as to satisfy the demand for higher efficiency. These amplifiers work in an opposite way to Class-A amplifiers. Bias point of the circuit is placed at the beginning of transfer characteristic, see Figure 3.4, and thus output current flows through particular output devices only during associated half of the sinusoidal cycle. In case of no input signal, all output devices remain turned off. Therefore, an audio input signal results in an iterative switching of active components between on and off state. This process is accompanied by a huge crossover distortion and switch-off phenomena, which negatively affect final sound quality. Practical implementation of Class-B amplifier is shown in the Figure 3.3.

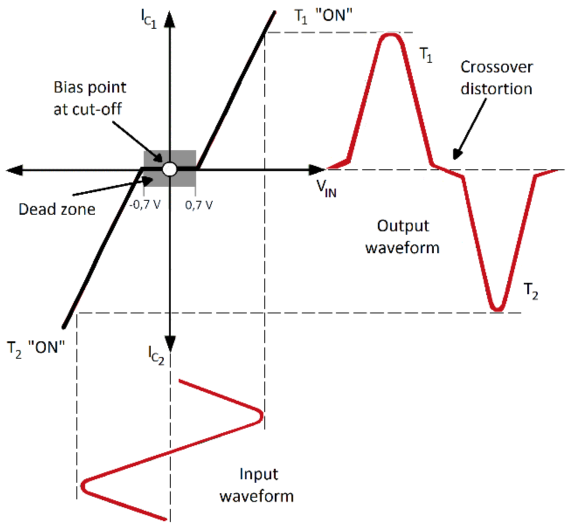



Figure 3.4: Class-B transfer characteristic

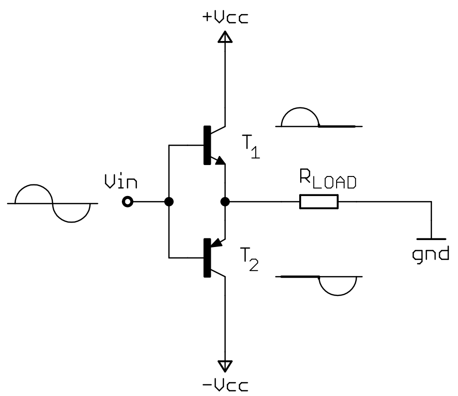



Figure 3.3: Class-B basic circuit

Mentioned crossover phenomena along with beta-mismatch in the output devices are major causes of large total harmonic distortion of output sound, which can rise up to units of per-cents. The only advantage of Class-B amplifiers is a relatively high efficiency, around 78.5 % at most [1].

## 3.3 Class-AB

Class-AB power amplifiers belong to most wide-spread classes in consumer electronics. The main reason for it is that they combine virtues of both Class-A and Class-B amplifiers. Efficiency is greatly enhanced compared to Class-A amplifiers and harsh distortion introduced by pure Class-B amplifiers is significantly reduced too. Theoretically speaking, this is done by placing bias point of typical Class-B amplifier at the lower bound of linear part of transfer characteristic. In practice, a little voltage offset is brought between base and emitter of both output transistors, which prevents them from completely turning off. A small amount of quiescent current $I_q$, from 10 mA to 100 mA, is usually sufficient [1].

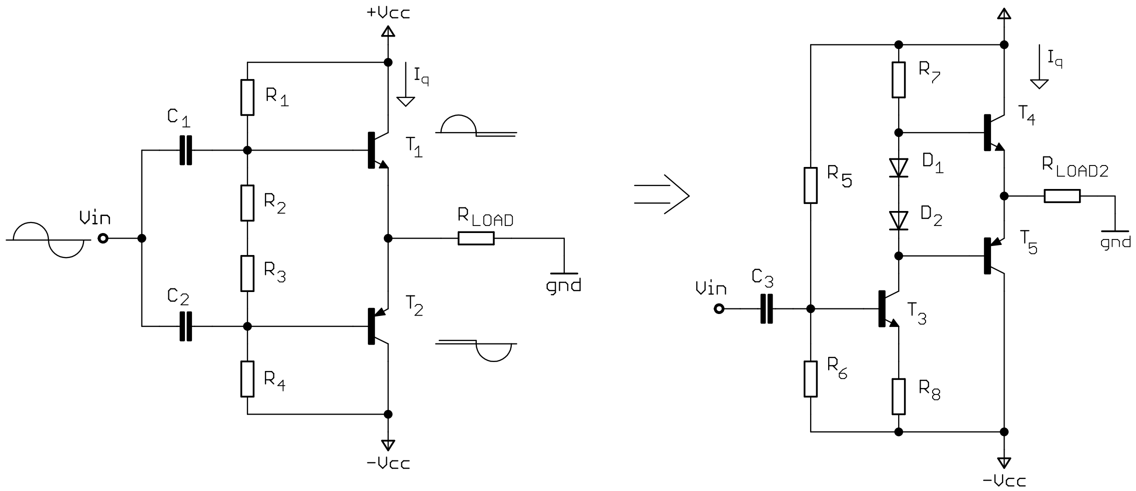



Figure 3.5: Class-AB amplifier, resistor bias (a) and diode bias (b)

For a comparison of different approaches to Class-AB power output design, two basic circuits were chosen, see Figure 3.5. In both cases voltage offset between base and emitter of output transistors will be tried to achieve. In the first one, voltage offset is represented by a voltage drop generated across resistors $R_2$ and $R_3$, through which biasing current is flowing. It should be noted that behavior of entire circuit is based on this biasing current. Even a little fluctuation in power supply voltage will result in total alternation of circuit's harmonic distortion and efficiency. Other approach is presented in figure b. The working principle remains, but this time a diode (or two diodes in series) replaced resistors $R_2$ and $R_3$. If they are chosen to perfectly match transfer characteristics of output transistors, final circuit will be much less liable to alter its parameters in case of power supply voltage deviation.

## 3.4 Class-D

Class-D power amplifiers belong to most modern and wide-spread audio amplifiers of this time. In this design all active devices are always either fully on or fully off, which greatly reduces power losses. Therefore, efficiency can easily exceed 80 % and rise up to 95 %. Working principle is shown in the Figure 3.6. The input audio signal is compared with a fast switching triangle wave. At comparator's output modulated square wave is generated. Square wave drives power output FETs (field-effect transistor), which are followed by a low pass filter. The purpose of this filter is to attenuate all frequencies higher than audible sound. For further derail refer to a chapter “CLASS-D AMPLIFIER”.

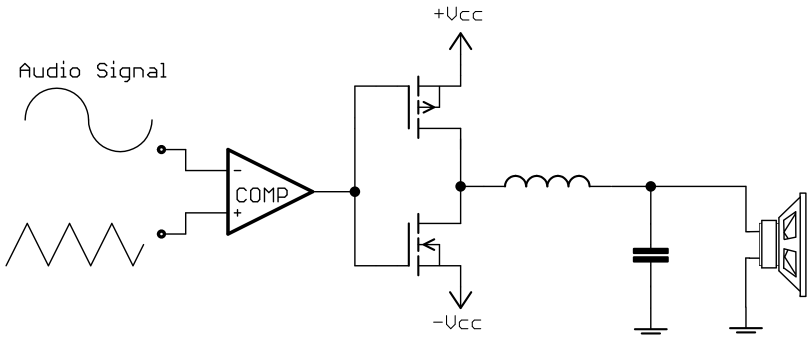



Figure 3.6: Basic block diagram of a Class-D amplifier

In “classic” power class designs amplifier efficiency η almost linearly rises up with an increasing power output. At amplifier maximum power output, efficiency achieves its highest possible value. On the contrary, efficiency of Class-D amplifiers reaches its maximum value once a power output has crossed a relatively low threshold value. See Figure 3.7 for a comparison [12].

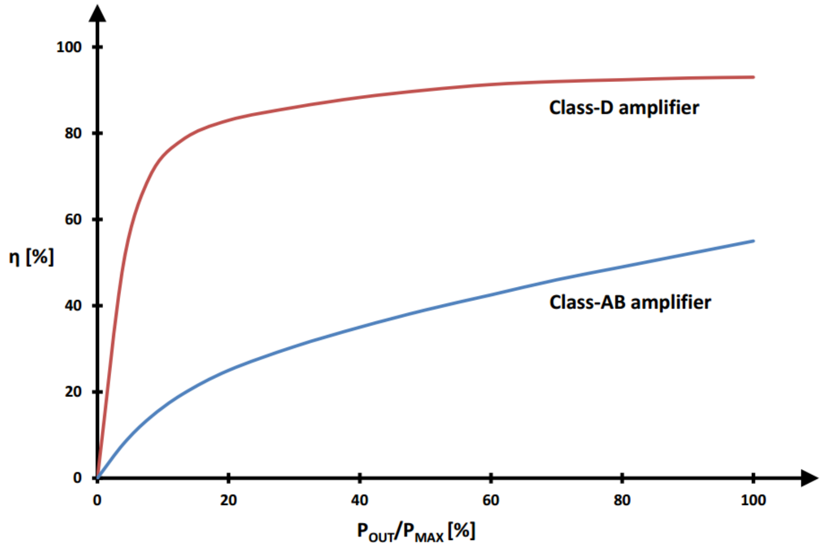



Figure 3.7: Comparison of Class-D and Class-AB amplifier efficiency

# 4 CLASS-D AMPLIFIER

Initial steps to the design of Class-D audio amplifier were taken in the 1950s. Although the concepts were completed at that time, construction of the amplifier was not launched, because combination of high switching frequencies and tube output transformers did not seem to have any future. Bipolar technology neither presented a solution. Bipolar transistors of sustainable power-handling capacity were not able to switch such high frequencies required. Later on, with an arrival of fast switching power FETs, Class-D amplifiers could finally spread their growth.

For a basic overview of Class-D amplifiers please refer to the previous chapter “Class-D“. Following pages will be devoted to a deeper insight into particular building blocks of Class-D amplifier. However, this chapter is not intended to cover all the nuances connected with this type of an amplifier, fundamental principles will be properly explained. Typical block diagram of Class-D amplifier is presented in the Figure 4.1 [6].

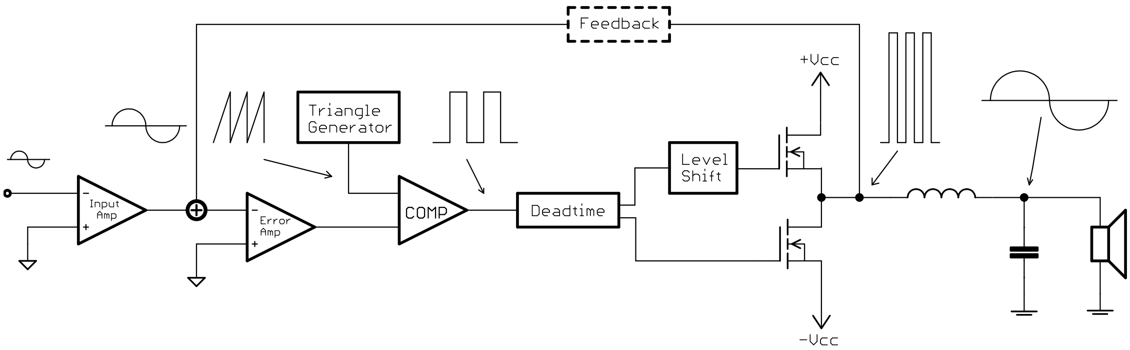



Figure 4.1: Block diagram of Class-D amplifier

## 4.1 Input amplifier

Input analog signal is supplied to an input amplifier through a pair of blocking capacitors as shown in Figure 4.2. The purport of an input amplifier is to prepare the signal for the following stages. Initially, any external DC bias contained in the signal is removed and then the signal is amplified to a reference voltage level. External capacitor with an internal resistor of an input amplifier serve as a filter too, which sets low frequency corner [7].

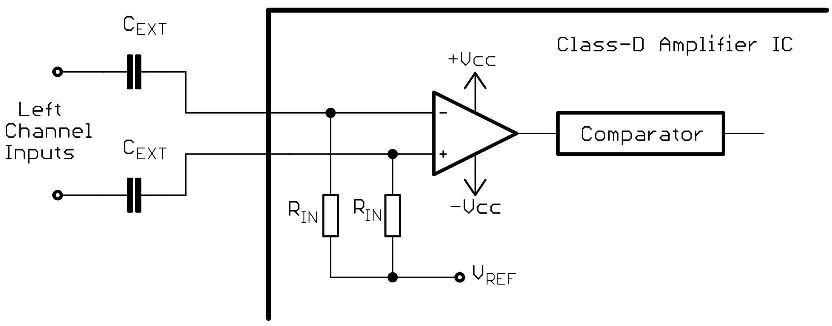



Figure 4.2: Input circuits of Class-D amplifier

## 4.2 Triangle wave generator

Triangle wave generator is an essential part to each Class-D audio amplifier. Its simplified version is shown in the Figure 4.3. The purpose of circuit is to create a ramp function switching between positive and negative slope over and over again. Triangle generator operates on a so-called switching frequency, which needs to be at least twice the value of maximum frequency introduced by an input analog signal. Violation of this condition results in an irreversible distortion of output signal. Thus is real world scenarios, switching frequency is always being chosen appropriately larger [5].

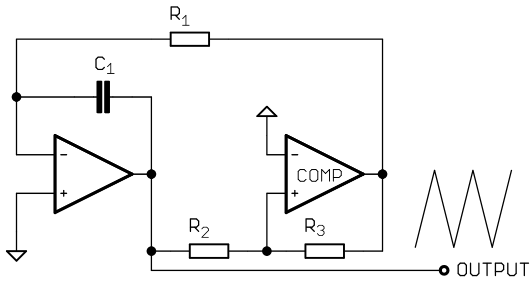



Figure 4.3: Triangle wave generator

## 4.3 Comparator

The purpose of a comparator is to compare an input audio signal with a referential triangle wave. If an audio input is greater than current value of a triangle wave, the output of comparator is driven high. In an inverse situation, the output of comparator goes low. This way can be audio signal modulated into PWM.

Long-time experience led designers to implement two comparators in a single channel so as to prevent from “shoot through” effect. It occurs as a consequence of imprecise timing of output devices. In case, when devices are switching between on and off states, there is an unwanted time gap during which both devices conduct. Large current pulse flows through them what negatively influences output signal as well as devices' life. The idea of two comparators, one for each output device, provides with an elegant solution. It introduces an addition of asymmetrical subtle delays to output square waves so that an “ON-ON” state will never occur [1].

## 4.4 Feedback

Regarding feedback Class-D amplifiers can be divided into two separate groups. Open-loop devices, which do not utilize any feedback at all and close-loop devices with a negative feedback installed. The advantage of an open-loop design is a great stability which, though, comes at price of minimal rejection of supply voltage deviations. This drawback can only be resolved by feeding output signal back to the input via negative feedback. Supply fluctuations are then handled and corrected by the control loop. Very basic example of such feedback is presented in the Figure 4.4. Error amp acts as a low-pass filter with a pole frequency greater than the highest frequency of an input signal, but lower than the switching frequency. Because of a large gain at dc, error amp nullifies all dc offsets at the output [5].

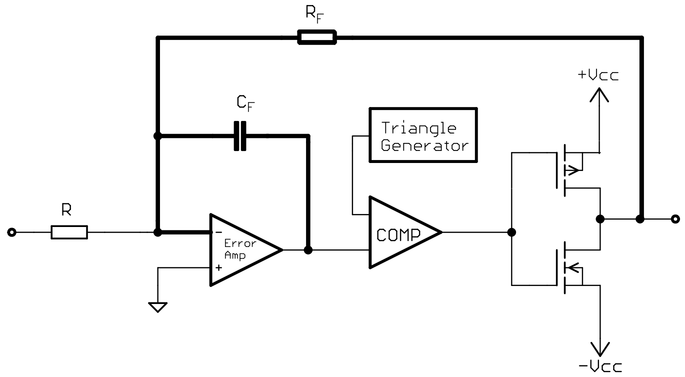



Figure 4.4: Feedback in Class-D amplifier

Generally, noise-shaping type of feedback is utilized. This way can be in-band noise caused by the non-linearities of the pulse-width modulator significantly attenuated [6].

## 4.5 Output circuits

There are two available configurations how amplifier's output devices can drive the loudspeaker. SE (single ended) configuration was presented in figures earlier, for instance Figure 4.1 since it is less complex and easier to understand. Common node of two complementary output devices drives load directly through a low-pass filter and DC blocking capacitor.

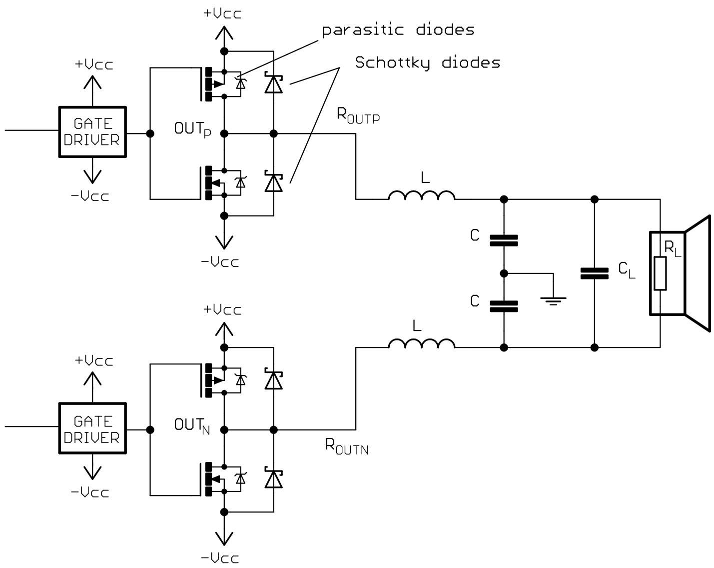



Figure 4.5: Output circuits of Class-D amplifier

Many Class-D amplifiers embedded into an integrated form work in BTL (bridge-tied-load) configuration, see Figure 4.5. It requires a pair of complementary output devices feeding audio signal of reversed polarity to the load. This way can be voltage swing doubled compared to single ended configuration and amplifier's dynamic resistance $R_{DSon}$ (drain-source on resistance) significantly reduced while boosting efficiency. Though, damping factor is halved. A square-wave output signal may be fed directly to a loudspeaker provided that a loudspeaker is inductive at the amplifier's switching frequency (for more information on this approach seek [10]). However, in real world scenarios this approach is almost always omitted and square-wave signal is sent to a filter beforehand [7].

Usage of external Schottky diodes is optional, but highly recommended. The diodes significantly cut down power losses during so called non-overlap time when neither of output transistors is driving OUT pin. At first, let's explain the behavior of parasitic diodes associated with a typical MOSFET (metal-oxide-semiconductor field-effect transistor) transistor structure. In case when the voltage level at the OUT pin reaches value 0.7 V below –Vcc (negative power supply voltage), the "low side" parasitic diode becomes forward biased and turns on. Thus, an unwanted charge induced on an OUT pin can be safely driven away. When the "high side" transistor turns on, the voltage level at OUT pin will boost up to +Vcc value (positive power supply voltage) that will make a diode to reversely bias. However, the nature of a parasitic diode is responsible for its long reverse recovery time what causes a current to flow through it longer than necessary and worsens amplifier performance. A similar scenario occurs when the filter coil induces a current that drives the OUT pin 0.7 V above +Vcc value. Therefore, due to faster recovery times Schottky diodes are employed. Not only less current is wasted, an unwanted charge is driven away earlier too, because of lower, 0.3 V, forward bias voltage [2].

## 4.6 Low-pass filter

By the nature of Class-D amplifier, output signal always comprises audible signal and unwanted high frequency components. The purpose of a low pass filter is to separate these two spectral zones and ideally attenuate to zero all the unwanted higher frequency components. Generally, low pass filters are built out of passive frequency dependent dividers. So as to reduce negative impact of filter's equivalent series resistance, achieve highest filter order while keeping retail price low, LC filters are preferred over other types. The output filters are usually designed using Butterworth approximation. There are two reasons for it straightway: it gives the best compromise between phase response and attenuation and it requires few components only. Normalized amplitude response of Butterworth filter is presented in Figure 4.6 [2].

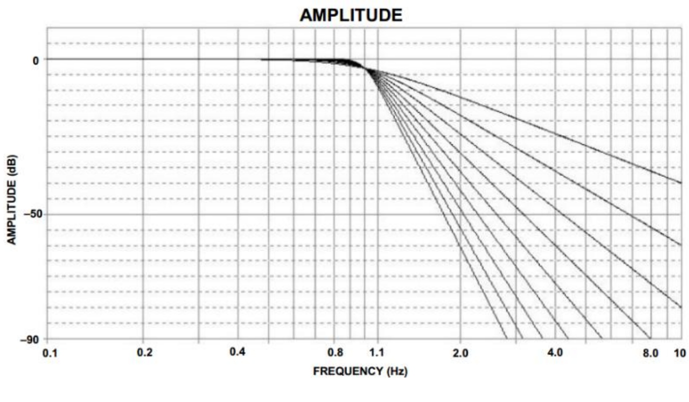



Figure 4.6: Normalized amplitude response of Butterworth filter [2]

## 4.7 Major causes of imperfection

Generally, primary reason for the nonlinearity in Class-D amplifiers is caused by a switching timing error in a gate signal. Even few tens of nanoseconds can introduce more than 1 % of THD (Total Harmonic Distortion). Thus, precise switching should always be of a main concern. Another source of imperfection are parasitic components which cause ringing on transient edges. Also notice that gain of Class-D amplifier is directly proportional to a power supply voltage. Any fluctuation in a bus voltage will become a cause of severe distortion. Choice of an output filter inductor should be done carefully too. If its current ratings are not high enough, inductor will not avoid magnetic saturation during an operation and will appear to PWM output as a short instead of an open circuit. Shielding of inductors will also help reduce crosstalk and prevent from electro-magnetic interference. Some of the mentioned effects are depicted in the Figure 4.7 [6].

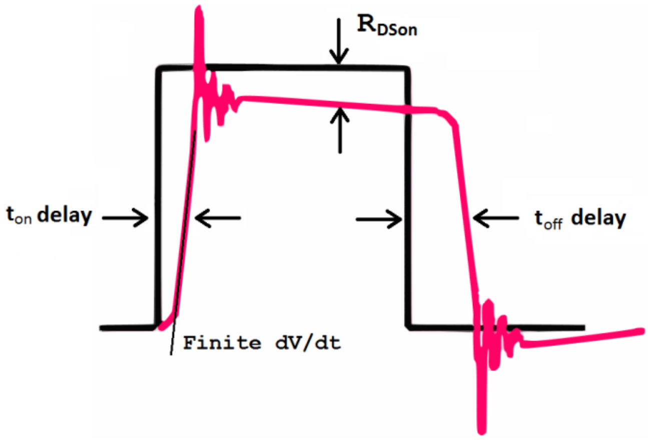



Figure 4.7: Distortion in Class-D amplifiers

# 5 POWER SUPPLIES

Each electronic circuit is in need of power supply in order to operate. Though, this part of any system design is often being neglected. When building an amplifier, especially of a “digital“ type, power supply represents one of the most essential subsystems as it directly influences purity of output signal. Power supply voltage needs to keep its AC component as little as possible for optimum amplifier’s performance.

There are three different ways to choose from when designing power supply for an amplifier. The simplest and most cost-effective one is a concept of transformer, rectifier and reservoir capacitor. In case better ripple performance is pursued, one can go for a linear regulated power supply. Switch-mode power supplies represent the last group and are generally utilized in system with very high output power requirements. For a little more information on each type, seek following pages.

## 5.1 Transformer-rectifier-capacitor

This technology represents an easiest and quickest way, how to supply power to an amplifier. Mains voltage 230 V is fed into primary winding of a transformer. On a secondary winding an output voltage appears, whose value is given by a ratio between primary and secondary winding turns. Output sine wave is rectified, so it only consists a voltage of one polarity and then filtered by reservoir capacitor, so its AC component is nullified. Working principle is depicted in the Figure 5.1.

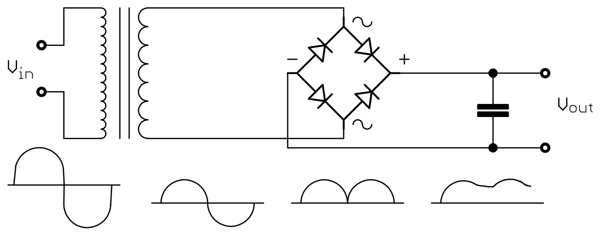



Figure 5.1: Transformer-rectifier-capacitor working principle

Advantages of the given configuration are as follows. It is simple with very few components needed, what results in a great reliability and longevity. Cheap price and almost no high-frequency switching interference only add up to its virtues. Thus the configuration makes the best choice for limited-budget, basic applications.

The simplicity of design comes at price of significant ripple on a DC output, what worsens amplifier power supply reject ratio. Though, when taken care of, output hum levels can be safely attenuated. Not-presence of switching devices may temptingly imply no high-frequency emissions. The opposite is true - diodes of the bridge rectifier produce bursts of radio-frequency components at a repetition rate of 100 Hz as they switch off. This problem is made worse with an increased current demand [1].

## 5.2 Switch-mode power supply

Switch-mode power supply is a must in case of high power requirements posed by an amplifier. Otherwise, in low and mid-power applications, it is almost always omitted as it brings in incredibly lot of work to entire production process of an amplifier.

To build most basic step-down switcher circuit, only one transistor, diode, inductor and a capacitor is required, see Figure 5.2. When a transistor $T_1$ is turned on, diode $D_1$ becomes reversely biased and the input voltage $V_{in}$ feeds the current to the load through the inductor coil. Input current causes an inductor to create a magnetic field. Once the transistor $T_1$ becomes switched off, input voltage is no longer present to load. Magnetic field generated around the inductor coil collapses, what sparks off an induction of a reverse voltage across the coil. Diode $D_1$ becomes forward biased and an energy stored in magnetic field feeds the current to the load in the same direction. Current returns back through the diode. Practical switch-mode power supplies, though, always implement control section that requires additional components such as oscillators, voltage reference circuits, error amplifiers, comparators and so on. Most sophisticated designs involve current limiters, shutdown timers and other optional features too.

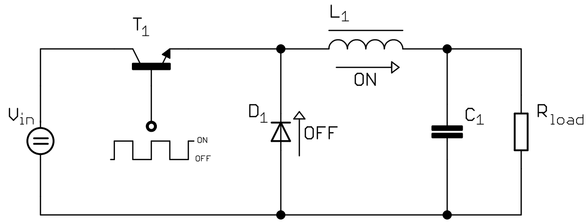



Figure 5.2: Basic switch-mode buck converter topology

Besides giving the best possible output power performance, voltage ripple can be considerably pulled down compared to unregulated power supplies too. The technology does not require any heavy mains transformer, thus dimensions of such power supply can achieve unbelievably small values. Devices allow both boost and buck operation, are light-weighted and very efficient.

However there is always the other side of the coin. Due to their working principle, switch-mode power supplies are prolific sources of high-frequency interference. Once this interference infiltrates into an audio signal, an unbelievably difficult task is posed in order to eradicate it out. Actual design is a very complex matter that usually requires specialists. Trying to build such supply without inadequate experience may result in hours of work and device's faulty performance [2].

## 5.3 Linear regulated power supply

Linear voltage IC (integrated circuit) regulators have served as standard building blocks for a very long time. The most explanatory reason for it is the fact that they provide output voltage with lowest noise characteristic possible. An amplifier taking advantage of such supply gives absolutely consistent power output no matter mains voltage deviations. Further on, overall simplicity and little parts count requirements make linear voltage regulators better solution for a vast amount of applications compared to switch-mode power supplies. The hugest and well-known drawback degrading overall “quality” of these power supplies are relatively high power losses.

To create a better picture of a linear regulator efficiency, refer to Figure 5.3. It demonstrates how regulator's efficiency varies throughout the lifetime of three 1.5 V supply batteries at constant output power load of 100 mW. When batteries are fully charged, regulator's efficiency is at its lowest value, around 70 %. As batteries age, their output voltage decreases, what results in lower regulator's dropout voltage and efficiency raises. At certain point, batteries' output voltage is too low, thus a regulator ceases operation and efficiency reaches 100 %. In total, when considering overall battery energy used to power the load, average regulator's efficiency is around 70 % [2].

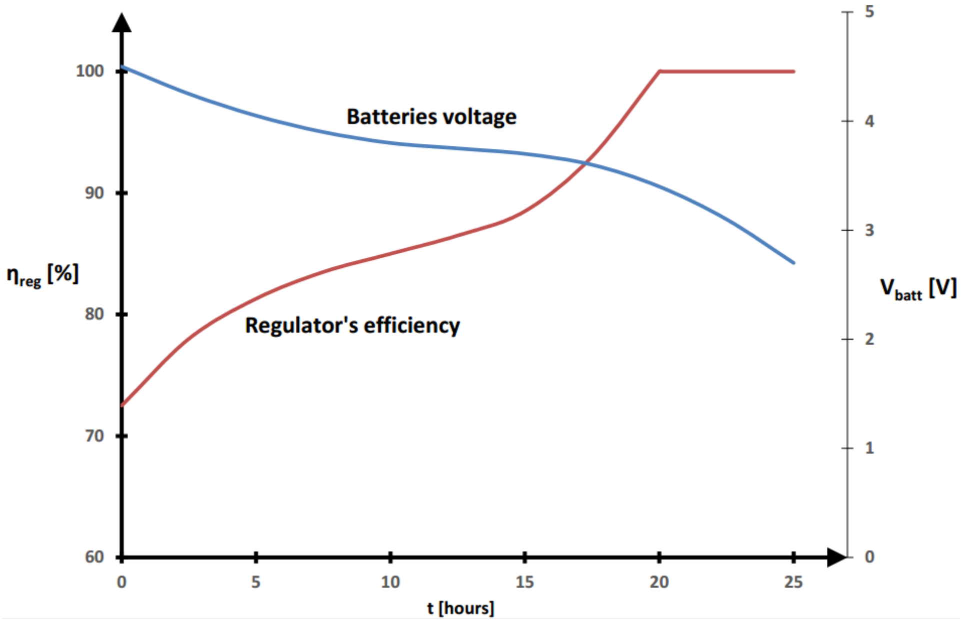



Figure 5.3: Efficiency of a linear regulator

### 5.3.1 Working principle

Probably the simplest way to think of the linear regulator is to picture an adjustable series resistor, see Figure 5.4. It will dynamically alter its resistance in case of an input voltage variation so as to keep output voltage across the load constant. It now becomes clear, that if half of the supply voltage is dropped across the load, other half will drop across the series resistor and will dissipate in power losses. This is the reason for device's relatively low efficiency.

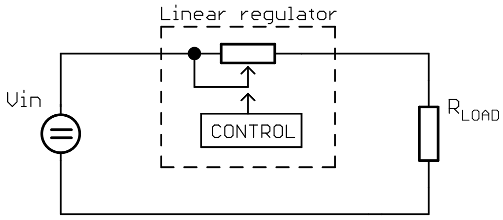



Figure 5.4: Linear regulator working principle

Though, in real world designs an adjustable series resistor is never used as it would require to find a way how to dynamically control device's resistance. Instead, a pass device comprised of active and passive components is used. For the sake of simplicity, let's suppose one transistor only as a pass device, see Figure 5.5. In order to control its dynamic resistance, i.e. voltage drop across C and E, a dedicated feedback loop has to be established. Conceptually, DC voltage on regulator's output is sensed by a sampling network made of resistors $R_A$ and $R_B$. Output of the voltage divider is brought to an error amplifier that compares it with a voltage reference block. Voltage reference purports to generate a stable voltage level, which is typically a band gap based voltage, around 1.2 V. An error amplifier controls a current amp that drives a pass device. Based on an input signal, pass device can raise or decrease regulator's output voltage so as to keep it constant no matter the load powered [2].

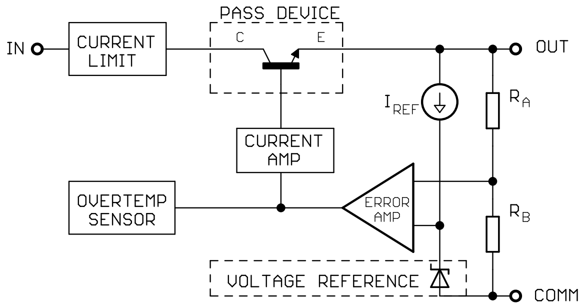



Figure 5.5: Linear regulator block diagram

## 5.3.2 Pass devices

Pass devices are one of the most notable contributors to final regulator's performance, though, the discussion has not treated them so far. Following few lines will provide a closer look at alternate forms and corresponding virtues/drawbacks of these devices. Attention will be paid mostly to dropout voltage, maximum output current and a bandwidth.

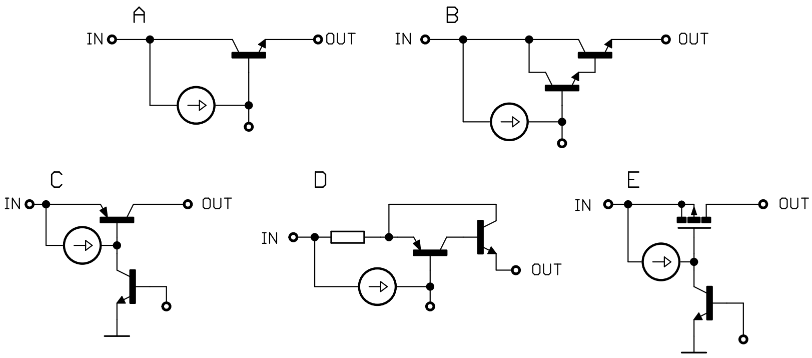



Figure 5.6: Variations of pass devices

Schematic representations of different pass devices are shown in the Figure 5.6. The first two, A and B, work as emitter followers and thus, share the same attributes. Their greatest advantages are large bandwidth and a relatively low output impedance, thanks to which they are immune to capacitor loading too. Further on, a Darlington configuration, schematic B, is capable of providing more than 1 A of output current, though at the expense of higher value of dropout voltage, around 2 V. Circuits C, D and E are typical for high output impedance, because of which they require an output capacitor for a stable operation. The fact, that these output devices are sensitive to compensation cap needs to be fully understood by their users. One should always carefully choose specific size and type of the output cap so as to keep regulator stable with respect to both temperature and time. On the other hand, circuits C, D and E stand out for relatively low dropout voltage, thanks to which they are very often used in low-dropout voltage regulators, known as "LDO" devices [2].

### 5.3.3 Optional blocks

A vast majority of linear voltage regulators will provide themselves with some means of protection. Current limiting and over-temperature sensing circuits are generally considered as the most important ones as they protect pass devices against irreversible failures. Current sensing is almost always implemented by a series resistor across which high output current establishes critical voltage drop that opens a sensing transistor. This transistor, in turn, shuts down a pass device. Sensing of excessive temperature is usually done by means of $V_{BE}$-based sensor monitoring the temperature of a chip. When a die temperature rises above the trigger level, approximately 150 °C, sensor output voltage crosses fixed reference voltage which causes the comparator to switch to off state and shut down a pass device. Some linear regulators offer an error flag output pin used to warn of recognized shut-downs [2].

### 5.3.4 Practical application

It would be a sin not to mention probably the most famous three-terminal adjustable voltage regulator LM317. Its simplified schematic is presented in the Figure 5.7. Transistors $T_1$ and $T_2$ serve as current mirror of Brokaw band gap reference cell formed also by transistors $T_3$ and $T_4$. This reference keeps a constant voltage of 1.2 V between output terminals OUT and ADJ. Thus, a change in value of external scale resistor $R_B$ causes an output voltage to be adjusted so that could 1.2 V difference remain intact. Transistor $T_5$ functions as a buffer which drives an output pass device. Darlington pair is used, thus an output current draw of 1.5 A is allowed [2].

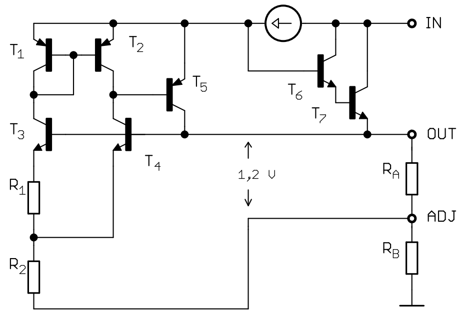



Figure 5.7: Simplified schematic of LM317

# 6 DESIGN

The aim of following subchapters is to explain decisions made during the design process of the device. The ordering of subchapters was chosen to match chronological progress of the design, that is from the most general steps to the most specific ones. At this place it is important to mention fundamental ideas that will be taken into consideration while solving particular design problems. The device to be constructed will serve educational purposes. That means, it will be in contact with students (people who, naturally, do not know how to operate it) on regular basis. Because of that, it needs to be extremely robust and foolproof. This will be achieved by use of components of higher power handling capacity and easy-to-replace in case of failure, and by implementing different protections. Though, it does not mean SMD (surface mount device) components will not be utilized at all. Parts of the PCB (printed circuit board) working with higher frequencies will use SMD components too, otherwise the device would most probably malfunction. The last key requirement imposed on the device is demonstrativeness. Some choices regarding device's design will be intentionally made not perfect. Thus, the device will not become a quality audio amplifier. In exchange, it will show how parasitic effects influence the shape of PWM signal, what output filter actually does in order to turn PWM wave into filtered out audio signal and other phenomena mentioned later.

## 6.1 Single-ended vs. Bridge-tied-load

The difference between single-ended output and bridge-tied-load can be found in a theoretical part of the work, particularly "Output circuits" section. In order to demonstrate this difference, and hence fulfill one of the key requirement stated in an introductory part of the chapter, the device will be fitted with an external switch $S_1$ that will allow to change configuration of output circuits, see Figure 6.1. Note that, the difference between the two configurations needs to be observed while driving the same load. This explains use of the switch $S_2$.

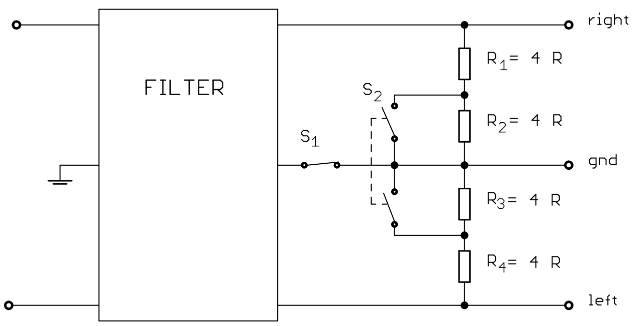



Figure 6.1: Switching between SE and BTL configuration

In order to utilize SE configuration, $S_1$ must be closed and $S_2$ opened. Then, resistors $R_2$ and $R_3$ are not shorted and total load driven by a channel equals $R_1 + R_2$. Oppositely, once $S_1$ becomes opened and $S_2$ closed, true BTL configuration is utilized. Resistors $R_2$ and $R_3$ are shorted and total load driven by "tied" channels equals $R_1 + R_4$. Whichever configuration is utilized, 8 Ω load is always driven.

In order to be able to experimentally measure device's output resistance, the device must be able to somehow "turn on" and "turn off" the load. For output resistance measurement seek chapter "Output impedance". In practice turn on/turn off operation will be handled by switch $S_2$. Note that, switches $S_1$ and $S_2$ in previous figure were tied together, so they are both considered as one switch $S_1$. Final output configuration is presented in Figure 6.2.

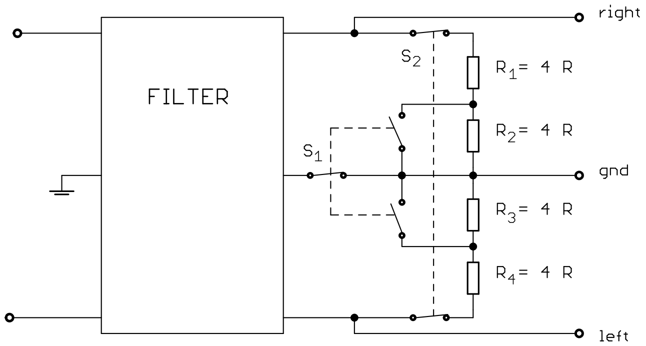



Figure 6.2: OPEN/LOADED switch

## 6.2 Output filter design

The importance of output filter is explained in a theoretical part of the work, e.g. in "Low-pass filter" chapter. To demonstrate this crucial importance, i.e. to demonstrate consequences of output filter order on an output signal, the device needs to somehow implement a "variable" filter. One elegant solution is presented in the Figure 6.3. It presents a system of tied switches, which short particular reactive or resistive components of a universal filter and that way turn it into a filter of required order.

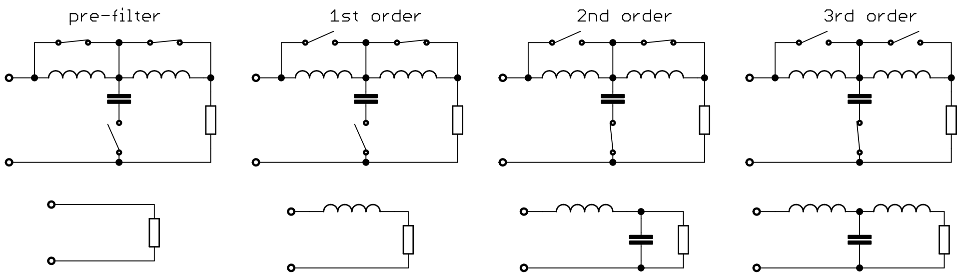



Figure 6.3: Variable-order filter

Although this solution requires very few parts, allows incrementing filter order by one and presents very sophisticated idea, it would be too difficult to build. First of all, despite many numeric calculations, each filter configuration would work with different cutoff frequency. Secondly, over the entire chassis would be spread many wires leading to control switches, which would not only look unprofessionally, but also present unwanted inductive components. And lastly, these wires could get burnt by power components such as driver FETs and load resistors.

Because of all the complications mentioned, output filter order will not be altered via switch. The design will rather focus on “classic” LC ladder filters generally recommended for Class-D audio amplifiers. The filter of 5th order was chosen since it offers four probe points, where could be a shape of an output signal observed - pre-filtered, after 2nd order, after 4th order and after 5th order. That must be enough for a student to create a notion of an influence of output filter order on a PWM-modulated sinewave signal.

The problem: do the filter's components need to change in value, when switching to SE configuration loaded with 8 Ω from BTL configuration loaded with 8 Ω? By seeking technical literature, e.g. [8], the answer can be easily found. Between SE and BTL exists an equivalence, see Figure 6.4, which states that in order for SE configuration to work properly with output filter designed for BTL configuration and load $R_{LOAD}$, SE's load needs to cut in half, that is $R_{LOAD}/2$. This means, if it is switched from 8 Ω BTL to 8 Ω SE and filter components are left as they are, filter parameters will notably change. Particularly, cutoff frequency will drift away, frequency response and phase response will become undesirably curved and so on. If the purpose of the thesis was to design high quality Class-D audio amplifier, the filter would need to be customized to work perfectly for both configurations. However, the device will serve as an educational tool, so leaving this problem intentionally unresolved can help students more easily understand the influence of load resistance on filter’s parameters.

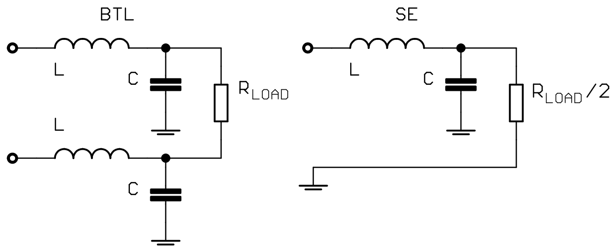



Figure 6.4: Equivalence between SE and BTL

To decide which configuration will the filter be designed for, performance measurements ought to be considered first. Once the device is built, it will serve to demonstrate frequency response. This measurement is usually done by measuring input/output voltage of one channel and thus the filter should be designed for SE 8 Ω. Alongside, the device will serve to demonstrate BTL configuration, so the filter ought to be designed for BTL 8 Ω. However, all performance measurements of BTL configuration will be held at 1 kHz frequency and what happens at other frequencies is not going to be evaluated at any point. Alternatively, measurements at other frequencies could demonstrate negative impact of an inappropriate load resistance. Based on these postulates, a filter design will be accurately tuned for SE 8 Ω configuration in an entire audio bandwidth. The filter will also work in BTL 8 Ω configuration, but with least attenuation only at 1 kHz. Although, output drivers have not been yet selected, for further calculations 100 mΩ of $R_{DSon}$ will be assumed.

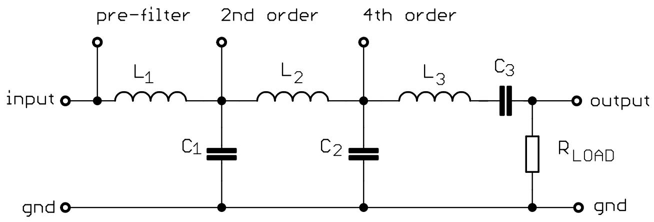



Figure 6.5: 5th order LC ladder filter

As a first approach to the filter design, 5th order of the filter, Butterworth approximation and 50 kHz cutoff frequency was chosen. Actual calculations were done using Filter Solutions program. Final filter's topology per one channel is presented in Figure 6.5.

Use of DC-blocking capacitor may seem redundant for the application as the device is not going to drive any sensitive speaker. Despite, it must be taken into account that while measuring frequency response of SE configuration, output signal cannot comprise any DC voltage. Alternatively it could, but the measurement would imply a systematic error, which would need to be corrected each time the measurement had proceeded.

Next figure, Figure 6.6, presents frequency response simulation of a filter prototype. The filter was designed primarily for SE 8 Ω configuration and because of that filter's passband is perfectly flat. It can be noticed that after cutoff frequency at the output of 2nd, 4th, 5th filter's order, voltage transfer characteristics falls down at 40 dB/dec, 80 dB/dec and 100 dB/dec rate, respectively. Since the load is coupled by a large capacitor, low frequency corner is pushed down as low as 10 Hz.

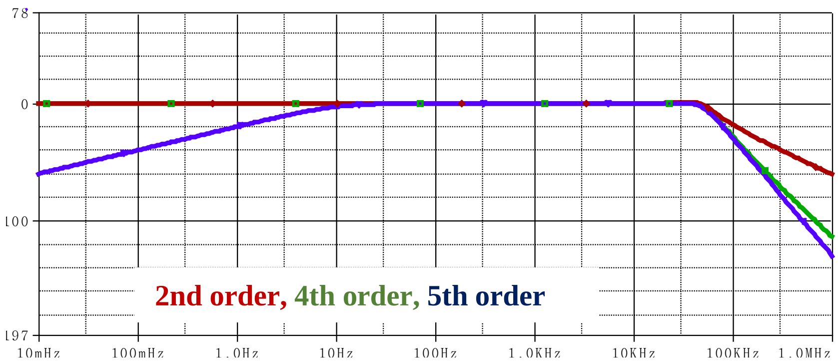



Figure 6.6: Frequency response simulation in SE configuration

Unfortunately, after such filter had been built and tested with an audio amplifying chip, it turned out that output signal is perfectly filtered of any unwanted interference already at the “2nd order” filter's output. The test ended up with an observation, that all probe points of the filter show the same, well filtered output sine wave. That is wrong, because filter ought to show markedly distorted sine wave at “2nd order” output, almost perfectly filtered out sine wave at “4th order” output and totally filtered sine wave at “5th order” output.

On second thoughts, this observation of filter's behavior is not that surprising. The filter consists of partial filters designed for same cutoff frequency, which is set too low. The amplifying chip samples input signal at 250 kHz, thus unwanted spectral components start at this frequency and go up to units of MHz. Due to this fact, even 2nd order filter with cutoff frequency of 50 kHz and little stop-band attenuation can nullify such “high frequency” products of PWM modulation.

In order for the filter to show desired signals, side by side with rising filter’s order, its cutoff frequency has to fall down. Alternatively it would only suffice to create a filter with adjustable cutoff frequency, though, the requirements of the thesis clearly state to build a filter of higher order.

The ideal frequency response of such filter would look like the one as presented in Figure 6.7

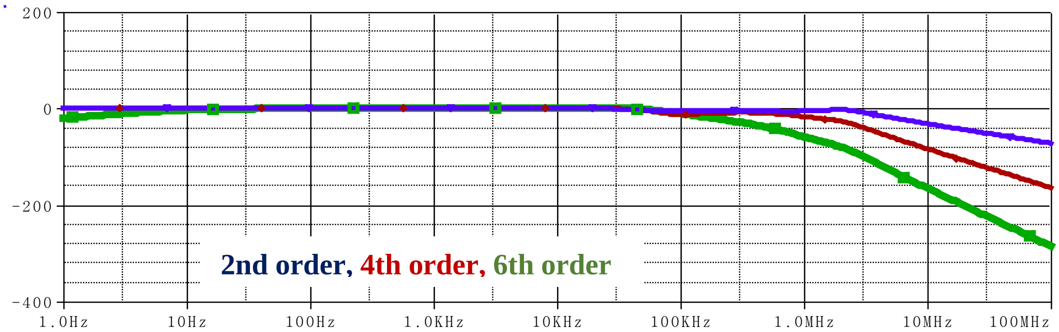



Figure 6.7: Frequency response simulation of sophisticated 6th order filter

There is only one, but huge complication. There does not exist a program, which would be able to calculate filter components’ values based on this particular frequency response. The reason for that is simple. Each consecutive section of ladder filter would need to work with complex input impedance in order to execute the calculations. And such feature is hardly provided by any computer program on filter design.

The only way out here is to utilize brute force approach and iteratively guess parts’ values until frequency response resembles the one pictured above. The rules for such design approach are:

- the lower capacitor/inductor value, the higher cutoff frequency of particular section of the ladder filter.
- Since cutoff frequencies of partial sections of ladder filter are different, each LC pair resonates at particular cutoff frequency. Due to this fact, a resistor must be placed in parallel with capacitor to attenuate the resonance.
- The resistor added introduces new path for DC current to flow and thus increases power demand of the device. Since the resistor only does its job at cutoff frequency of the particular section of the filter, it can be separated via another capacitor. The value of this capacitor should be chosen as high as possible within the given bounds so as to present open circuit for DC signal and an entire audio signal bandwidth.

Final filter’s topology and values of its components are presented in Figure 6.8. Frequency response of this circuit have already been presented in Figure 6.7. As can be seen, cutoff frequency of “2nd order”, ”4th order” and ”6th order” output is around 2.6 MHz, 600 kHz and 60 kHz, respectively. The objectives have been met.

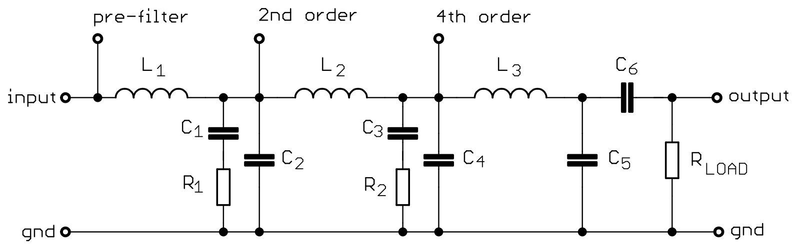



Figure 6.8: Topology of sophisticated 6th order filter

Another positive note to this filter is that, the filter is relatively immune to $R_{LOAD}$ value. Frequency response simulations are for both values 4 Ω and 8 Ω almost the same. Thus, when switching between SE 8 Ω and BTL 8 Ω configuration, the audio signal quality degrades unnoticeably.

## 6.3 Chip selection

According to the requirements stated at the beginning of the chapter, Class-D chip to be utilized in a device, needs to be robust. Ideally, it will be encapsulated in a PDIP (plastic dual in-line package) package and placed in a PDIP socket. Then, it will not only be easy to solder, but also almost effortless to replace in case of chip's failure. Further on, chip needs to be able to work at wide range of operating voltages, so it will not be damaged by mistakenly applied wrong power supply voltage. Output power of the chip is basically not important once it can feed at least 2 A of output current. Although the chip will directly drive output power MOSFETs with an almost infinite input impedance at DC, parasitic capacities of MOSFET structure will require peak current of around 2 A to switch the transistors on and off.

Chip TPA3122D2 perfectly suits mentioned needs. Robust amplifier encapsulated in 20-pin PDIP package offers 15 W of output power and can operate within 10 V to 30 V. Continuous drain current may be as high as 2.5 A and peak current must not exceed 3 A. Chip is very efficient, so it eliminates the need for any external heat sink. Thermal and short-circuit protection promise chip's longevity. Moreover, chip is fitted with MUTE, SHUTDOWN and GAIN SELECT functionality that allows to select among 20, 26, 32 and 36 dB [13].

## 6.4 Input filter design

The purpose of an input filter was explained in a theoretical part of the work, seek those pages, i.e. chapter “Input amplifier”, in case of need for more information. The Table 1 shows the relationship between input impedance $Z_{in}$ and chip's gain selected by pins $G_0$ and $G_1$. Since the device will be constructed with an adjustable gain settings, and hence varying input impedance, the input filter needs to be prepared for that.

Table 1: Input impedance and gain setting

| **$G_1$** **[-]** | **$G_0$** **[-]** | **$A_u$** **[dB]** | **$Z_{in}$** **[kΩ]** |
|---|---|---|---|
| 0 | 0 | 20 | 60 |
| 0 | 1 | 26 | 30 |
| 1 | 0 | 32 | 15 |
| 1 | 1 | 36 | 9 |

Input filter will be built of one external capacitor $C_{ext}$ (per channel) and internal input impedance $Z_{in}$. In the worst case, when considering highest gain setting and worst manufacturing tolerance of 20 % ([13]), input impedance will equal:

$$Z_{in} = 9000 - 0.2 \cdot 9000 = 7.2\ k\Omega \tag{6.1}$$

External capacitor with an internal impedance will create 1st order RC filter. If the cutoff frequency is chosen to 20 Hz, the value of capacitors will be:

$$C_{ext} = \frac{1}{2\pi f Z_{in}} = \frac{1}{2\pi \cdot 10 \cdot 7.2 \cdot 10^3} = 1.1\ uF \approx 680\ nF \tag{6.2}$$

Value of capacitors was floored down to 680 nF, because quality capacitors of higher capacities are way more expensive.

The choice of an external capacitor is crucial and must be taken carefully. Any parasitic leakage current flowing though the capacitor will result in an unwanted DC offset at the input amplifier and will consequently reduce useful headroom. Because of that, ceramic capacitors or low-leakage tantalum ones are perfectly suited for the application.

## 6.5 Output MOSFET driver design

Although the TPA3122D2 chip itself offers integrated output drivers, final circuit will comprise 4 external MOSFETS that will drive the load. One explanation for this kind of solution is protection of an amplifying chip and another is demonstrativeness of power transistors switching not truly-resistive load. The most straightforward design of such circuit would implement two pairs of push-pull transistors controlled directly by output pins of a chip, see Figure 6.9. For the sake of simplicity, no output filter will be considered in the following schematics.

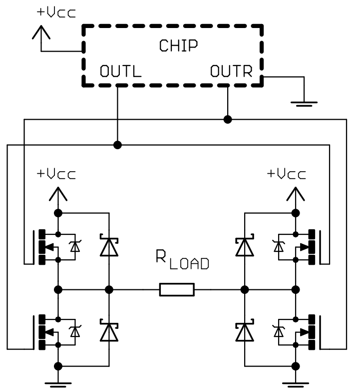



Figure 6.9: Most straightforward approach to external driver design

Although it looks well at first sight, it would not work quite as expected. Expectations are that if N-channel MOSFETs with almost zero $R_{DSon}$ were chosen, the transistors would not suffer from conductive losses. And if switching losses were negligible, the transistors would not dissipate any heat. However, the problem emerges once a deeper look is taken at the configuration. Depending on an input signal (plus polarity vs. minus polarity) one half of full H-bridge functions as a common-source follower. And for a voltage across load $V_{LOAD}$ in such configuration applies formula:

$$V_{LOAD} = V_{in} - V_{GS} \tag{6.3}$$

where $V_{in}$ is voltage of chip's output pins. Ideally, it will switch between 0 V and power supply voltage. $V_{GS}$ is voltage specific for a transistor. Value of $V_{GS}$ mainly depends on threshold voltage, which is, in case of standard power MOSFETs, around 4 V large. This means that voltage across load will be at least 4 V below power supply voltage. The 4 V drop will appear across $R_{DSon}$ resistance of the transistor. Thus, the transistor will dissipate around 4 V . 1 A = 4 W if the current of 1 A is expected to flow through. 4 W of heat losses per one transistor of an H-bridge is excessively large. There must exist a better solution.

Based on the equation above it can be deduced that the chip's output voltage must be at least 4 V higher than supply voltage of output transistor drivers. This could be easily done by introducing two power supplies - a DC-DC step up convertor to power amplifying chip and a laboratory power supply to power output drivers. Although this solution would work, it has few drawbacks. At first, medium-quality DC-DC step up converters are relatively expensive and would most probably be the most expensive part in an entire device. Secondly these circuits are very sensitive to power supply voltage. The voltage has to fit specified narrow range. This does not comply with robustness requirement. What if someone applies wrong supply voltage to the circuit by mistake? After such, and not unrealistic, scenario the circuit would have to be replaced. And in case of DC-DC convertor's failure there are the odds of burning out output drivers too.

Much safer solution based on an idea of two power supplies would introduce laboratory power supply powering a chip and a linear regulator powering output drivers, see Figure 6.10. The advantage of the solution compared to the latter is that linear regulators are much cheaper than DC-DC convertors and can work with a wide range of input voltages. However, the solution has a little fault. Linear regulators work on a principle of heat dissipation, hence the voltage drop would be achieved by turning large amount of power into heat losses. Despite, these loses could be pulled down to 2 W by tuning the design. That is within acceptable bounds.

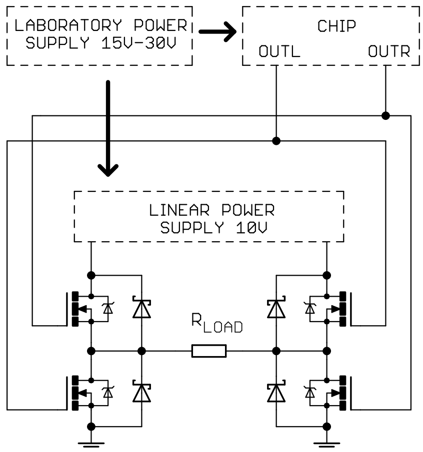



Figure 6.10: “The two power supplies“ improvement

Final solution that will actually be utilized, presents H-bridge constructed from N-channel and P-channel MOSFETs, see Figure 6.11. Gates of each push-pull pair are tied together and thus controlled by the same signal. The greatest advantage is that no matter input signal polarity, H-bridge always functions as a common source amplifier. For this configuration does not apply formula listed above, so there will not appear huge conductive losses. The second greatest advantage of the solution compared to the latter is that current circuit enables to implement both SE and BTL configurations. Previous solution would not allow that. On the other hand, this mixed-channel MOSFET H-bridge circuit reverses the phase of an output signal and requires to use perfectly matched transistors, otherwise they will shoot-through each other.

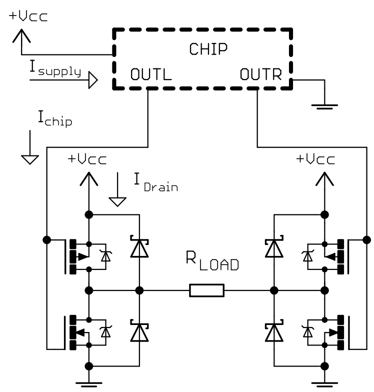



Figure 6.11: N-channel and P-channel H-bridge

Since output power transistors will be switching relatively high currents, they need to meet certain minimal criteria. Ideally, the transistors ought to be encapsulated in TO220 package because it can easily sink heat losses. Further on, transistors need to withstand at least 2.5 A of continuous output current and 20 A of peak currents. Shoot-through effect is going to be taken into account (this effect was mentioned in a theoretical part of the work). $R_{DSon}$ should be as low as possible, but based on approximate calculations, it should not exceed 200 mΩ. Maximum voltage does not really matter once it is higher than roughly 30 V. The most important parameters for the application are $t_{on}$ and $t_{off}$ time periods. These periods must roughly equal and be as short as possible. Partially because of low harmonic distortion, mainly due to shoot-through effect. The effect has crucial impact on an entire device and will be depicted in a while.

Table 3 and Table 2 shows comparison of best P-channel and N-channel MOSFETs for the application.

Table 3: Comparison of P-channel MOSFET transistors

| **Type** | $I_{Dcont}$ | $I_{Dpeak}$ | $U_{DSS}$ | $R_{DSon}$ | $t_{on} + t_{rise}$ | $t_{off} + t_{fall}$ |
|---|---|---|---|---|---|---|
| | [A] | [A] | [V] | [Ω] | [ns] | [ns] |
| IRF9630 | -6,5 | -26 | -200 | 0,8 | 39 | 52 |
| IRF5210 | -40 | -140 | -100 | 0,06 | 103 | 160 |
| IRF4905 | -74 | -260 | -55 | 0,02 | 117 | 157 |
| IRF9540 | -19 | -72 | -100 | 0,2 | 89 | 91 |
| IRF9Z34N | -19 | -68 | -55 | 0,1 | 68 | 71 |

Table 2: Comparison of N-channel MOSFET transistors

| **Type** | $I_{Dcont}$ | $I_{Dpeak}$ | $U_{DSS}$ | $R_{DSon}$ | $t_{on} + t_{rise}$ | $t_{off} + t_{fall}$ |
|---|---|---|---|---|---|---|
| | [A] | [A] | [V] | [Ω] | [ns] | [ns] |
| IRF510 | 5,6 | 20 | 100 | 0,54 | 23 | 24 |
| IRF520 | 9,2 | 37 | 100 | 0,27 | 39 | 39 |
| IRF540 | 33 | 110 | 100 | 0,044 | 46 | 74 |
| FDP6030BL | 40 | 120 | 30 | 0,02 | 20 | 31 |
| IRLZ34 | 30 | 110 | 55 | 0,035 | 109 | 50 |

Here, a short comment on few transistors is in place. IRF9630 is very fast and thanks to that, it could be easily found N-channel complementary pair (P-channel MOSFETs are usually significantly slower than N-channel ones). However, it does not provide enough current handling capacity, thus it cannot be selected. Oppositely, IRF5210 and IRF4905 provide enough drain current, but they are way too slow. IRF9540 presents a compromise between drain current and $t_{on}$/$t_{off}$ time periods, however it has large $R_{DSon}$ compared to all the other transistors. Finally IRF9Z34N suits all the requirements.

While choosing N-channel MOSFET it could be moved ahead the same way as it was done in case of P-channel ones. However, a different approach will be applied - alongside considering mentioned rules, emphasis will mainly be imposed on $t_{on}$ and $t_{off}$ time periods. Because by choosing a transistor with $t_{on}$ period greater than $t_{off}$ of its P-channel pair and $t_{off}$ period shorter than $t_{on}$ of its P-channel pair, shoot-through effect can be most efficiently eliminated. From the transistors listed in a table IRLZ34 is a clear choice.

Figure 6.12 depicts situation when conditions $t_{onN} > t_{offP}$ and $t_{offN} < t_{onP}$ are violated and once they are not. Since both gates of transistor complementary pair are tied together, they are controlled by the same signal SIG. Figure 6.12 supposes duty cycle of signal SIG to be 50 %. Rows N and P represent the state of N-channel of P-channel transistor. For the sake of simplicity only ON state and OFF state are supposed. Now, first falling edge of a signal SIG will be considered. If a signal SIG changes state from ON to OFF, N-channel transistor does the same. P-channel transistor behaves oppositely since it is transistor of a reversed polarity. But, if N-channel transistor turns off slower than P-channel one turns on, there exists short period of time, when both transistors conduct. During this time tremendous amount of current flows through, which is generally known as shoot-through effect. To avoid it, transistor pair should abide the condition $t_{onN} > t_{offP}$ and $t_{offN} < t_{onP}$.

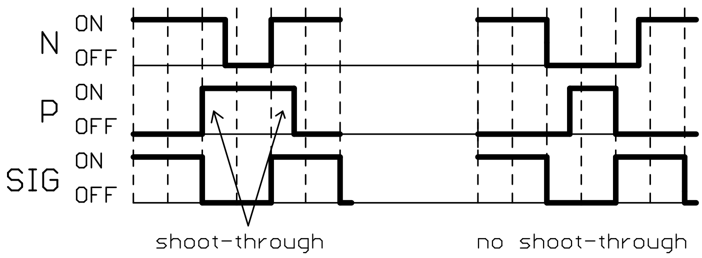



Figure 6.12: Eliminating shoot-through effect by choosing matched transistor pair

Figure 6.13 shows, what really happens, when external power MOSFETs are driving the load. The circuit simulated, see Figure 6.11, does not comprise anything “redundant”, e.g. any protection, reservoir capacitor and other. In Figure 6.13 $I_{Drain}$ represents current flowing through drain to source of both P-channel and N-channel MOSFETs of a half-bridge. $I_{supply}$ stands for power supply current, which powers entire circuit. In the simulated circuit, $I_{supply}$ is in value almost the same as $I_{Drain}$, if current demand of the chip $I_{chip}$ is ignored. $I_{chip}$ current mostly depends on the current of chip’s internal output driver. If a deeper insight is desired, current of chip’s internal output driver mainly depends on the parasitic charge that needs to be provided in order to turn on/off external power MOSFETs. Although the load current of around 1.5 A can be seen, shoot-through effect is the most dominant process in an entire figure.

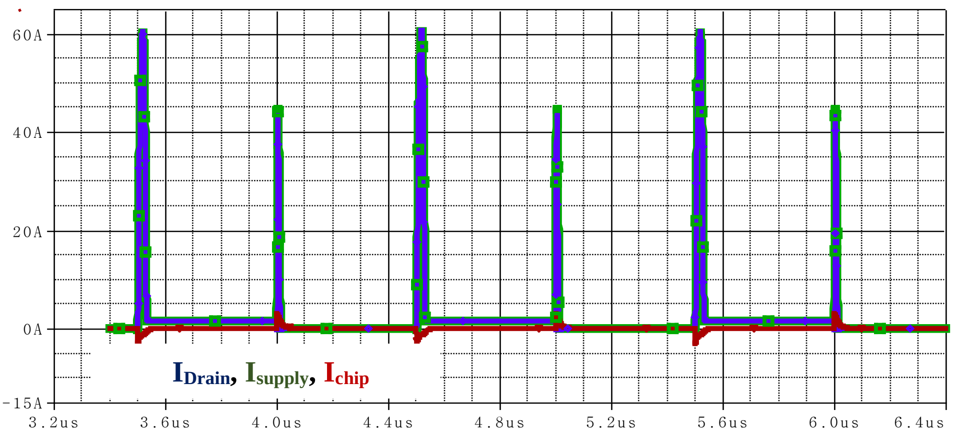



Figure 6.13: Shoot-through effect in an output signal simulation

In order to eliminate undesired shoot-through effect, some elaboration needs to be performed at first. Figure 6.14 shows zoomed peak of a preceding simulation. When shoot-through effect happens, its current demand is handled by power supply only. There is flowing maximum current of around 40 A in the circuit. Unless power supply is prepared for such current peaks, it will soon get damaged. Moreover, mentioned current peaks flow through an entire PCB and introduce noise. Once this noise gets into an input signal path, by no means will the designer be able to get rid of it. And lastly, although the transistors can withstand such peaks according to datasheet, it will be requested for their maximum ratings around 600 000 times a second. The question is, how long it will take until they refuse to do so. Output current of amplifier chip $I_{chip}$ is of the concern too, since it exceeds safe values. At the beginning of each switching process $I_{chip}$ current flows through amplifier output driver and provides a charge to both gates of external MOSFET transistors. During each switching, no matter falling/rising edge, the value of $I_{chip}$ current is the same. Initially, it steeply rises to dangerous peak of 4 A and subsequently slowly falls down to safe zone. Although "the dangerous period" lasts for about 10 ns, it cannot be accepted.

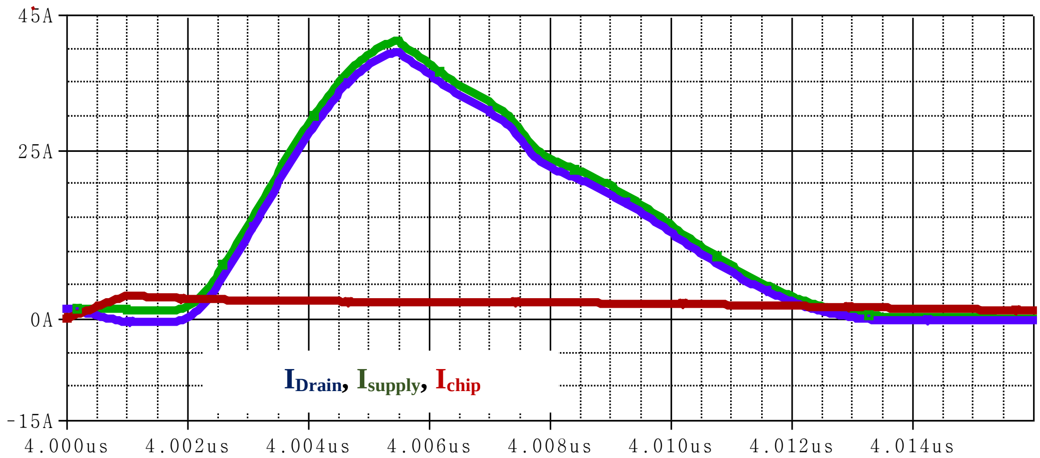



Figure 6.14: Zoomed shoot-through effect

At this point, there are two possible solutions to harsh shoot-through effect presented above. One is to buy professional full H-bridge driver that comprises all kinds of protections. And the other, which requires to build custom protections to the circuit that would attenuate the effect. Since the device will serve educational purposes, thus attenuated negative effects are actually desired and buying professional chip would feel like cheating, implementation of protections will rather be applied. Detailed elaboration on these protections is discussed in the following subchapters.

## 6.6 Driver's and chip's protection circuits

In the preceding subchapter it is mentioned that chip's output current $I_{chip}$ exceeds safe values and thus, it should be taken care of. Though, simulation of $I_{chip}$ current depicted probably the worst case, because it expected perfectly conductive traces between chip's outputs pins and transistor gates. It also expected no parasitic inductances of traces and worked with idealized transistor models. These and other effects omitted by simulation significantly contribute to slowdown of charging process of transistors' gates, thus reduce peak value of $I_{chip}$ current. Since $I_{chip}$ exceeds safe values just by little amount even in simulation, it was decided to leave this unprotected. To prove the decision right, small chip NE555 with maximum output current of 200 mA was selected as temporary driver of external transistors. After hours of testing chip remained cool with no change to its functionality. Thus, it can be proclaimed that much more robust amplifying chip will be able to drive output transistors without any damage made to it too.

### 6.6.1 Testing of external driver

Before designing protection circuits against shoot-through effect, the effect needs to be observed in a real device at first. Main objective of this section is to experimentally state whether shoot-through really occurs in the circuit as simulation expects and in what amount.

In order to measure shoot-through effect in particular transistor pair, few parts are required only, see Figure 6.15. Transistor pair is controlled by laboratory square wave generator and the transistor pair drives 8 Ω load. In series with the transistor pair 0.5 Ω resistor $R_{SENSE}$ is connected, which will serve as shoot-through sensor. Once shoot-through effect occurs, high current flowing though this resistor will cause some, at this time unknown, voltage drop. Voltage drop will be monitored by a scope connected in parallel with the sensing resistor. At the same time will the sensing resistor serve as a current limiter.

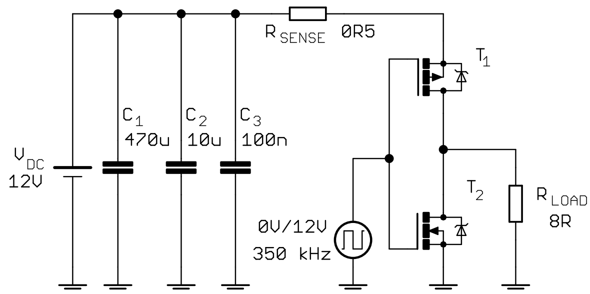



Figure 6.15: Testing of external driver schematic

Laboratory function generator was utilized as a square wave generator and the scope used was Agilent MSO-X 3052A 500 MHz. The measurement was held at a room temperature.

Figure 6.16 shows voltage across $R_{SENSE}$ resistor when circuit is operating. It can be easily seen that at each edge of control signal, shoot-through effect occurs. Although shoot-through current based on experiment is notably smaller than simulation expected, it cannot be taken not seriously because of reasons explained in preceding parts of the work.

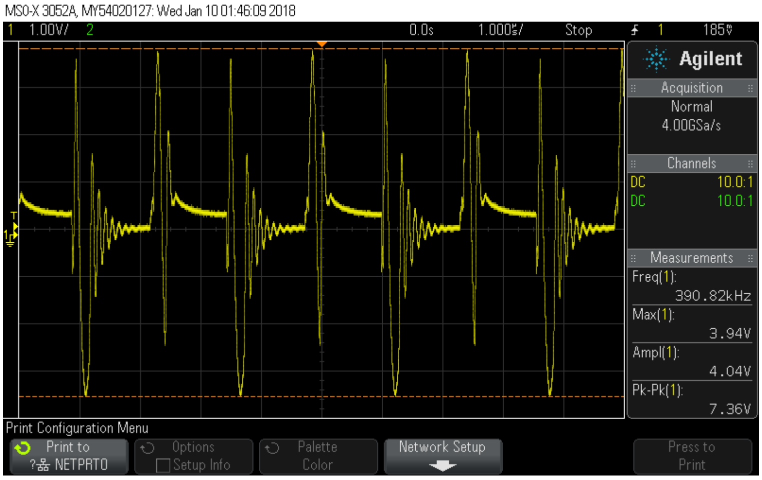



Figure 6.16: Switching current of external driver

Most important “discovery” of this experiment is surprisingly high dependency of shoot-through effect on power supply voltage. Although the dependency is evident, the more voltage, the more current, it is far not linear. For example, at 8 V of power supply voltage, output MOSFETs $T_1$ and $T_2$ did not heat up at all. At 10 V of power supply voltage, output MOSFETs overheated after few minutes of operation. And at 12 V the transistors overheated within a minute. To cool down such high power losses, large external heat sinks are required. Or, alternatively, some sort of protection circuit against shoot-through effect.

Figure 6.17 captures voltage across load. It is presented for one reason only – to show how output signal looks like, when the driver circuit consists of only two output MOSFETs, load and no other parts.

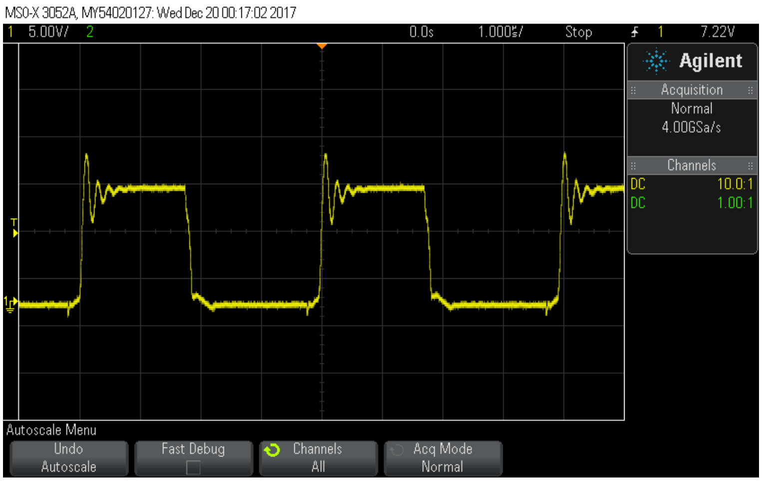



Figure 6.17: Output voltage of external driver

## 6.6.2 Shoot-through protection circuits

A moment's thought suggests that in order to implement shoot-through protection, computer simulation should be used at first. However, it must be taken into consideration that shoot-through effect is extremely fast phenomena which depends on huge amount of different factors. To simulate such effect, very precise transistor models are required. And such precise models are hardly provided by any simulating program. Because of that, computer simulation will be used only to prove basic functionality of protection circuits, but their final evaluation will be based on results of practical experiments. Thus, note that, all of the protection circuits that are going to be discussed in a while totally removed shoot-through effect in a computer simulation, in real world they did not always behave the same way at all.

## 6.6.3 Linear power supply protection

Results of measurement held in previous subchapter clearly state that output MOSFETs can operate at 8 V of power supply voltage without need for heat sinking. Since amplifying chip requires at least 10 V of power supply, then shoot-through protection circuit may only need to solve this conflict.

The easiest possible solution to the conflict is to split power supply of the device into two individual units. Laboratory power supply would provide power for amplifying chip and 8 V linear regulator to external MOSFET driver and internal driver of amplifying chip. Such circuit is presented in Figure 6.18. Note that, resistance of crucial PCB traces $R_{TRACES}$ was included too. Capacitor $C_{st1}$ and $C_{st2}$ would be soldered as close as possible to output MOSFETs, so as to prevent high current pulses spread around PCB. Reservoir capacitor $C_{res}$ would be mounted close to input power pins of PCB and it would provide peak current pulses with the charge instead of power supply.

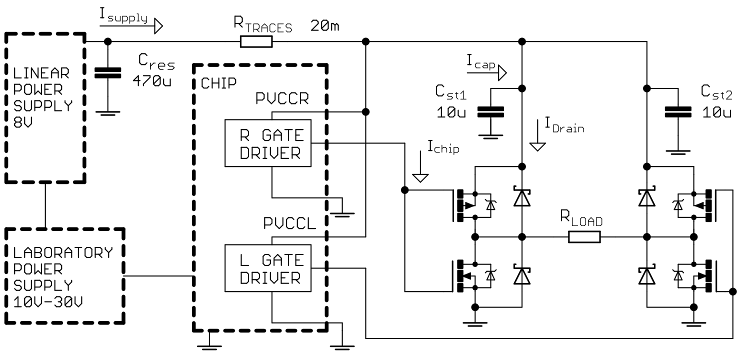



Figure 6.18: Linear power supply protection circuit

Although distrust of computer simulation of shoot-through effect was expressed at the beginning, result of it are presented in Figure 6.19. From the figure it can be noticed that all protective parts added function as they were intended. The majority of charge during shoot-through effect is provided by $C_{st1}$ and $C_{st2}$. Just a little charge travels through PCB and it is “handled” by a reservoir capacitor $C_{res}$. The power supply current remained unchanged during an entire switching process. Linear regulator has pulled down shoot-through current below safe 19 A and output chip's current below limit value either.

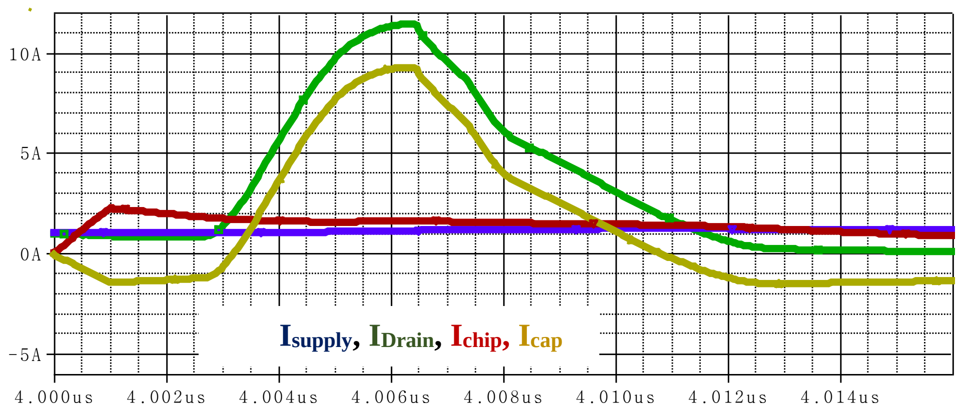



Figure 6.19: Computer simulation of circuit protected against shoot-through effect

The protection circuit has, though, few downsides. To begin with, at 8 V of power supply voltage, it can only be expected 1 W of output power in SE configuration and 4 W in BTL configuration. Furthermore, across linear power supply it will be dropped at least 2 V, which means around 2 W of power losses. So, although shoot-through effect was attenuated, heat sinking is still needed, but this time, for linear power supply. And lastly, what if someone leaves laboratory power supply with output voltage of 20 V set? Or even more? Power losses of linear power supply would exceed tremendous values and the device would only turn off once thermal protections of both amplifying chip and linear power supply noticed overheat conditions. At that time, some other parts of PCB had got already damaged.

Because of the downsides protection circuit will not be utilized in the device. It was mentioned here for one important reason. The function of reservoir capacitors $C_{st1}$ and $C_{st2}$ will be utilized no matter protection circuit that is going to be used in the end. Simulation results clearly proclaim, that once these capacitors are properly placed on PCB, they can effectively attenuate large current pulses flowing through power traces.

### 6.6.4 Current limiter protection

In practice shoot-through effect means that for a very little period of time the circuit is shorted. Then, why not to implement very fast current limiting circuit that would be connected in series with power supply traces? This circuit would constantly observe the value of driver's current and once the safe value has been exceeded, current limiter would detach power supply. It does not necessarily need to totally detach power supply, but at first, it does not really matter.

In Figure 6.20 it is presented, how such current limiting circuit could look like. In series with power supply traces there is resistor $R_1$ and transistor $T_4$ connected. Depending on current flowing through power supply traces, voltage across $R_1$ is generated. This voltage is used to control the state of transistor $T_3$ which in turn controls transistor $T_4$. Once shoot-through effect appears, current flowing through power traces is large and hence, voltage generated across resistor $R_1$ increases. When this voltage exceeds precise threshold value, transistor $T_3$ opens, what in turn results in switch-off of transistor $T_4$. Whether protected circuit is detached completely or partially is ruled by the value of resistor $R_2$. The main requirement for construction of the circuit are fast transistors, thus

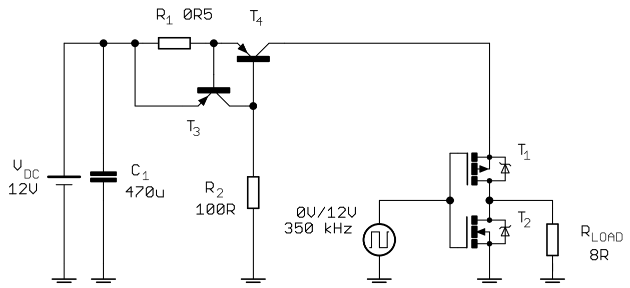



Figure 6.20: Current limiter protection circuit

bipolar ones were chosen over FETs.

Although the circuit works perfectly at DC, bipolar transistors are not fast enough to completely remove shoot-through effect. By the time transistor $T_4$ turns off, initial peak of shoot-through effect has already appeared. But once the transistor $T_4$ turns off, shoot-through effect is attenuated. Protection partially works, external output MOSFETs $T_1$ and $T_2$ do not heat up as much as they did without it.

### 6.6.5 Transistor switch protection

Next protection circuit will be based on two facts. The first one says, the less semiconductive parts in protection circuit, the faster it will be. The second one says that load current of transistor switch biased at the edge of saturation is always constant no matter load resistance value. The protection circuit discussed in this section will basically consist of transistor switch with circuit protected against shoot-through effect as its load. The idea is that shoot-through effect appears for protection circuit as if the load of transistor switch has decreased in value. Since transistor switch is biased at the edge of saturation, it always tries to keep its load current constant. Thus, in case of shoot-through, the transistor will decrease voltage across the protected circuit so as to preserve the balance.

The implementation of transistor switch protection is presented in Figure 6.21. It comprises transistor $T_3$ and two resistors $R_1$ and $R_2$. These resistors set bias point of the transistor at the edge of saturation. It means that voltage between collector and emitter of the transistor will equal to saturation voltage, when protected circuit is operating normally. Once protected circuit asks for more current than is allowed, voltage drop across transistor rises and voltage drop across protected circuit decreases. The loss of

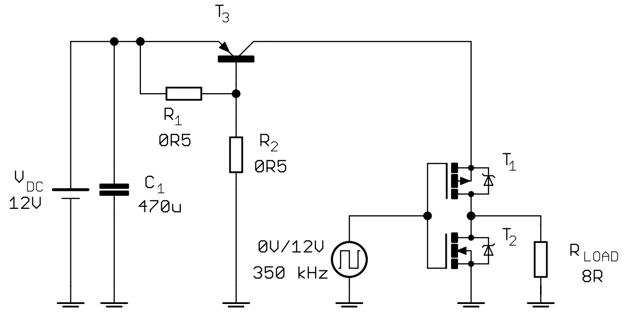



Figure 6.21: Transistor switch protection circuit

power supply voltage in protected circuit results in less current demand. Again, because of need for fast response, bipolar transistors were chosen.

As for preceding protection circuit, same applies here. Protection circuit works absolutely perfectly in computer simulation and totally removes shoot-through effect from protected circuit. However, in real world, the circuit is not fast enough. Initial peak of shoot-through effect is “unnoticed” by the protection circuit, but once transistor $T_3$ opens, the rest of shoot-through is effectively attenuated. External power MOSFETs $T_1$ and $T_2$ still heat up too much.

Note that, if circuit passed the initial testing, it would need to be tuned for particular application. For example values of resistors $R_1$ and $R_2$ only apply at power supply voltage of 12 V. In order for protection circuit to work at other supply voltages, transistor’s $T_3$ bias point would need to be set using Zener diode or other constant voltage reference. Another complication that would be faced with this protection circuit (and the preceding one) is, where to physically place the circuit on PCB. If it was placed close to external MOSFETs, it would get in a way of important signal traces and if it was placed too distant form external MOSFETs, its efficiency of attenuation of shoot-through noise would be worsened.

### 6.6.6 Dead time protection

The final and the only working solution to shoot-through protection circuit that had been found is presented in this section. As its name implies, the idea of the circuit is to insert few nanoseconds of dead time to control signal of external MOSFETs so as to prolong its particular edges. The implementation of such circuit is shown in Figure 6.22. It consists of two resistors $R_1$ and $R_2$ and two very fast Schottky diodes $D_1$ and $D_2$. The circuit greatly takes advantage of parasitic capacities of MOSFET transistors. These capacities can be pictured as external capacitors connected from transistor’s gate to its source. Their value is something around 200 pF per transistor. The circuit works for both transistors in same manner. It intentionally slows down turn-on process of the transistor and turn-off process leaves intact. Note that, in order to turn the transistor on, its parasitic capacity needs to be charged. Thus, protection circuit charges this capacity through resistor and the process is slow. On the other hand, to turn the transistor off, its parasitic capacity needs to be discharged. This process is handled by Schottky diode with very low value of series resistance, thus the process is fast. Once turn-on process is slower than turn-off, two transistors connected in series cannot shoot through each other. Note that, resistor $R_{SENSE}$ does not serve any shoot-through protection, it will only be used to measure value of shoot-through current with the scope.

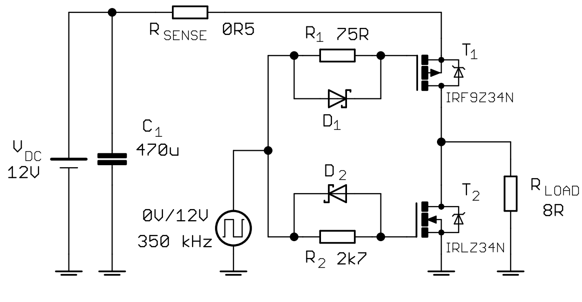



Figure 6.22: Dead time protection circuit

Figure 6.23 shows the oscillogram taken of gate signal of transistor $T_1$ (yellow trace) and voltage across load (green trace). The oscillogram clearly proves that shoot-through protection does its job correctly. As can be seen, rising edge of gate signal is very steep, thus turn-off process of transistor is very fast. On the other hand, falling edge of the signal is slow, hence turn-on process of transistor is significantly decelerated.

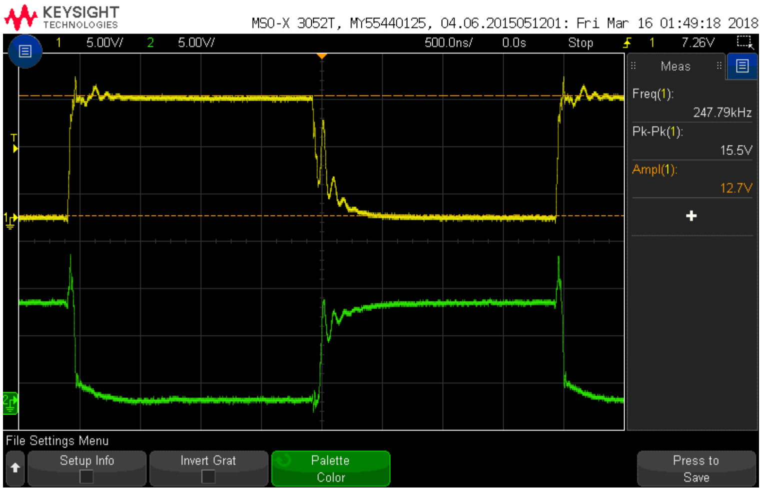



Figure 6.23: Gate signal of transistor $T_1$

Figure 6.24 depicts gate signal of transistor $T_2$ (yellow trace) and voltage across load (green trace). This time, the oscillogram is even more demonstrative. The falling edge of gate signal is steep, thus turn-off process of transistor is again very fast. The rising edge is very slow, due to large value of resistor $R_2$, what results in slow turn-on process of transistor $T_2$.

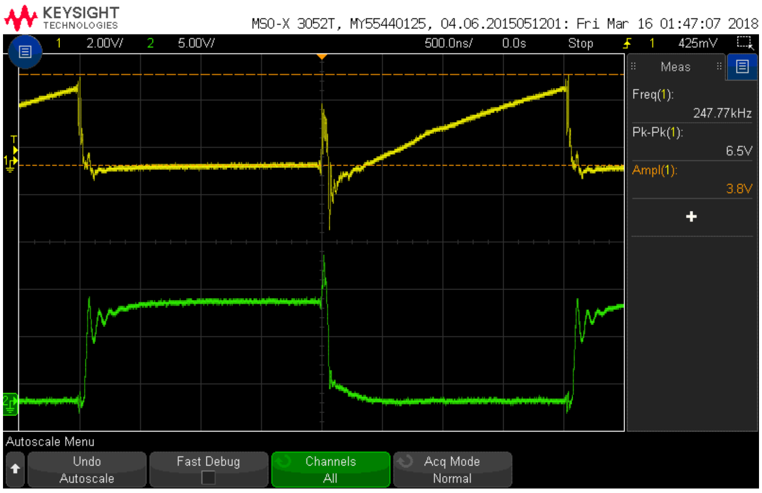



Figure 6.24: Gate signal of transistor $T_2$

The circuit is far not ideal. It does not remove shoot-through effect entirely, but it does its job good enough for the application. Power supply voltage can be as high as 17 V and output MOSFETs $T_1$ and $T_2$ are still able to cool down themselves without any external heat sink. For comparison, without protection circuit, external MOSFETs overheated at 10 V of power supply voltage.

The hugest downside of the circuit is its high dependency on temperature of external MOSFETs, the type of external MOSFETs and value of filtering capacitor $C_1$. Once the protection circuit is not tuned for particular conditions, it causes harsh destruction of MOSFETs' output signal. Hence to minimize negative impact of the dependency, resistors $R_1$ and $R_2$ ought to be replaced with trimmers whose value would be adjusted at the construction process of PCB. The only variable left unhandled is temperature of external MOSFETs. Fortunately this dependency is subtle. Moreover, protected MOSFETs are going to work at supply voltages around 15 V. For such low supply voltages protection circuit works well and MOSFETs temperature does not alter much.

Figure 6.25 shows voltage across $R_{SENSE}$ resistor when values of resistors $R_1$ and $R_2$ were chosen so as not to affect MOSFETs' output signal. The scope record was taken in the same scale as Figure 6.16 which pictures voltage across $R_{SENSE}$ resistor without any protection circuit. It can be seen that although shoot-through effect is not completely removed, it is largely attenuated. That suffices enough to keep output MOSFETs cool at required supply voltages.

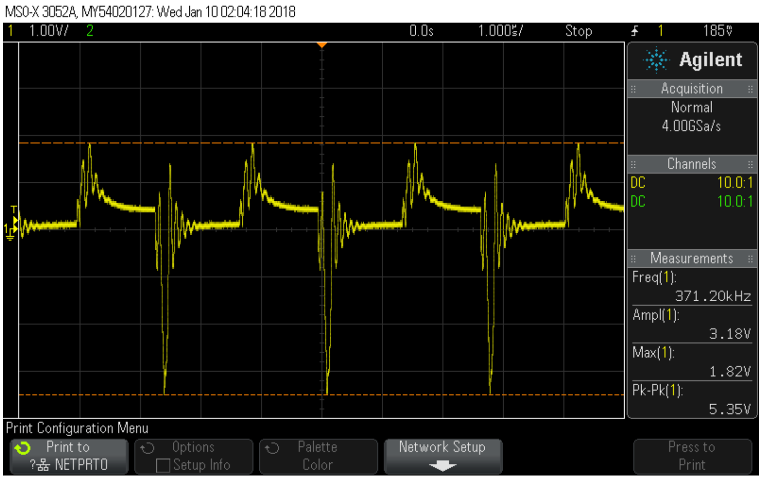



Figure 6.25: Switching current of protected external driver

Although it was stated above that external MOSFETs can cool themselves down even at 17 V of power supply voltage, it was decided to fit transistors with small heat sinks. These heat sinks provide total assurance that transistors will never overheat. In order to test the device, it was powered at 20 V, fed with sine wave and set for the highest gain. The device ran for 24 hours and it remained safely cool. The amplifying chip and external MOSFETs remained at a room temperature all day long. Thus, it can be now proclaimed that the device is safely protected against shoot-through effect.

Last note regards use of resistor $R_3$ in Figure 6.26. It does not relate to shoot-through protection in any way. It only builds a voltage divider $R_2$-$R_3$ which assures, that at no circumstances there will generate voltage higher than 16 V across gate and source of transistor $T_2$, if the device is powered by voltages less than 20 V. This sort of protection is required for transistor $T_2$ only, since its maximum $U_{GS}$ equals 16 V. Maximum $U_{GS}$ of transistor $T_1$ is 20 V, hence here, everything is safe. This simple protection against excessive $U_{GS}$ voltage has been tested in a range of power supply voltages from 10 V to

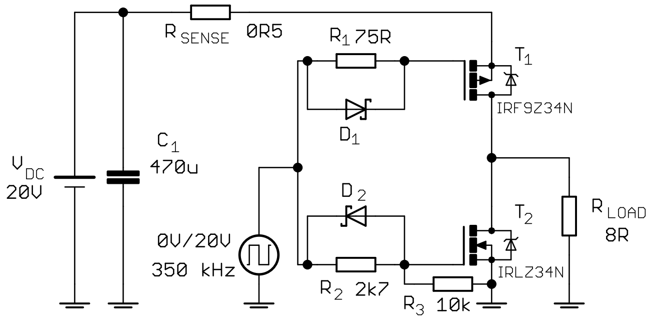



Figure 6.26: Voltage divider integrated into shoot-through protection circuit

20 V. No change to external driver functionality was observed.

## 6.7 Power supply protection circuits

In this section of the work, device's power supply protections will be discussed, particularly continuous low overvoltage protection and reversed polarity protection. The protection against power supply voltage less than 10 V is not going to be implemented, since amplifying chip has this type of protection integrated in it.

### 6.7.1 Continuous low overvoltage protection

The aim of the circuit presented in this section will be to protect an entire audio amplifier from continuous low level overvoltage that may appear between power supply pins. This overvoltage may be a consequence of improper device's manipulation, e.g. the device becomes powered by a new power supply with output voltage set excessively high.

The protection circuit does not need to be very fast in this case, neither does it need to provide protection against high overvoltage. The highest possible value of output voltage of standard laboratory power supply is 30 V. It is such a low value that will never damage amplifying chip. Output MOSFETs can withstand it for a considerably long period of time too, though, they are not cooled enough to operate at such conditions indefinitely. Moreover amplifier's 8 Ω load represented by 20 W resistors can operate at most at 22 V of power supply voltage, otherwise it overheats. The only sensitive parameters to power supply voltage higher than 20 V are maximum $U_{GS}$ voltages of MOSFET transistors used in external driver. They are both equal to 20 V and cannot be exceeded, otherwise the MOSFETs will surely get damaged.

Because of all the facts stated above, it was decided to create a protection circuit with 21 V compare level. If power supply voltage remains below this compare value, the voltage is allowed to power the device. But, once the power supply voltage crosses compare level, the relay turns on and cuts off power line to the device. Entire process takes around 5 ms. The relay remains turned on until power supply voltage is not set below compare value. No hysteresis was implemented in the circuit, because it is not needed. When the circuit is powered by stabilized power supply, there does not exist a voltage level, which would cause the relay to oscillate. Furthermore, implementation of hysteresis is hard task to accomplish, because any feedback set via new transistor is very sensitive to part values. Even a little deviation in resistors' resistance value, for example, rapidly pushes down the compare level.

Entire schematic of low overvoltage protection circuit is presented in the Figure 6.27. Zener diode $D_1$ creates 21 V compare level that once is crossed, turns on bipolar transistor $T_1$. Transistor $T_1$, in exchange, turns on relay $K_1$ that cuts off power line to the protected device. The purpose of Zener diode $D_2$ is important – it provides constant voltage across DC coil of relay no matter input voltage and, simultaneously, provides protection to transistor $T_1$ when relay turns off. The last comment on implementation concerns possible circuit's destruction. When power supply voltage is in range from 21 V to 22 V, transistor $T_1$ is half open and dissipates dangerous amount of power. This scenario ought to be avoided.

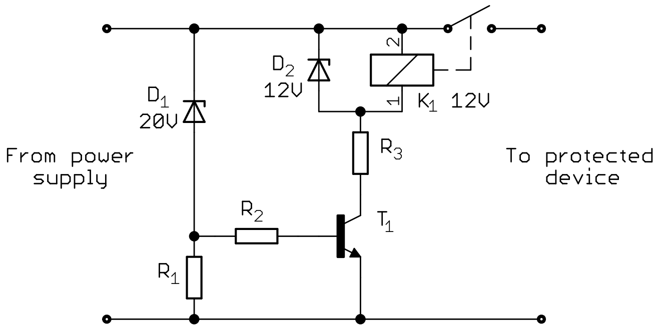



Figure 6.27: Low overvoltage protection circuit

If Zener diode $D_2$ was chosen to bear 2 W of power dissipation, maximum possible voltage that may appear on inputs of protection circuit is practically limited by power dissipation of resistor $R_3$. Since transistor $T_1$ always operates in a deep saturation, its power losses do not need to be taken into consideration. Practically speaking, if resistor $R_3$ can withstand 1 W of power losses, maximum input voltage may be as high as 35 V. 2 W resistor $R_3$ only lifts this boundary to 45 V.

Another possible solution to such protection circuit could equally be MOSFET transistor connected in series with main power line, just like contacts of relay are. The transistor would be constantly turned on and once the power supply voltage had crossed the compare level, the transistor would turn off. This approach is also convenient, though, it was not utilized due to following two reasons. Whereas the transistor has to always turn on and off, when the device powers up and down, the relay remains in its default position during the lifetime of the device. Provided that, no overvoltage condition occurs. Sure, the transistor can withstand millions on switchings, but the relay does not need to switch even once. So, which one is expected to last longer? And second, since transistor comprises some, although very little, value of $R_{DSon}$, there is always some voltage generated across its drain and source. This voltage not only reduces the headroom of amplifier, it also heats up the transistor, which, in turn, needs to be cooled down. A relay solution, on the other hand, does not impose such complications, since its contacts are almost perfect conductors.

### 6.7.2 Reversed polarity protection

Because of the same reasons as presented in “Continuous low overvoltage protection” it was decided to implement protection against reversed polarity of power supply. Few other alternatives were carefully considered, however the easiest one seemed as a best choice for this particular application. Simply, a series Schottky diode will be placed next to power supply pins. Once reversed voltage less than 60 V appears on power supply pins, it will be blocked by a diode. In case of device’s normal operation, the voltage drop introduced by a diode will be around 0.5 V, which is within acceptable bounds. A little LED diode was added to the circuit so as to signal reversed polarity state.

## 6.8 Circuit schematic

Figure 6.28 shows final circuit schematic which groups together all the minor circuits designed in previous subchapters.

The device will be powered by a laboratory power supply ideally of lowest output voltage fluctuations. Little fluctuations are accepted since large reservoir capacitors $C_5$ and $C_6$ were included in the design. The supply voltage ought not to decrease below 10 V and not exceed 20 V. The lower bound is a result of power requirements of amplifying chip. Once the supply voltage falls down below this value, the chip automatically shuts down and outputs no PWM signal. The higher boundary of supply voltage range is limited by power rating of 20W output load. Since continuous supply voltage larger than 22 V could heat up power resistors to dangerous temperatures for entire PCB, relay protection was implemented. It automatically cuts off power to the device, once it has recognized supply voltage larger than 21 V. This state is indicated by LED diode $D_5$. However, it is highly recommended not to use power supply voltages higher than 18 V, because they present a potential danger to external MOSFETs, whose control voltage cannot exceed 20 V. Basic rule of thumb applies here - the lower power supply voltage, the higher longevity of the device. In the design, there was added another LED indicator $D_1$, which warns about reversed polarity of input power wires. During this condition the device remains protected too via Schottky diode $D_2$.

The device can provide sinusoidal output power of 2 x 5 W in SE configuration. During normal operation the amplifying chip remains cool as well as external MOSFETs $T_2$, $T_3$, $T_4$ and $T_5$. During state of full load external MOSFETs only heat up to around 30 °C. If they are hot to touch, there has something went wrong with their protection circuit discussed in subchapter “Shoot-through protection circuits”. However, note that, the protection circuit had been tested long hours (three days in a row) and never showed malfunction.

Schottky diodes $D_{10}$, $D_{11}$, $D_{12}$ and $D_{13}$ protect external MOSFETs against overvoltage generated by inductors of the filter. Capacitors from $C_{13}$ to $C_{18}$ belong to output driver too and provide with decoupling function. Each time the transistors switch on, these capacitors provide them with required peak current. Since circuit comprises another output driver (integrated into TPA3122D2), further decoupling capacitors need to be provided. This function is supplied by capacitors $C_7$ and $C_8$.

The schematic comprises four jumpers, two switches and few probe points. Jumper $JP_1$ ought to be shorted, otherwise the amplifying chip will shut down. Jumper $JP_2$ should be left open, otherwise output pins will be muted. The difference between shut down and mute functionality is distinct. While during shut down there is 0 V voltage on LOUT and ROUT pins of the chip, during mute state there is PWM output signal of 50 % duty cycle. Such duty cycle is by filter turned into 0 V average voltage. Jumpers $JP_3$ and $JP_4$ are used to set gain settings of the chip. For possible combinations and resulting gain, see Table 1. Switch $S_2$ can connect/disconnect the load to/from the driver so as to make it possible to measure amplifier's output impedance. Probe points can be used to observe the process of transforming PWM wave into audio signal.

In case of MOSFETs' failure and their total destruction, they must be replaced by transistors of the same type. If replacement parts are no more on the market, the transistors can be replaced by similar alternatives. The most vital transistor parameters are – parasitic gate capacity, on-off time periods, drain current and $R_{DSon}$. Though, resistors from $R_{11}$ to $R_{16}$ need to be trimmed to new values for shoot-through protection to work properly.

If the relay protection circuit against supply voltage higher than 21 V starts to malfunction, the relay can be unmounted and mains line reconnected together. This scenario is, though, hardly expected to occur.

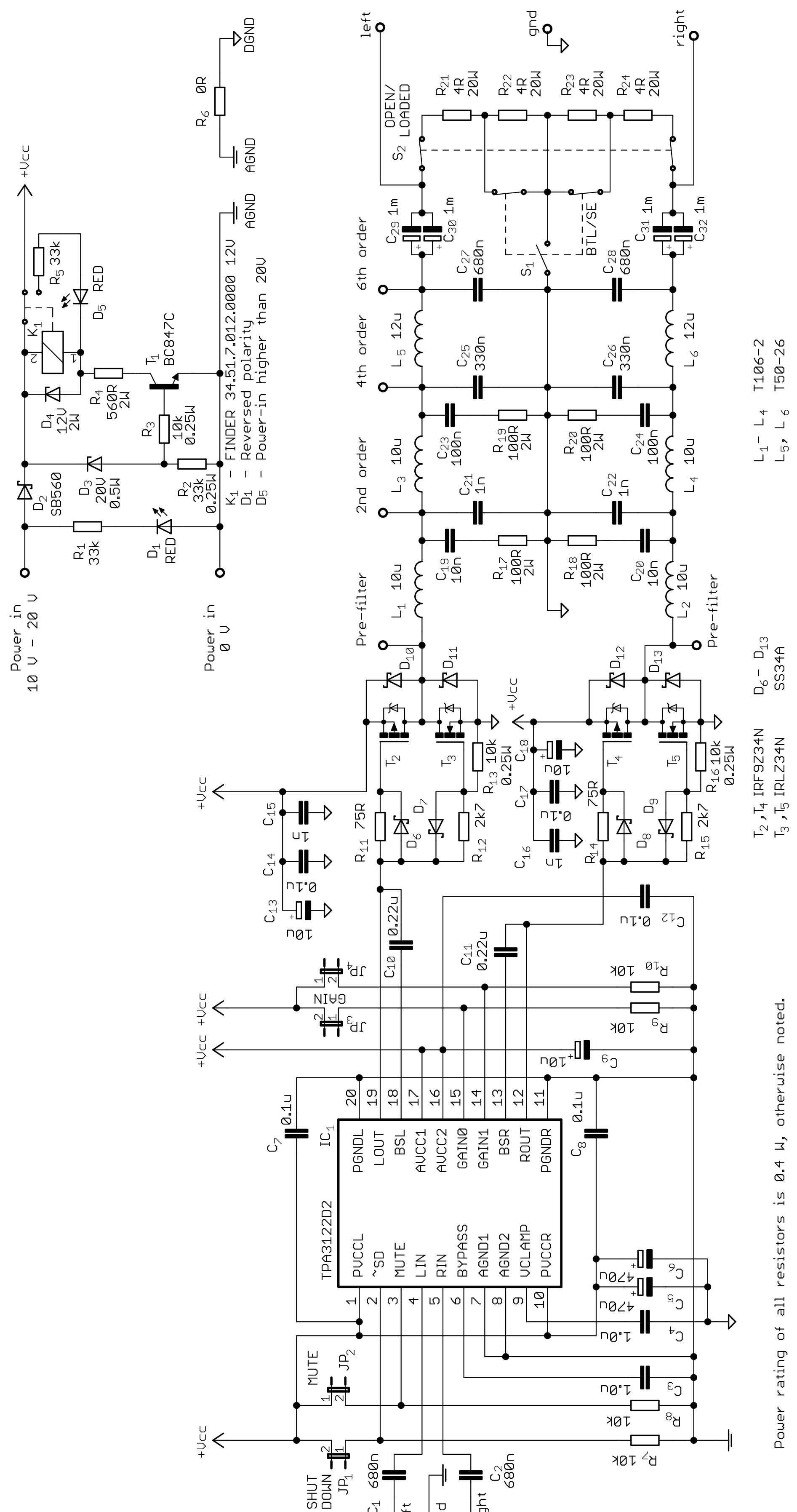



Figure 6.28: Final device's schematic

# 7 CONSTRUCTION

Main objective of this part of the work is to design and build PCB for the device. However, before doing that, it must be first built an output analog filter. Following subchapters guide through whole construction process.

## 7.1 Coils construction

Coil design plays an important role in an entire construction process, since it significantly influences final cost of the device. Moreover, coils, if inappropriately designed, become excessively large and take up lots of useful space on PCB and enlarge the size of the chassis too. Because of all this, the main target of this chapter will be to design output filter coils small enough to fit, for example, T106 toroidal core (outer diameter of around 3 cm).

When designing custom coil there may be taken two approaches – a common sense and an erudite one. The common sense will be used to state the core size of inductor and subsequently, once that has been found, the core size will be checked against magnetic saturation using proper design formulas.

At first, a type of coil must be stated. According to literature [3] best type for the application of Class-D audio amplifiers is iron-powder toroidal core. Although iron-powder core does not provide with high permeability compared to, for example, ferrite core, so its size will rather be large, iron-powder core does not, though, introduce harsh non-linearities. The advantage of toroidal shape of the core is that magnetic field stays encapsulated around inner core dimensions, thus the core does not interfere with other parts of the PCB. Air coils were also taken into consideration during the design, but neither single-layer, nor multi-layer ones would be small enough to meet the requirements. Literature [3] further recommends use of core that still works at frequencies five times higher than the frequency of internal oscillator of an audio amplifying chip. For TPA3122D2 with internal oscillator frequency of 250 kHz (see [13]), the core must operate at least at 1.25 MHz to effectively attenuate 5th order harmonics. That means use of “2 Material Iron Powder Toroid” core type, which is designed for frequencies as high as 30 MHz. Once “high frequency” components of PWM modulation are attenuated, cores for lower frequencies, particularly “26 Material Iron Powder Toroid”, can be used. At lower frequencies material 26 will be used instead of material 2 because of following reasons. Cores of material 26 provide with higher permeability, thus they are smaller in size. Since they were designed for frequencies less than 1 MHz, they retain higher quality factor and less core loss in audible spectrum compared to material 2. And lastly, material 26 is significantly cheaper than its “high frequency” counterpart. If a schematic presented in Figure 6.8 is considered, then coils $L_1$ and $L_2$ will be wound around core made of material 2 and coil $L_3$ around core made of material 26.

Diameter of the wire that will be used for coil winding should be known at this time too. For coils $L_1$ and $L_2$, wire of 1.00 mm diameter will be used, since it is currently at university’s disposal. If the length of wire is expected to be something around 1 m, DC resistance of such wire will not exceed 20 mΩ. That is low enough. Since coil $L_3$ will be wound around core of smaller size, a thinner wire must be used. A wire of 0.60 mm diameter was chosen.

Next, approximate value of coil inductance must be known. The final filter schematic has already been presented in Figure 6.8, thus inductance of all coils will be around 10 μH. Now, if coils $L_1$ and $L_2$ are considered, then toroidal core T106-2 will be chosen. Note that, core selection was based on repeated calculations that are going to be presented below.

To calculate maximum number of turns $N_{max}$ around any toroidal core, following formula can be applied:

$$N_{max} = \frac{\pi d_i}{d_w} \tag{7.1}$$

where di stands for inner diameter of the core and $d_w$ for diameter of the wire used. Bear in mind that formula is approximate. In practice maximum number of turns that can be wound around core is significantly less because of thickness of the wire, which reduces effective core's inner diameter. Once maximum number of turns $N_{max}$ is acquired, required number of turns around the core ought to be calculated. Here applies following formula:

$$N = \sqrt{\frac{L_{coil}}{A_L}} \tag{7.2}$$

where $A_L$ stands for inductance factor given in nH/turn$^2$ and $L_{coil}$ for coil inductance in nH. In practice, inductance factor is usually given in Henrys per some precise number of turns, e.g. 50 μH/100 turns. In order to use formula stated above, $A_L$ has to be re-counted to nH/turn$^2$. This can be achieved by using formula:

$$A_L = 1000\frac{U}{T^2} \tag{7.3}$$

where $A_L$ stands for inductance factor given in nH/turn$^2$, U and T comprise inductance factor given in format "U μH/T turns".

In case of core T106-2, with inner diameter of 14.5 mm and inductance factor of 135 μH/100 turns, maximum number of turns $N_{max}$ is 45. Required number of turns to build an inductance of 10 μH is 27. Although T106-2 now seems unnecessarily large, in practice maximum number of turns that can be wound around the core is around 32, when considering wire of 1.0 mm diameter. Hence, the selection of core T106-2 was correct. Otherwise, the same procedure would need to be repeated over again to find best matching core size.

Since core size has been selected, it should be now checked whether it is not underestimated in terms of magnetic saturation. Detailed check procedure can be found in [3]. Here will only be presented a brief summary.

Before calculation itself, few parameters should be stated. More specifically, coil inductance $L_{coil}$, maximum current flowing through the coil $I_{coil}$ and two core's constants, magnetic permeability $\mu_{tor}$ and a magnetic intensity $H_{tor}$. Coil inductance $L_{coil}$ was calculated earlier and its value is 10 μH. Maximum current flowing through the coil $I_{coil}$ will be equal to load current. Thus, if we expect at most 20 V of power supply voltage and 8 Ω of load resistance in SE configuration, load current will result in value of 2.5 A.

Maximum coil current should be, though, a little oversized, thus 3 A will be supposed in following calculations. Value of core's magnetic permeability $\mu_{tor}$ can be found in datasheet, which states the value of 10 for T106-2 type. Besides, this is common value for iron-powder toroidal cores. Numerical value of magnetic intensity $H_{tor}$ was found in [3] and equals 390 A/cm.

Based on formula presented below, toroidal core's volume $V_{tor}$ can be calculated. Note that, $\mu_0$ equals $4\pi.10^{-7}$ H.m$^{-1}$.

$$V_{tor} > \frac{L_{coil}\, I_{coil}^2}{\mu_0\, \mu_{tor}\, H_{tor}^2} \tag{7.4}$$

For parameter values stated above, minimum core volume is 0.018 cm$^3$. Now, if volume of toroidal cores of different types is calculated, or by seeking literature [3] it can be found that even core size T30, with $V_{tor}$ = 0.12 cm$^3$, meets the criteria. Note the lower number after "T" letter, the less core dimensions and worse magnetic saturation immunity. Thus, it can be proclaimed that toroidal core of size T106-2, with $V_{tor}$ = 4.48 cm$^3$, safely meets the requirements.

If a brief summary is desired, the first two coils $L_1$ and $L_2$ of the filter will have an inductance of 10 µH and will be wound around T106-2 toroidal core. The wire used will have 1.0 mm in diameter and 27 turns will be performed. Wire length of 1.1 m is necessary.

Two inductors are done, there is one last left. Since all the calculations concerning coil design are relatively simple, they will not be performed again. The procedure remains the same. Here will only be presented results of calculations.

The last coil in the filter is supposed to have an inductance of 12 µH. It will be wound around iron-power toroidal core T50-26. Winding wire will be 0.60 mm in diameter. This time 20 turns will be performed. Wire length of 0.7 m is necessary.

## 7.2 Output filter construction

In "Output filter design" subchapter it was presented how an ideal frequency response and topology of output filter ought to look like in order for the filter to demonstrate the creation of audio signal. In this chapter such filter is going to be built.

Coils for the filter have already been wound in the previous subchapter and capacitors have been bought based on recommendations given in [3]. The prototype is going to be built on a breadboard.

The first problem emerges right after the filter prototype is constructed and probed by a scope. The audio signal measured at designated probe points totally denies theoretical expectancies. Tested sine wave is way too much distorted by unwanted frequency components at every probe point. It can be easily observed that the sine wave comprises another unwanted high frequency signal. It is no surprise that the noise is at 250 kHz, which is frequency of internal oscillator of audio amplifying chip. Although these PWM modulation products are actually desired, since they show, what the output filter does, they cannot appear at such high voltage levels. Particularly, at the filter's very output, the signal should be totally filtered out. But this does not happen.

It is evident that something went wrong. Particularly, values of some parts are not as they ought to be. Resistors and capacitors were bought with 5 % tolerance, thus they are safe. On the other hand, coils have been wound unprofessionally with an unknown tolerance and what is more, coils wound around toroid cores are always frequency dependent. Because of these facts it was decided to measure their inductance in an audible spectrum. For the measurement it was chosen a coil based on core T106-26 and expected inductance of 40 µH. The results of measurement are as follows. The coil has an inductance over 200 µH at 20 Hz, around 190 µH at 200 Hz, 170 µH at 2 kHz and over 90 µH at 20 kHz. The inductance does not match its expected value. At low frequencies it is five times as inductive as expected and at 20 kHz the inductance still does not meet the design criteria. The coil reaches the inductance of 40 µH somewhere around 60 kHz. This conclusion is not that bad as it seems at first sight. The coil roughly reaches its proper value around cutoff frequency and that is important. At lower frequencies this non linearity has subtle effect on final filter's frequency response. Though, this drift in coil inductance causes the filter not to behave as theoretically predicted.

Because of significant deviation of the filter from theoretical expectations it was decided to build the filter in successive steps. At first, it was constructed 2nd order filter with pass-band wider than entire audio spectrum, but cutoff frequency set low enough to totally filter out unwanted PWM modulation products. Then, it was added another 2nd order filter with even wider pass-band, which introduces few of these products. Finally, the same procedure was repeated and new 2nd order filter was joined that filters out almost nothing. This way has been entire filter built. Its frequency response ought to correspond to simulation results presented in Figure 6.7.

Note that, although the construction of filter seems easy and straightforward, the building process takes tens of hours of work. In order to build a filter the described way, one must pass through numerous mathematical computations, computer simulations, winding different cores of various inductances, measuring of output signal and observing it on scope. Not to mention the time spent on getting the prototype back to work after some wire has loosen in the socket of breadboard.

Final circuit schematic of filter built is presented in Figure 7.1. After comparing it with theoretical schematic presented in Figure 6.8, few differences can be noticed. Capacitors $C_4$ and $C_5$ have changed in values so as to compensate for too inductive inductors and hence, push cutoff frequencies to desired values. Inductors have been left intact because winding of new coils is rather expensive and time consuming than just replacing capacitors. The last change has been made to resistor $R_2$, which increased in value from 22 Ω to 100 Ω. The reason for it simple. Although the change of resistor slightly deforms final frequency response, the resistor does no more need to be of high

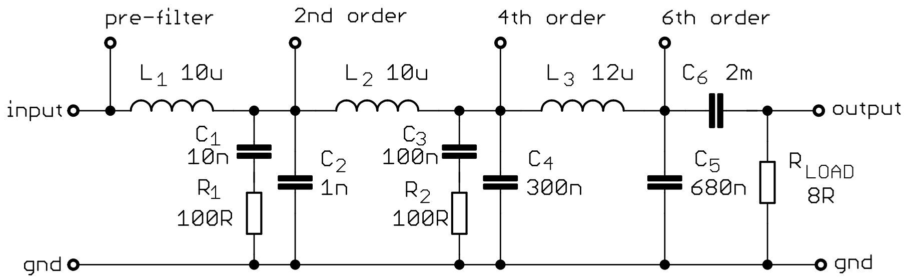



Figure 7.1: Output filter for the final device

power rating. Moreover, this swap in resistors unnoticeably alters the shape of (intentionally distorted) sine wave signal.

At this point it would be more than desired to measure final frequency response of the filter constructed. However, it is not possible – the laboratory does not possess any low output impedance high frequency generator. The only possible solution is to measure output filter using the amplifying chip. However this solution is very limiting – because of Nyquist theorem the amplifier could not be fed with a signal of frequencies higher than 100 kHz.

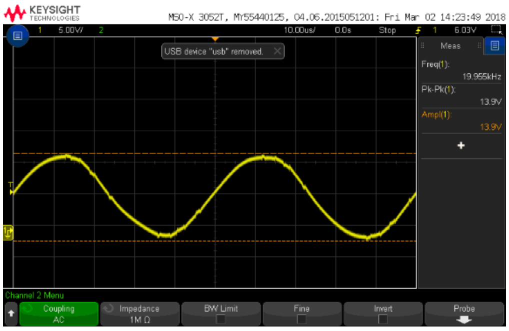
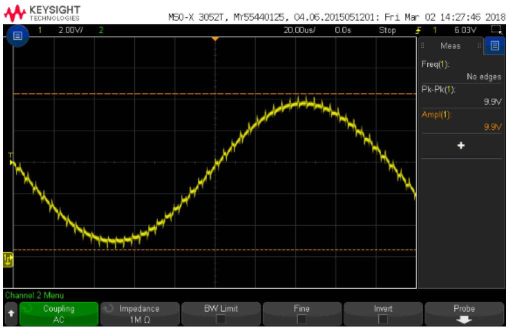
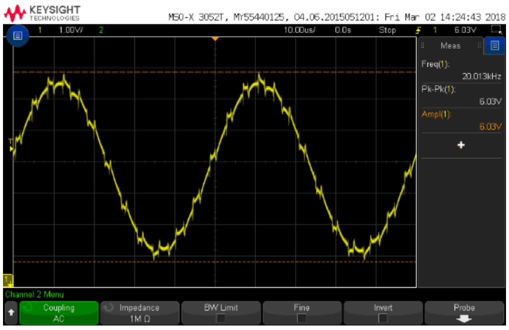
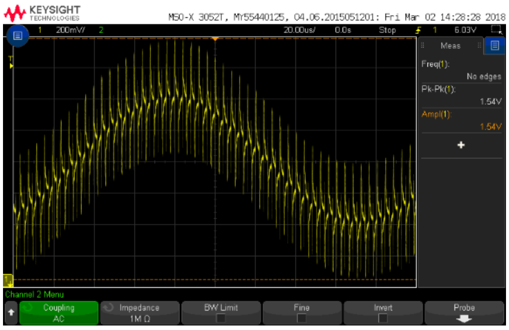
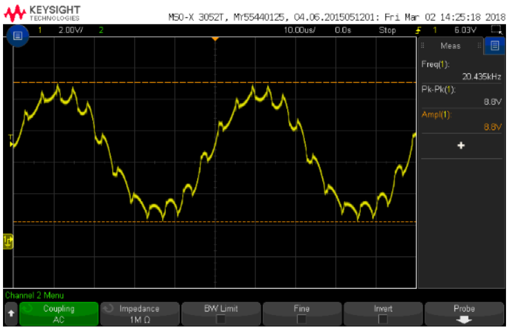
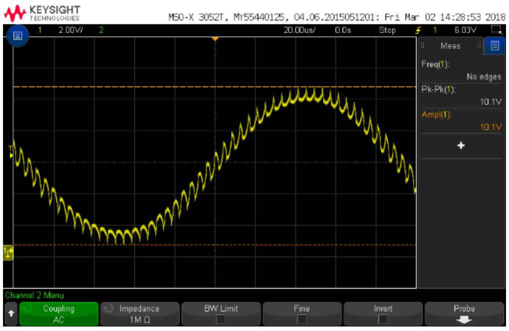
Second part of this subchapter will devote to examination of PWM modulated audio signal processed by the filter. The PWM modulated signal will originate from audio amplifying chip, which will be fed with low level and high level sine wave of 20 kHz and of 5.5 kHz for comparison. The results of measurement are presented in Table 4. Note that, oscillograms have been taken using high tech scope Agilent MSO-X 3052A 500 MHz. Cheaper scopes had not been fast enough to portray oscillograms in such detail as presented.

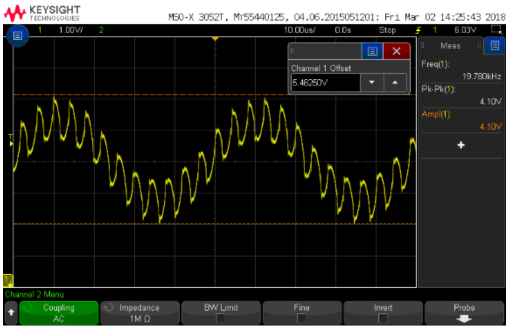
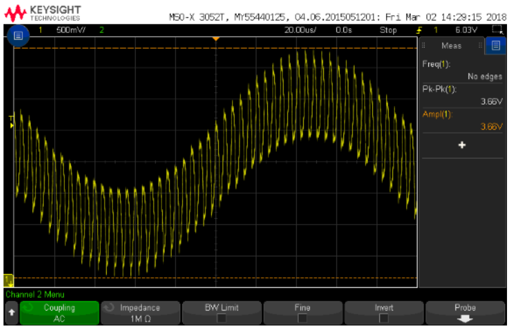
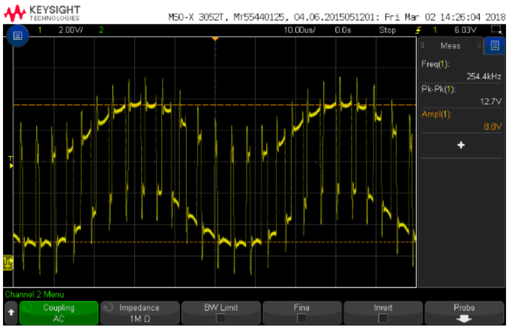
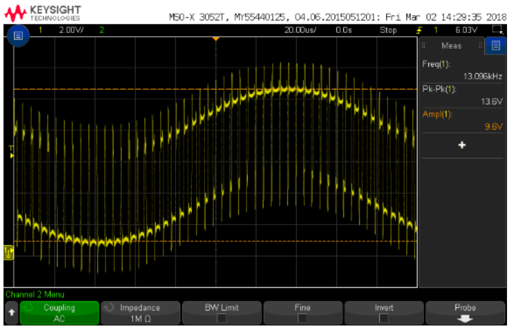
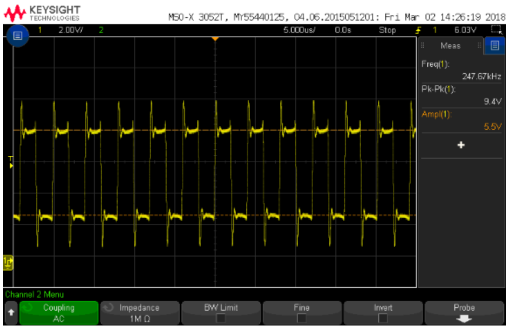
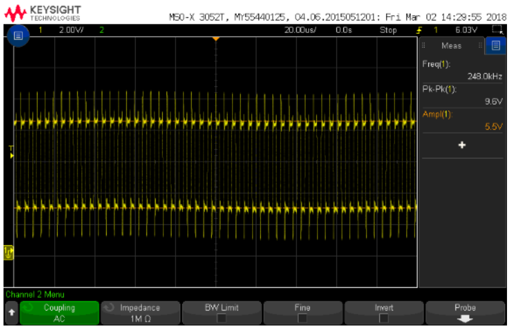
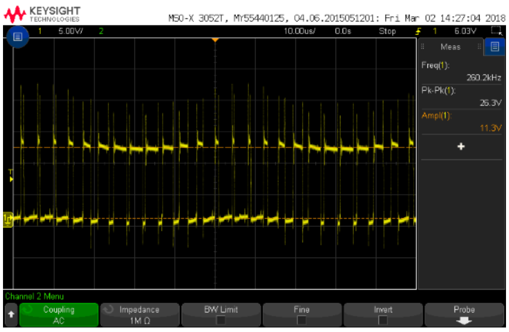
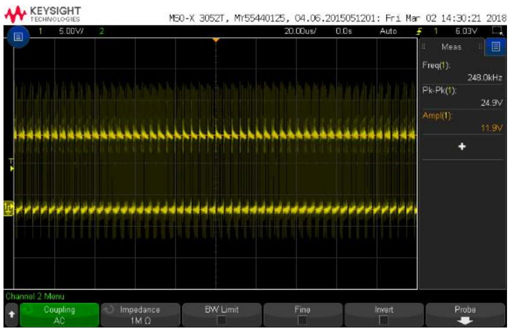
As can be observed from the Table 4, high level 20 kHz sine wave is totally filtered out from any unwanted PWM modulation products at filter's "6th order" probe point. The same sine wave is significantly distorted at "4th order" probe point. This distortion originates in PWM sampling frequency since it oscillates at 250 kHz, what is chip's internal oscillator frequency. Pass-band at "4th order" output is, though, not wide enough to pass sharp edges of PWM modulation. Due to this fact, the distortion resembles a sine wave of 250 kHz superposed on an audio signal. Probably the most interesting signal shape can be observed at "2nd order" probe point. This oscillogram has been zoomed and shown in a new figure, Figure 7.3. It clearly demonstrates, what output filter does. The filter only turns duty cycle of PWM modulated signal into its constant average voltage level during particular period. Further filtering then curves remained sharp edges. The last oscillogram was taken from "pre-filter" probe point and it presents how PWM modulation works. High level input voltage is turned into high duty cycle square wave, low level input voltage is turned into low duty cycle square wave and no input signal results in duty cycle of 50 %.

The difference between same signal of high and low voltage level observed at same probe point can easily be explained. The lower voltage level of input signal, the lower variation in duty cycle of PWM modulated signal, e.g. variation from 45 % to 55 %, thus the narrower pulses of PWM signal and the wider bandwidth with greater "high frequency" products.

The last note to output signal shape regards high, initial peaks at the beginning of each partial square wave that can found for example in Figure 7.3. These sharp pulses consist of wide spectrum that comprises frequencies as high as tens of MHz. At such high frequencies toroidal cores utilized in the filter no more effectively attenuate any signal, hence it passes the filter "unnoticed".

Table 4: Oscillograms taken of output filter

| | **Input signal frequency:** 20 kHz | **Input signal frequency:** 5.5 kHz |
|---|---|---|
| **Input signal level:** high<br><br>**Output probe point:** 6th order |  |  |
| **Input signal level:** low<br><br>**Output probe point:** 6th order |  |  |
| **Input signal level:** high<br><br>**Output probe point:** 4th order |  |  |

| | **Input signal frequency:** 20 kHz | **Input signal frequency:** 5.5 kHz |
|---|---|---|
| **Input signal level:** low<br><br>**Output probe point:** 4th order |  |  |
| **Input signal level:** high<br><br>**Output probe point:** 2nd order |  |  |
| **Input signal level:** low<br><br>**Output probe point:** 2nd order |  |  |
| **Input signal level:** high<br><br>**Output probe point:** pre-filter |  |  |

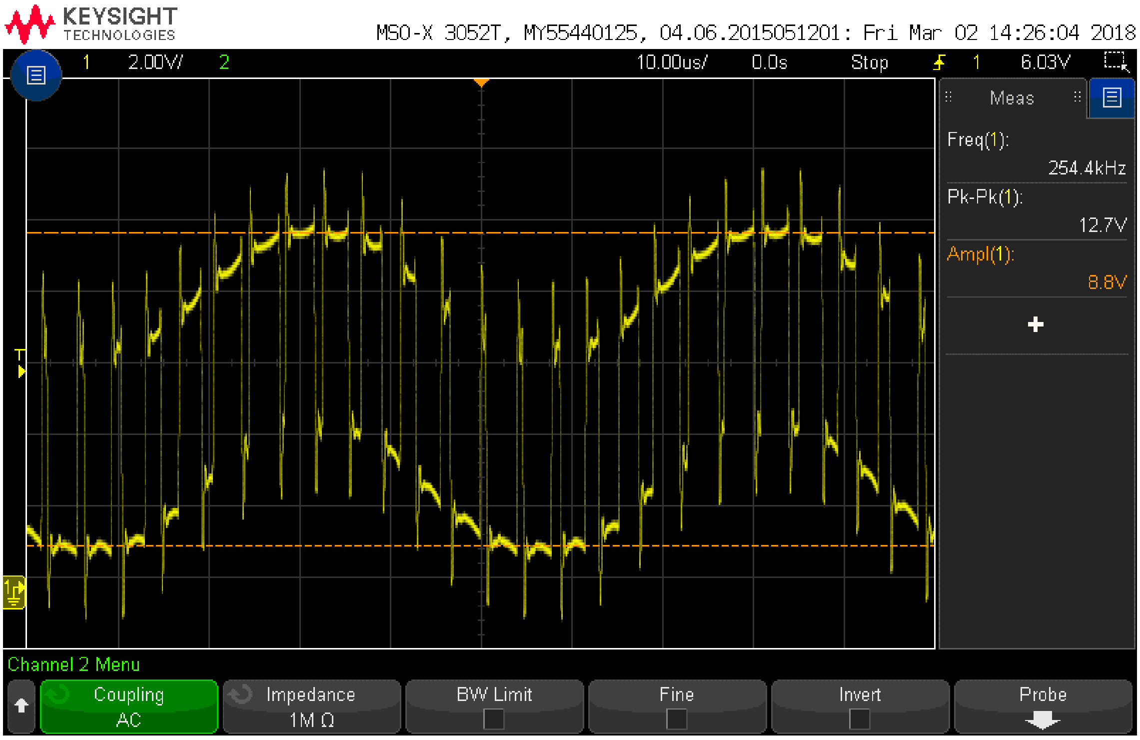



Figure 7.3: Shape of sine wave at 2nd order output of the filter

Although the frequency response of the filter cannot be measured, it can be observed a spectrum of signal processed by the filter. Figure 7.2 shows the spectrum of 20 kHz input signal at the “2nd order” probe point. Based on position of cursors, it can be seen that spectrum is as large as 12 MHz. The most significant components of PWM modulated signal are at 250 kHz.

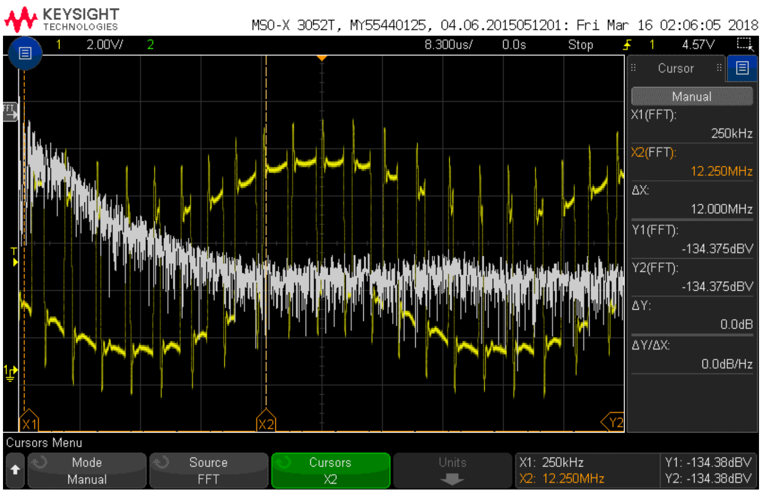



Figure 7.2: Spectrum of signal at "2nd order" output

Figure 7.4 shows spectrum of the same input signal, but this time, at “4th order” probe point. It can be observed that most significant components are at 20 kHz and 250 kHz. Further PWM components appear at multiples of sampling frequency, i.e. 500 kHz, 750 kHz and at frequencies, for which applies formula (k.250000 ± n.20000) Hz, where

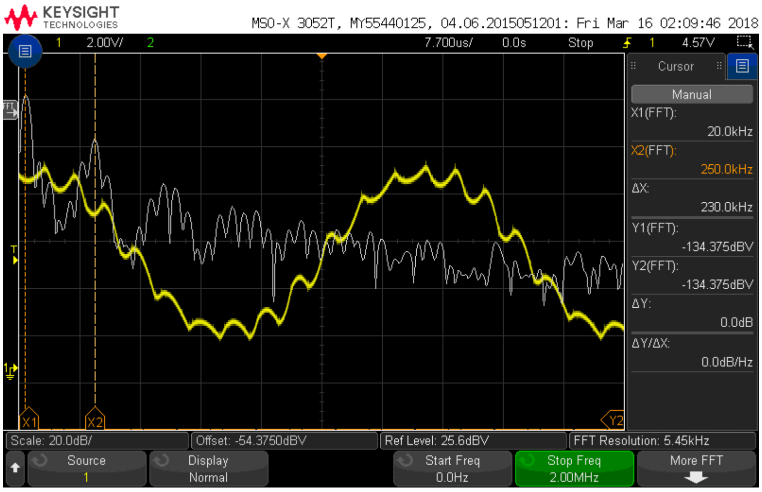



Figure 7.4: Spectrum of signal at "4th order" output

k and n belong to natural numbers.

Finally, Figure 7.5 depicts totally filtered out sine wave signal. No PWM modulation “high frequency” components occur. The filter behaves as expected.

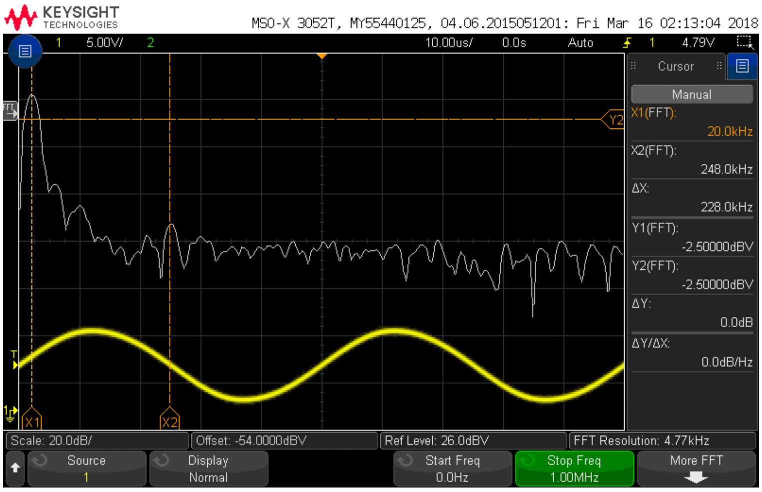



Figure 7.5: Spectrum of signal at "6th order" output

## 7.3 PCB construction

Regarding Class-D amplifier construction, PCB layout has probably the greatest influence on a final sound quality. Good layout practices ensure low level of noise interference, stable function of a circuit and an excellent performance. On the whole, there are two main areas of concern closely correlated to each other - component placing and routing. Following pages will be devoted to briefly sum up important design rules that were applied during PCB layout.

## 7.3.1 Inputs and outputs

Input traces are extremely prone to pick up noise. To lower their exposure to unwanted signal sources, they were designed as short as possible between AC coupling capacitors and amplifying chip's input pins. Moreover, ground trace of input signal was separated from the rest of ground plane, see section "Grounding". Last point to mention, inputs have been kept distant from inductors so as to effectively reduce magnetic coupling.

It is worth to note that during PCB layout it was carefully watched out that all high-current output traces are designed wide enough to provide maximum peak current and no narrow sections are created. These traces were always turned into polygons so as to take up largest surface possible. Failure at this point would result in a disaster - excessively large voltage drops, decreased efficiency and significantly increased level of distortion. Other careful considerations were put in practice to minimize the lengths of traces containing full square waves. That way could be electro-magnetic interference kept at a reasonably low level.

## 7.3.2 Grounding

It is crucial to realize, that each ground track represents a little resistance, across which signals cause formation of unwanted voltage drops. Unless taken care of, these voltage drops add up to useful signals, what consequently results in worsened signal-to-noise ratio.

Because of that, ground tracks were fattened up at every possible point so as to reduce their resistance and nullify ground potentials. To make grounding system even more robust against noise, star-point topology was utilized, since it effectively overcomes ground loop issues. They emerge whenever two or more mains-powered components are connected together and produce spurious hum and buzzing noises. Taking advantage of this knowledge, all ground pins of the essential components were connected separately to one central ground point, see Figure 7.6.

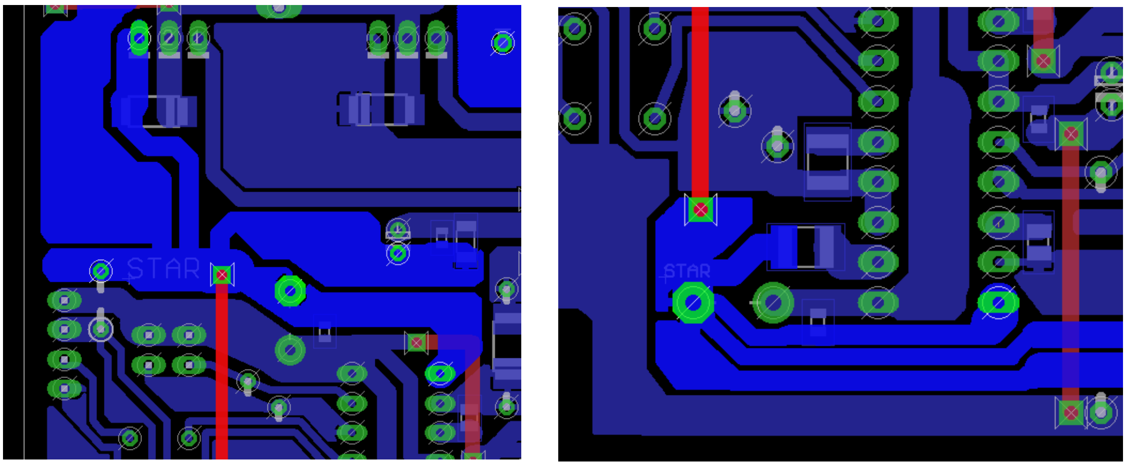



Figure 7.6: Examples of star-point topology

Ideally, there would be no potentials spread alongside grounding paths. But, as already pointed out, some potentials do exist and degrade noise floor of an amplifier.

They always buzz at frequencies very closely related to signal, that is currently being handled. For instance amplifier's CMOS output signals imply high frequency components beginning at system clock and rising up from here because of their high edge rates. Further on, they introduce an uneven current flow caused by switching between inverse logic states, what invokes ground modulation. On the other hand, analog signals are typical for an even current flow interfered by a thermal noise. Thus, it is vital to physically separate whole subsections of PCB working with diametrically different signals. That way can be "noise infiltration" from one subsection to other one effectively attenuated. This concept in PCB design is generally known as partitioning and explains the reason, why analog and digital grounds were secluded from each other. In Figure 7.7 it is presented, how and where analog and digital grounds have been reconnected.

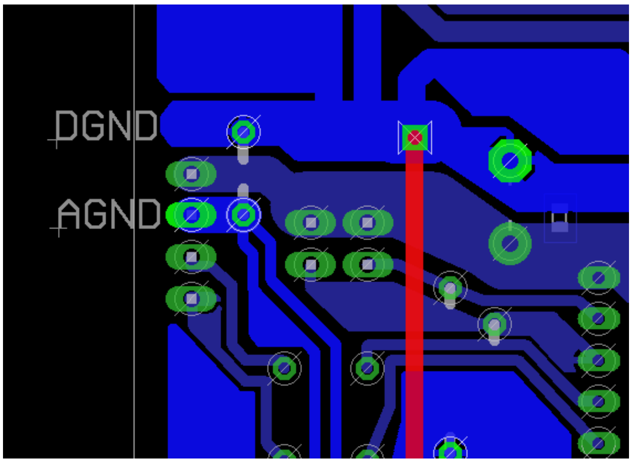



Figure 7.7: Analog and digital ground reconnection

### 7.3.3 Decoupling capacitors

Because of the fact that audio amplifying chip and external MOSFETs switch high currents, there arises a risk of large power supply voltage bounce every time these components switch. Not only current pulses spread around mains plane, the decrease in power supply voltage may result in an unpredictable operation of the chip. To avoid this unwanted situation, close chip and external MOSFET decoupling was put into practice. As an example of how it was done, see Figure 7.8.

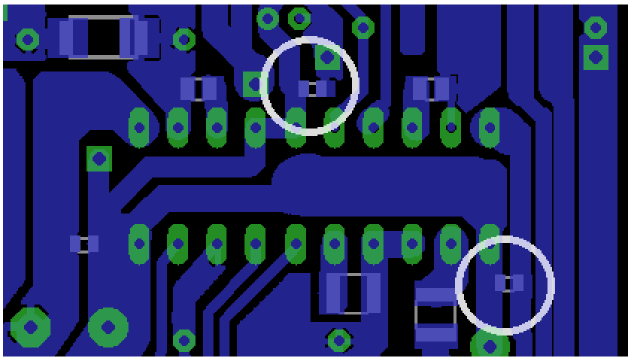


Figure 7.8: Example of decoupling capacitors

Note that, since the PCB was designed as a single layer board, it did not need to be suppressed the temptation of decoupling through vias. Such decoupling slightly decreases its effectiveness, because vias introduce inductive properties, which slow down decoupling capacitors in their operation.

# 8 PERFROMANCE MEASUREMENTS

After device has been constructed, its performance measurements were performed. The measurements were held at university's laboratory with designated measurement hardware, in particular:

- Power supply MCP M10-DP-305E
- Low frequency function generator Agilent 33220A
- TRMS multimeter Fluke 179

Following sections of thesis present results of measurements proceeded.

## 8.1 Frequency response

Frequency response of amplifier was measured at 12 V of power supply voltage. Input voltage $V_1$ has been kept constant during entire measurement process at 100 mV. Effective value of output voltage $V_2$ has been measured using TRMS voltmeter and final gain was calculated using formula presented in section "Frequency response". Note that, selectable gain setting was chosen to equal 32 dB. It was only measured "6th order" probe point. Since it is not possible to measure frequencies higher than 100 kHz, because of sampling theorem, it is pointless to measure "4th order" and "2nd order" probe points. At frequency range from 0 Hz to 100 kHz, their response is totally flat. Values measured and calculated are presented in Table 5.

Table 5: Frequency response, table of values

| **f [Hz]** | **$V_2$ [V]** | **$A_u$ [dB]** | **f [Hz]** | **$V_2$ [V]** | **$A_u$ [dB]** |
|---|---|---|---|---|---|
| 10 | 2.9 | 29.1 | 1000 | 3.8 | 31.6 |
| 20 | 3.2 | 30.1 | 2000 | 3.8 | 31.6 |
| 30 | 3.2 | 30.1 | 3000 | 3.8 | 31.6 |
| 50 | 3.4 | 30.5 | 5000 | 3.8 | 31.6 |
| 70 | 3.4 | 30.5 | 7000 | 3.8 | 31.6 |
| 100 | 3.4 | 30.5 | 10000 | 3.8 | 31.6 |
| 200 | 3.4 | 30.5 | 20000 | 4.5 | 33.0 |
| 300 | 3.4 | 30.5 | 30000 | 4.0 | 32.0 |
| 500 | 3.6 | 31.1 | 50000 | 2.5 | 28.1 |
| 700 | 3.8 | 31.6 | 100000 | 0.6 | 16.1 |

Values calculated were put in graph and they are presented in Figure 8.1. The response matches theoretical expectations. It is almost perfectly flat in range of audible spectrum. At very low frequencies less than 100 Hz it can be noticed the influence of input filter. The lower frequency, the less gain. At "high frequencies" around 20 kHz it can be observed the influence of unmatched load connected to the filter. Once the filter is constructed for load that is lower in value than actual load that will be used in the final device, the filter resonance at cutoff frequency is not attenuated enough and gain rises.

Described situation happened here. Though, gain only rises 2 dB above desired value. The load does not perfectly match filter, but it is still within acceptable bounds. Filter's cutoff frequency was stated to be 60 kHz.

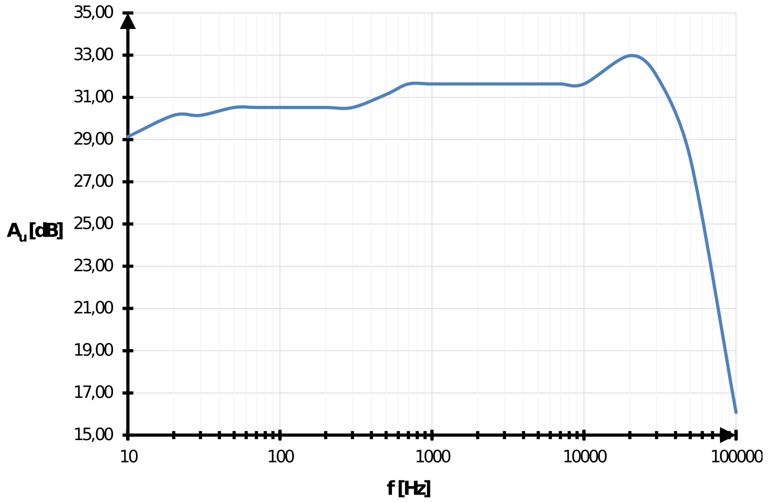



Figure 8.1: Measured frequency response at "6th order" probe point

## 8.2 Output power and efficiency

This section is devoted to measurement of amplifier's output power and its efficiency. Output power $P_2$ of audio signal was measured at all device's power supply voltages $V_{cc}$. Besides measuring output power, it has been kept a record of input current flowing to the device $I_1$ and input power $P_1$ has been calculated as well. Data measured have been evaluated and device's efficiency $\eta$ was stated. Note that, column $V_2$ states maximum possible output RMS voltage, at which no clipping occurs. See Table 6 for values measured and calculated.

Table 6: Output power and efficiency, table of values

| $V_{cc}$ [V] | $V_2$ [V] | $I_1$ [A] | $P_2$ [W] | $P_1$ [W] | $\eta$ [%] |
|---|---|---|---|---|---|
| 10 | 3.3 | 0.35 | 1.4 | 3.5 | 40.0 |
| 11 | 3.6 | 0.39 | 1.6 | 4.2 | 38.4 |
| 12 | 3.9 | 0.42 | 1.9 | 5.0 | 38.2 |
| 13 | 4.1 | 0.46 | 2.1 | 6.0 | 35.3 |
| 14 | 4.6 | 0.52 | 2.6 | 7.2 | 36.1 |
| 15 | 4.9 | 0.55 | 3.1 | 8.3 | 37.0 |
| 16 | 5.3 | 0.59 | 3.5 | 9.5 | 36.5 |
| 17 | 5.6 | 0.62 | 4.0 | 10.5 | 37.5 |
| 18 | 5.9 | 0.67 | 4.4 | 12.1 | 36.6 |
| 19 | 6.3 | 0.70 | 4.9 | 13.3 | 36.8 |
| 20 | 6.4 | 0.72 | 5.2 | 14.4 | 35.9 |

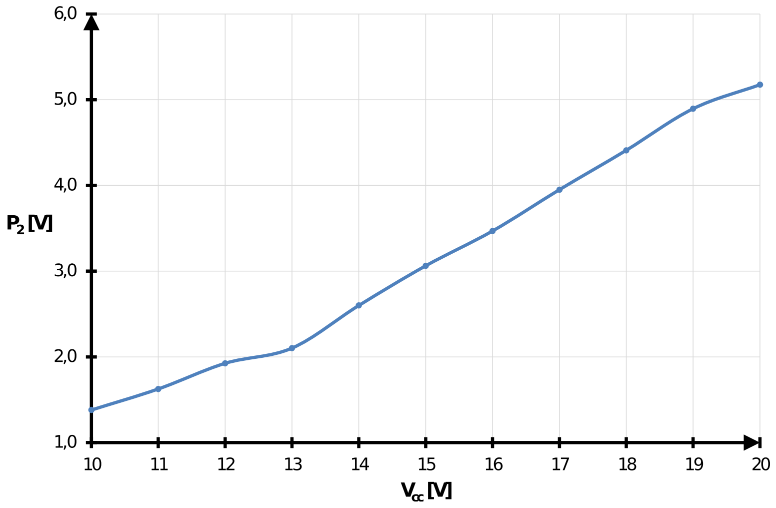



Figure 8.2: Measured output power at different power supply voltages

Figure 8.2 presents relation between maximum output power and power supply voltage. It can be seen pure linear relationship. Maximum output power per channel in SE configuration is 5.2 W.

Device's efficiency is very poor. It is half the efficiency of commercial devices. The reason for such bad performance is output driver built of external MOSFETs. Since the transistors heavily shoot through each other, large part of input current is shorted directly to ground. If there had been no external driver circuit included in the design, the efficiency would have shot up rapidly in value.

## 8.3 Output impedance

Output impedance $Z_{out}$ has been measured using procedure explained in theoretical section "Output impedance". Measurement was held at three power supply voltages $V_{cc}$ equal 12 V, 15 V and 18 V and 1 kHz input sine wave signal. Afterwards, damping factor D was calculated. Measured and calculated values are presented in Table 7. Note that, $V_{20}$ stands for output TRMS voltage measured without load connected and voltage $V_2$ stands for output TRMS voltage measured with load connected.

Table 7: Output impedance and damping factor, table of values

| $V_{cc}$ [V] | $V_{20}$ [V] | $V_2$ [V] | $Z_{out}$ [Ω] | D [-] |
|---|---|---|---|---|
| 12 | 5.68 | 5.04 | 1.02 | 7.88 |
| 15 | 5.52 | 4.96 | 0.90 | 8.86 |
| 18 | 11.1 | 10.40 | 0.54 | 14.86 |

Output impedance is roughly equal to 1 Ω at 12 V of power supply voltage and decreases in value with increasing supply voltage. Output impedance is still relatively high for typical Class-D amplifier. Though, typical Class-D amplifier does not comprise 6th order output filter with three coils connected in series prior to output connectors.

Because of the large filter, worsened output impedance could be predicted. Damping factor remains less than 15 for all supply voltages.

## 8.4 Input impedance

Measurement of input impedance $Z_{in}$ was held at 12 V of power supply voltage. Since input impedance of the device is frequency dependent, it was decided to perform measurement only at one, precise frequency and that is 1 kHz. At such frequency, impedance of input DC-blocking capacitor is very low and output of the measurement will represent input impedance of amplifying chip. That value depends on gain settings $G_1$ and $G_0$ of the chip. For variations in gain settings and corresponding input impedance that has been measured, see Table 8.

Table 8: Input impedance, table of values

| $G_1$ [V] | $G_0$ [V] | $Z_{in}$ [kΩ] |
|---|---|---|
| 0 | 0 | 58 |
| 0 | 12 | 28 |
| 12 | 0 | 14 |
| 12 | 12 | 8.5 |

## 8.5 Slew rate

Slew rate was measured at 12 V of power supply voltage and at 1 kHz input signal. The amplifier was initially fed with 1 kHz sine wave. The amplitude of input signal was set to a value, when amplifier achieves its maximum output power. Sine wave was then exchanged for square wave and it was measured rise time and fall time of each signal edge and corresponding voltage change $\Delta V$. Results of measurement are presented in Table 9.

Table 9: Slew rate, table of values

| $\Delta V_{rise}$ [V] | $\Delta V_{fall}$ [V] | $\Delta t_{rise}$ [µs] | $\Delta t_{fall}$ [µs] | $SR_{rise}$ [V/µs] | $SR_{fall}$ [V/µs] |
|---|---|---|---|---|---|
| 7.92 | 6.0 | 9.8 | 6.8 | 0.81 | 0.88 |

## 8.6 Harmonic distortion and THD+N

Harmonic distortion and THD+N was measured at 12 V of power supply voltage and 1 kHz input signal with 100 mV effective value. Output signal had effective value of 3.8 V.

Harmonic distortion at 2 kHz was measured to be 0.7 % and at 3 kHz to be 0.08 %. These results are perfect, since they clearly state that amplifier does not distort amplified signal.

THD+N was measured to be 5.21 %. This result in significantly worse than harmonic distortion presented above, though, it can be easily explained. Output signal contains sharp pulses at chip's sampling frequency, which are result of switching load through large, inductive filter. The switching appears to measuring device as a noise and degrades final performance measurements of the device.

In summary, the device introduces almost no distortion to signal amplified. Though, due to way, how input signal is being processed, the device introduces switching peaks, which worsen noise floor.

## 8.7 Bridge-tied-load output power

The last section of performance measurements devotes to measuring output power at BTL configuration. Since maximum output power in SE configuration has already been stated to 5.2 W, it is expected maximum output power of 20.8 W in BTL configuration.

Though, maximum output power in BTL configuration could not be measured. Once the control switch is flipped to BTL configuration, the device starts to totally malfunction. Output signal is excessive in value, around 80 V peak to peak, filter's coils dangerously heat up and output resistors remain cold all the time.

Tens of hours had been spent to get the BTL configuration to work, though, without any success. The schematic has been checked, the PCB has been checked, the measuring device has been replaced with battery-powered one, but problem remains. It seems like output filter in configuration utilized cannot work in BTL configuration. This statement also supports the fact that once 6th order filter is replaced with 2nd order counterpart, BTL configuration starts to function properly, as expected.

# 9 CONCLUSION

Bachelor's thesis presents construction process of Class-D audio amplifier. During the design, emphasis was mainly imposed on robustness and demonstrativeness of the device. At the end, the objectives of the thesis have been met at all points. A brief summary of what has been done during preceding semesters is presented below.

Construction of a bare amplifier consisting of just one amplifying chip connected as datasheet suggests is quick, easy and robust. It does not imply any complication with power supply, heat sinking or operation within different conditions.

Though, once external driver is required to implement, the design becomes significantly harder. It is the root of numerous limitations and complications. Shoot-through effect that occurs in push-pull transistor pair causes overheating issues of originally working amplifier even at low power supply voltages. Many hours had been spent in order to attenuate the unwanted effect and make it possible for an amplifier to operate without the need for large heat sinking. Although several working suggestions on shoot-through effect protection circuits have been presented and utilized in the device, the effect still persists and must be borne in mind during entire design process. Since the effect persists, it significantly worsens effectivity of amplifier. Next time, e.g. in other thesis, construction of external driver should be omitted. It is highly recommended to utilize commercial push-pull driver chip instead of inventing the wheel all over again.

Further botherations had been brought to the design by output analog filter, which had to demonstrate the creation of output signal from PWM modulated wave. Initially, it was tried to design the filter using only computer simulations and mathematical calculations, but such approach to the problem is wrong. It cannot be predicted the shape of output signal only based on frequency response of the filter. Due to this fact, the filter had to be designed experimentally side by side theoretical calculations. In the end, a sophisticated filter of 6th order was successfully constructed, which clearly shows, how PWM modulation components influence output signal shape.

Final, probably the most important step in the design was testing of the device constructed. It was carefully watched out to observe long-term device's normal operation, particularly, that it does not excessively heat up or stops outputting signal for no reason. It has also been observed that protection circuits against continuous low overvoltage are not mistakenly triggered and do not turn off the device, when they are not supposed to. These circuits have also been tested for overvoltage state, more specifically that they do not unexpectedly turn on power to protected device and do not get damaged by overvoltage neither.

It was tried the best to build a device that will serve the laboratory for many years.

The device built demonstrates working principles of numerous block sections of general Class-D audio amplifier. In future, the thesis can be extended and amplifying chip replaced by separate blocks, which would demonstrate, how PWM wave is created from input signal. Such device covering entire topic of Class-D amplifiers would be a masterpiece.

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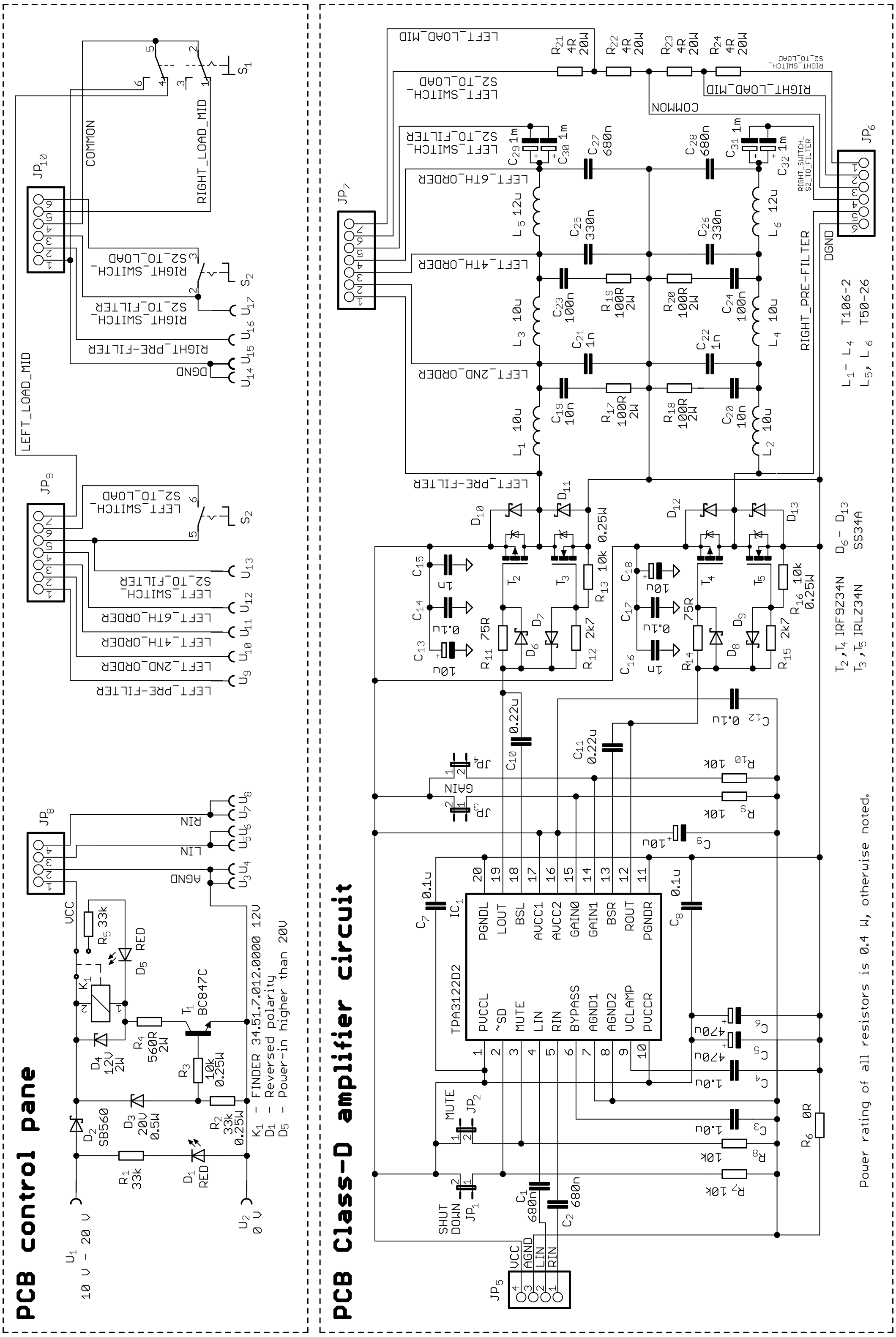
# 11 ABBREVIATIONS LIST

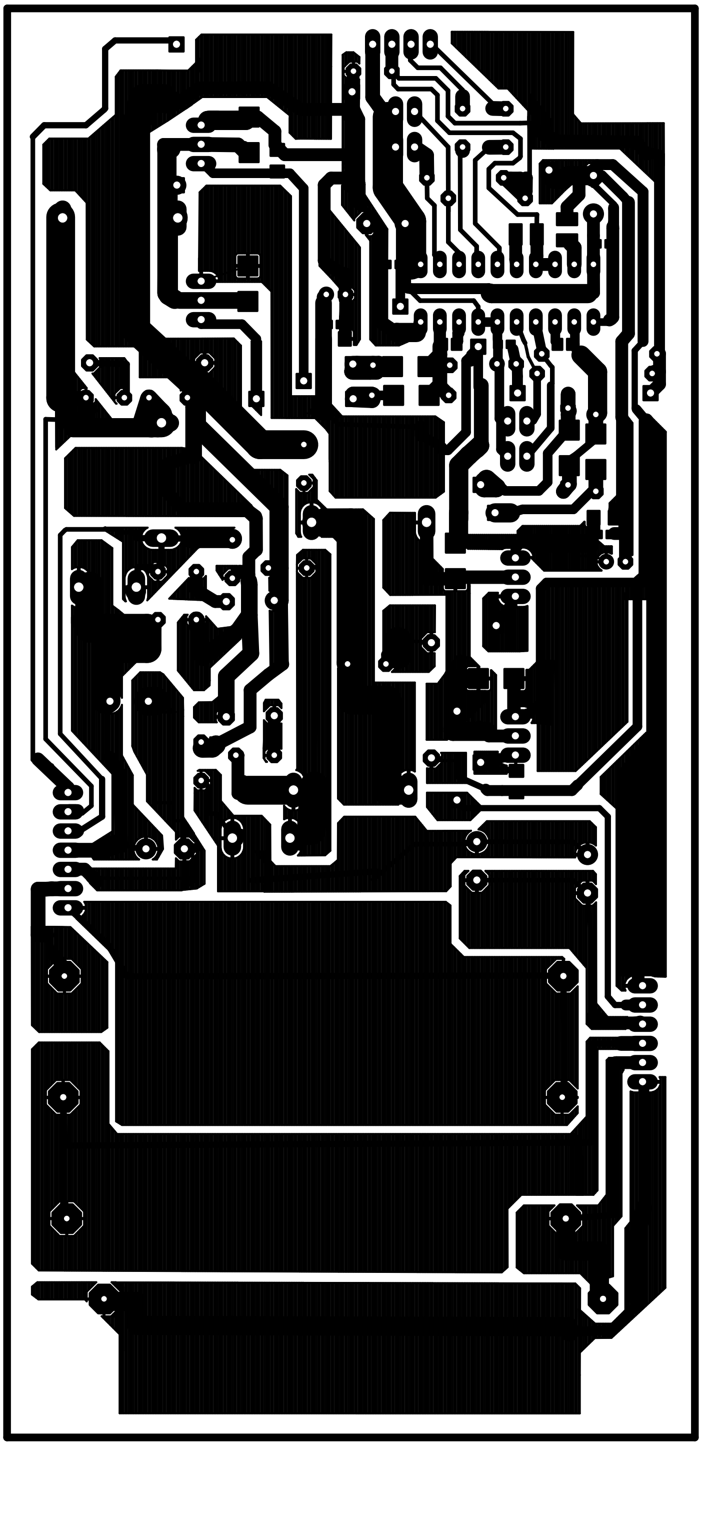
| | |
|---|---|
| PCB | printed circuit board |
| CPP | component placement plan |
| IC | integrated circuit |
| THD | Total Harmonic Distortion |
| FET | field-effect transistor |
| MOSFET | metal-oxide-semiconductor field-effect transistor |
| SE | single-ended |
| BTL | bridge-tied-load |
| PDIP | plastic dual in-line package |
| +Vcc | positive power supply voltage |
| -Vcc | negative power supply voltage |
| $R_{DSon}$ | drain-source on resistance |
| SMD | surface mount device |
| TH | through-hole device |
| ID | inner diameter |
| OD | outer diameter |
| LS | lead spacing |

# A CONSTRUCTION PLANS

## A.1 Schematic for PCB construction

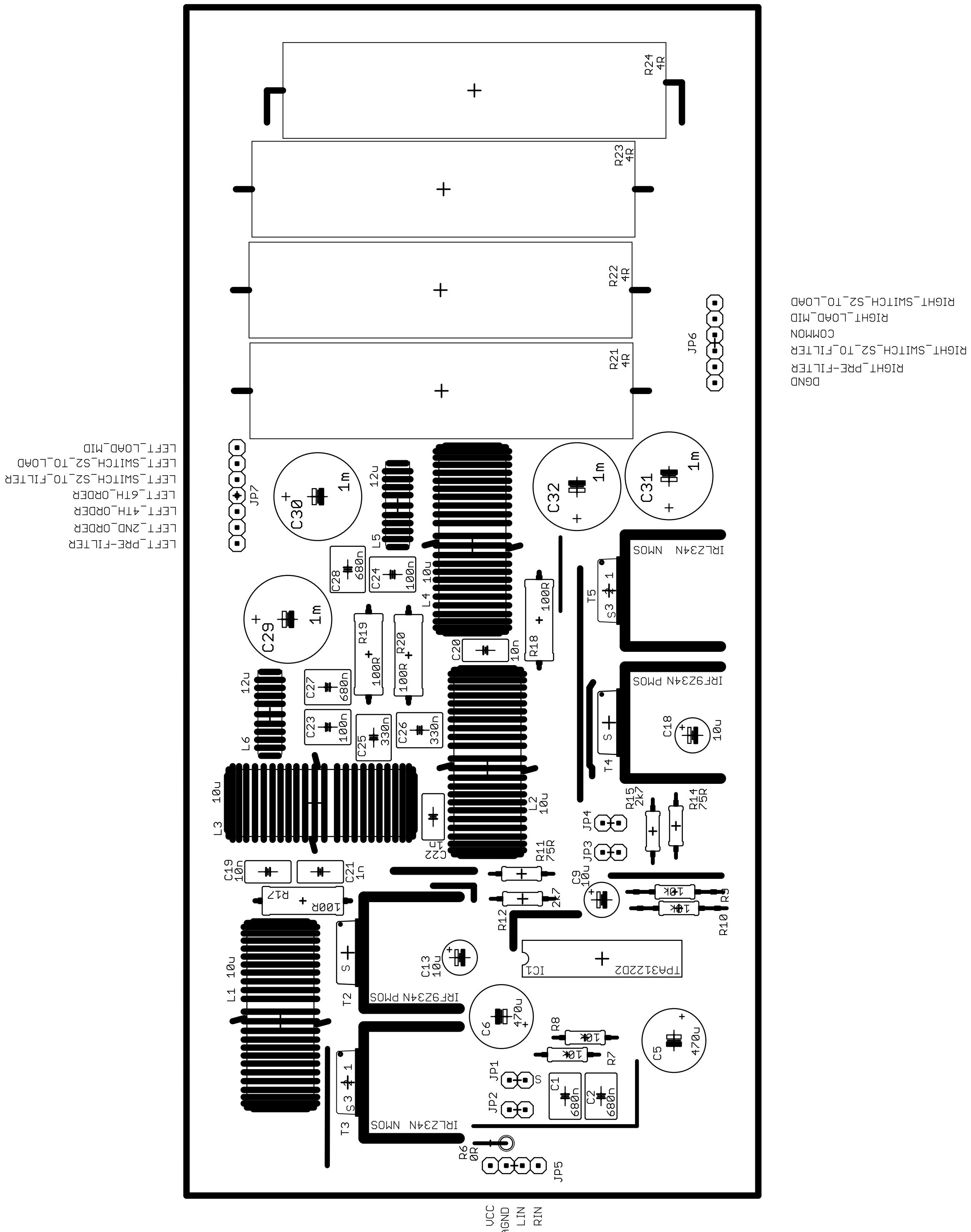


## A.2 Class-D amplifier circuit, PCB



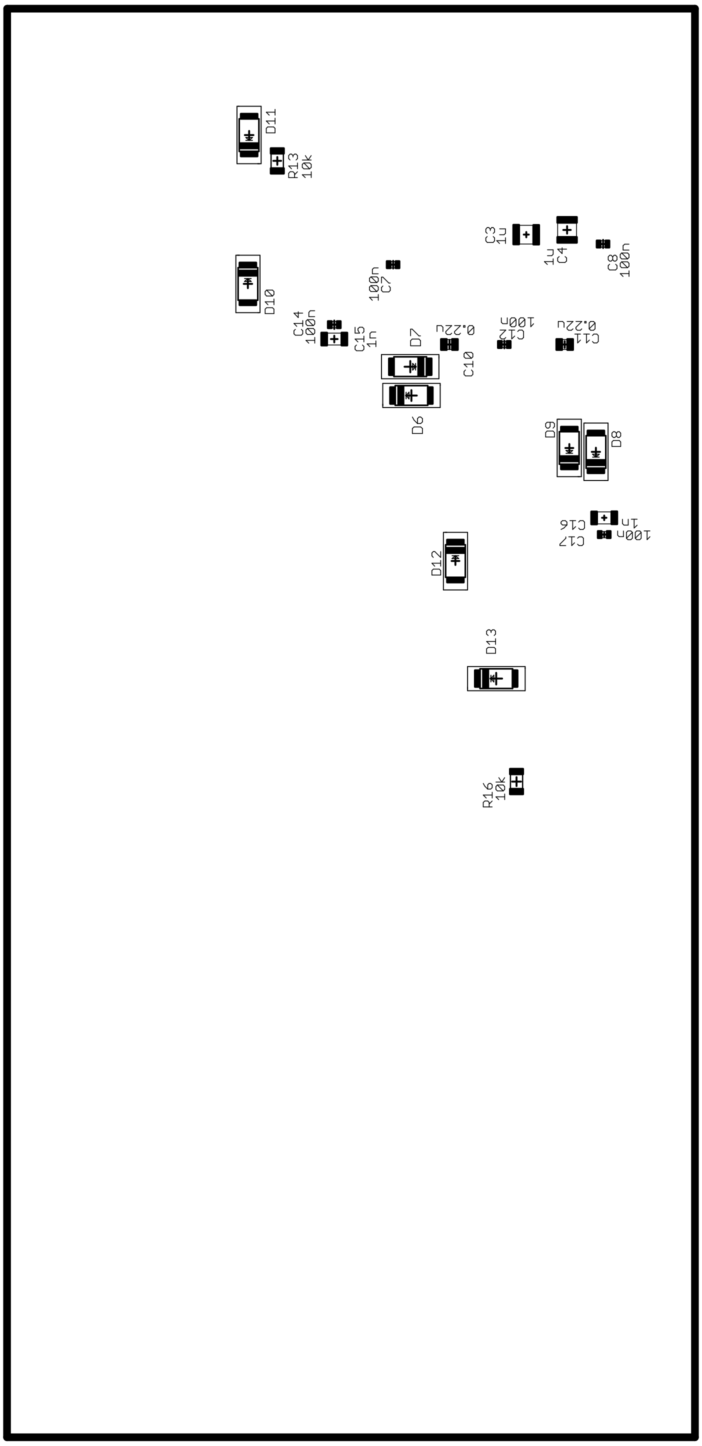
Attachment 1: PCB for Class-D amplifier circuit (scale 1:1, dimension 189 x 91 mm, BOTTOM layer)

# A.3 Class-D amplifier circuit, CPP



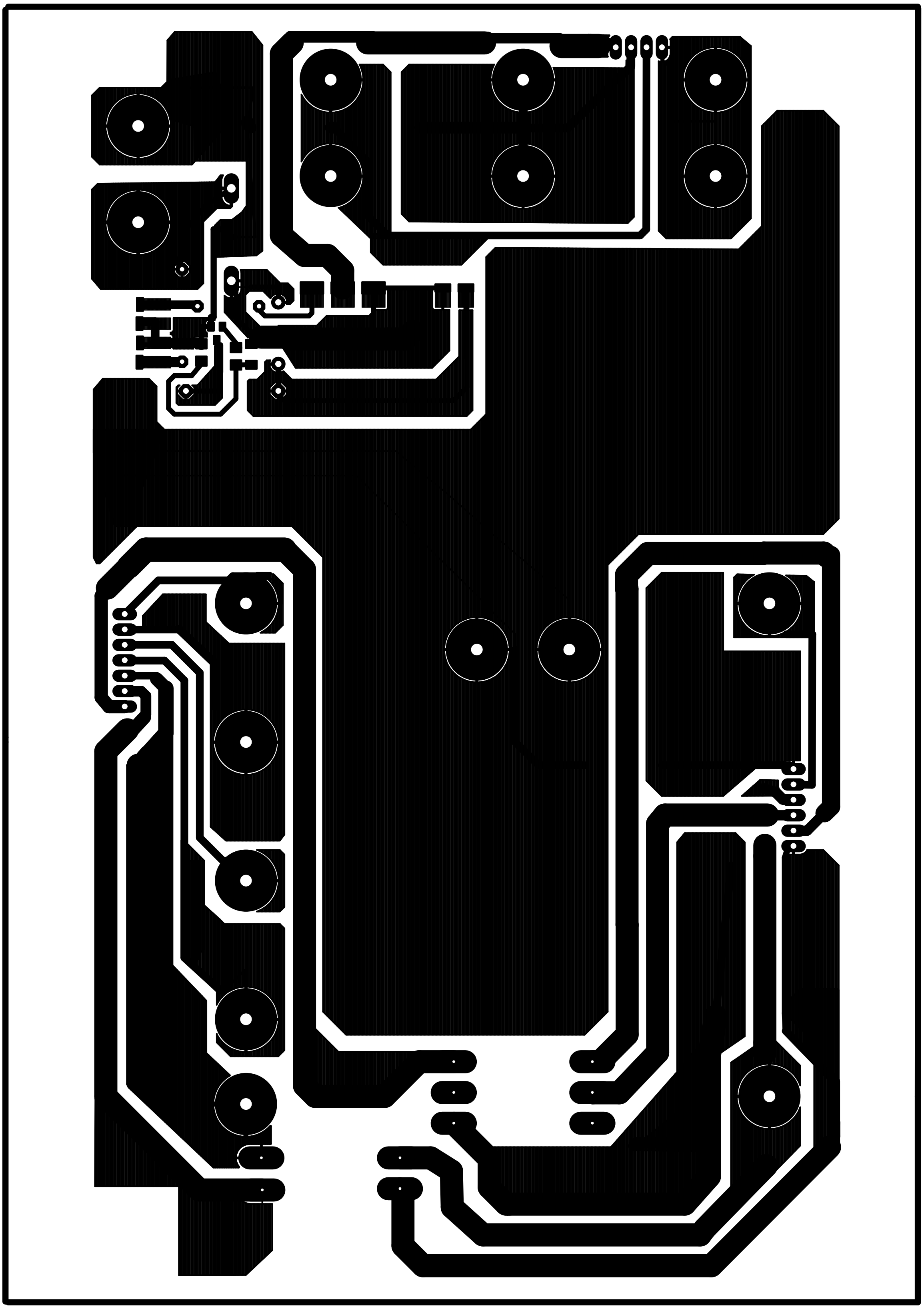

Attachment 2: CPP for Class-D amplifier circuit (scale 1:1, dimension 189 x 91 mm, TOP layer)

## A.4 Class-D amplifier circuit, CPP



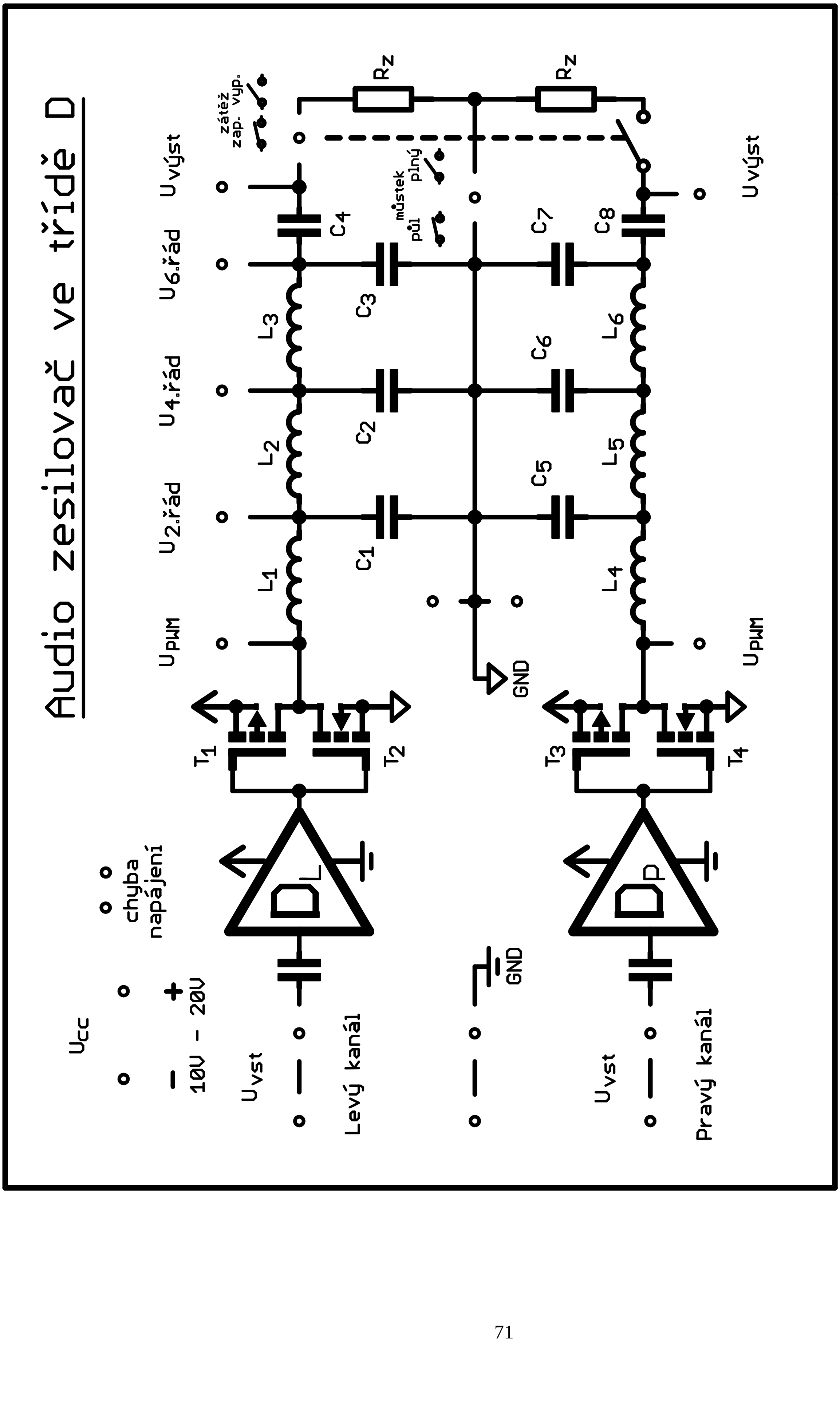

Attachment 3: CPP for Class-D amplifier circuit (scale 1:1, dimension 189 x 91 mm, BOTTOM layer)

## A.5 Control panel, PCB



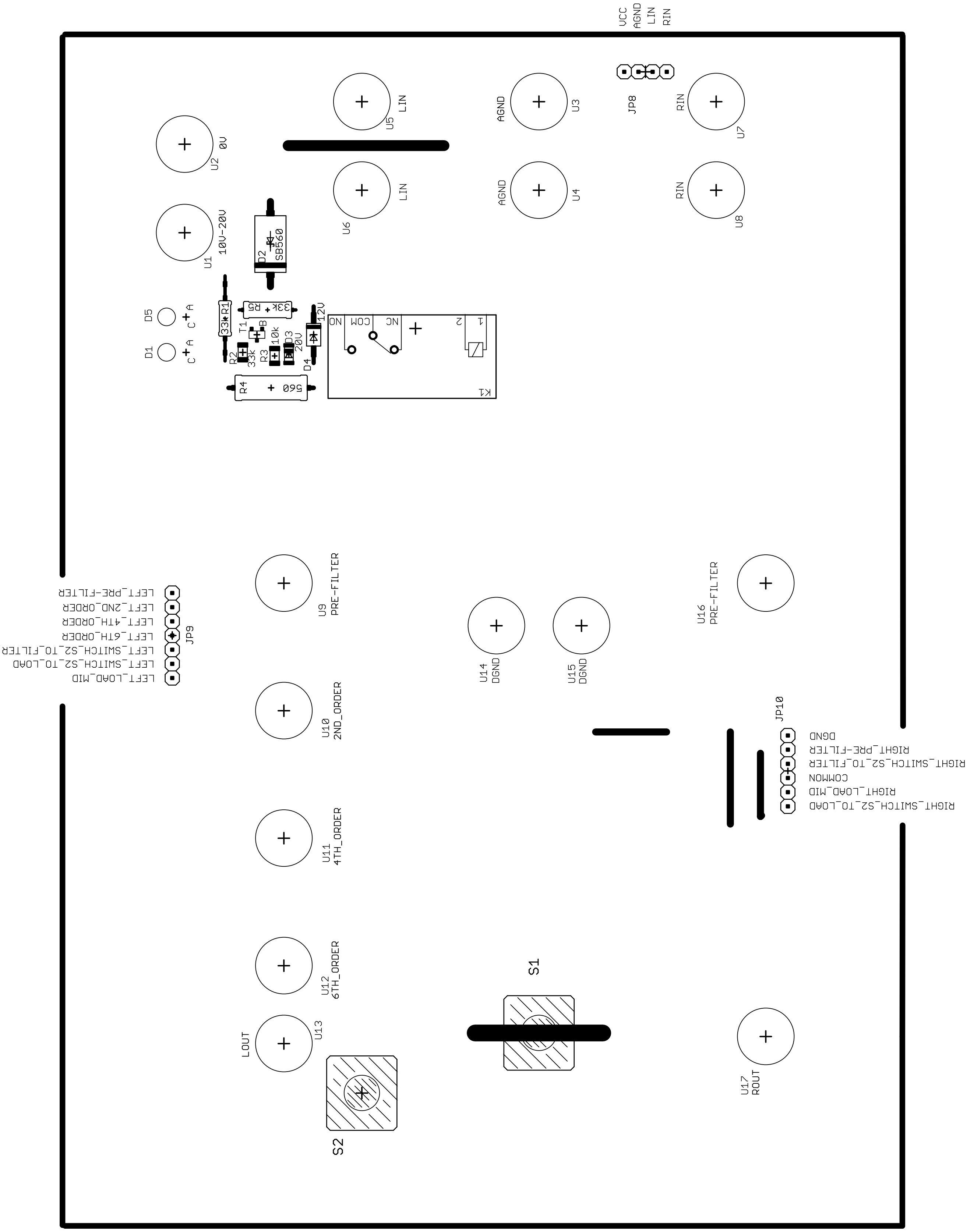
Attachment 4: PCB for Control panel (scale 1:1, dimension 214 x 150 mm, BOTTOM layer)

## A.6 Control panel, PCB




Attachment 5: PCB for Control panel (scale 1:1, dimension 214 x 150 mm, TOP layer)

## A.7 Control panel, CPP




Attachment 6: CPP for Control panel (scale 1:1, dimension 214 x 150 mm, BOTTOM layer)

# B PARTS LIST

## B.1 Capacitors

| Part | Value | Package | Description |
|---|---|---|---|
| C1, C2, C27, C28 | 680n, 63 V | TH, LS 5 mm | DC film capacitor, metallised, PET |
| C3, C4 | 1u, 50 V | SMD, 1210 | Multilayer ceramic capacitor, X7R |
| C5, C6 | 470u, 35 V | TH, LS 10 mm | Electrolytic capacitor, radial leaded |
| C7, C8, C12 C14, C17 | 100n, 50 V | SMD, 0603 | Multilayer ceramic capacitor, X7R |
| C9, C13, C18 | 10u, 35 V | TH, LS 2 mm | Electrolytic capacitor, radial leaded |
| C10, C11 | 220n, 50 V | SMD, 0603 | Multilayer ceramic capacitor, X7R |
| C15, C16 | 1n, 50 V | SMD, 0603 | Multilayer ceramic capacitor, X7R |
| C19, C20 | 10n, 250 V | TH, LS 5 mm | DC film capacitor, PET |
| C21, C22 | 1n, 100 V | TH, LS 5 mm | DC film capacitor, PET |
| C23, C24 | 100n, 100 V | TH, LS 5 mm | DC film capacitor, low ESR, PET |
| C25, C26 | 330n, 63 V | TH, LS 5 mm | DC film capacitor, PET |
| C29, C30, C31, C32 | 1m, 35 V | TH, LS 12.5 mm | Electrolytic capacitor, low ESR, radial leaded |

## B.2 Diodes

| Part | Type | Package | Description |
|---|---|---|---|
| D1, D5 | BL-B5141-L | TH, OD 3 mm | RED LED |
| D2 | SB560 | TH, DO201AD | Schottky diode |
| D3 | BZV55C20SMD | SMD, SOD80 | Zener diode, 20 V, 0.5 W |
| D4 | BZY012 | TH, DO41 | Zener diode, 12 V, 2 W |
| D6, D7, D8, D9, D10, D11, D12, D13 | SS34A | SMD, SMA | Schottky diode |

## B.3 Integrated circuits

| Part | Type | Package | Description |
|---|---|---|---|
| IC1 | TPA3122D2 | TH, DIL20 | Class-D amplifying chip |

## B.4 Wire-to-board connectors

| Part | Type | Package | Description |
|---|---|---|---|
| JP1, JP2, JP3, JP4 | 2 pins | TH, LS 2.54 mm | |
| JP5, JP8 | 4 pins | TH, LS 2.54 mm | |
| JP6, JP10 | 6 pins | TH, LS 2.54 mm | |
| JP7, JP9 | 7 pins | TH, LS 2.54 mm | |

## B.5 Relays

| Part | Type | Package | Description |
|---|---|---|---|
| K1 | FINDER 34.51.7.012.0000 | TH | 12 V DC coil relay |

## B.6 Coils

| Part | Value | Package | Description |
|---|---|---|---|
| L1, L2, L3, L4 | 10u | T106-2 | Iron powder toroidal core, 27 turns |
| L5, L6 | 12u | T50-26 | Iron powder toroidal core, 20 turns |

## B.7 Resistors

| Part | Value | Package | Description |
|---|---|---|---|
| R1, R5 | 33k, 0.4 W | TH, 0204 | |
| R2 | 33k, 0.25W | SMD, 1206 | |
| R3 | 10k, 0.25W | SMD, 1206 | |
| R4 | 560R, 2 W | TH, 0411 | |
| R6 | 0R | | A piece of wire |
| R7, R8, R9, R10 | 10k, 0.4 W | TH, 0204 | |
| R11, R14 | 75R, 0.4 W | TH, 0204 | |
| R12, R15 | 2k7, 0.4 W | TH, 0204 | |
| R13, R16 | 10k, 0.25 W | SMD, 1206 | |
| R17, R18, R19, R20 | 100R, 2 W | TH, 0411 | |
| R21, R22, R23, R24 | 4R, 20 W | TH, KERAM | |

## B.8 Switches

| Part | Type | Package | Description |
|---|---|---|---|
| S1, S2 | P-KNX2 | | 125 V, 6 A |

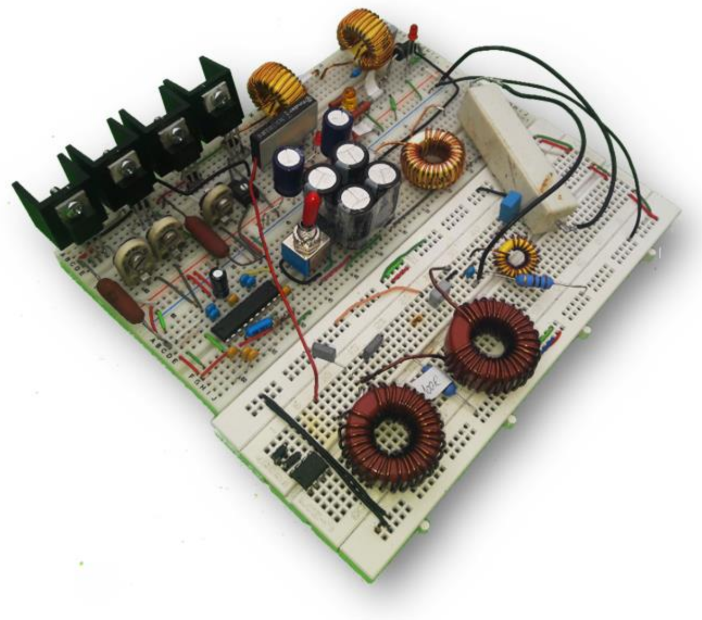
## B.9 Transistors

| Part | Type | Package | Description |
|---|---|---|---|
| T1 | BC847C | SMD, SOT23 | bipolar |
| T2, T4 | IRF9Z34N | TH, TO220AB | MOSFET |
| T3, T5 | IRLZ34N | TH, TO220AB | MOSFET |

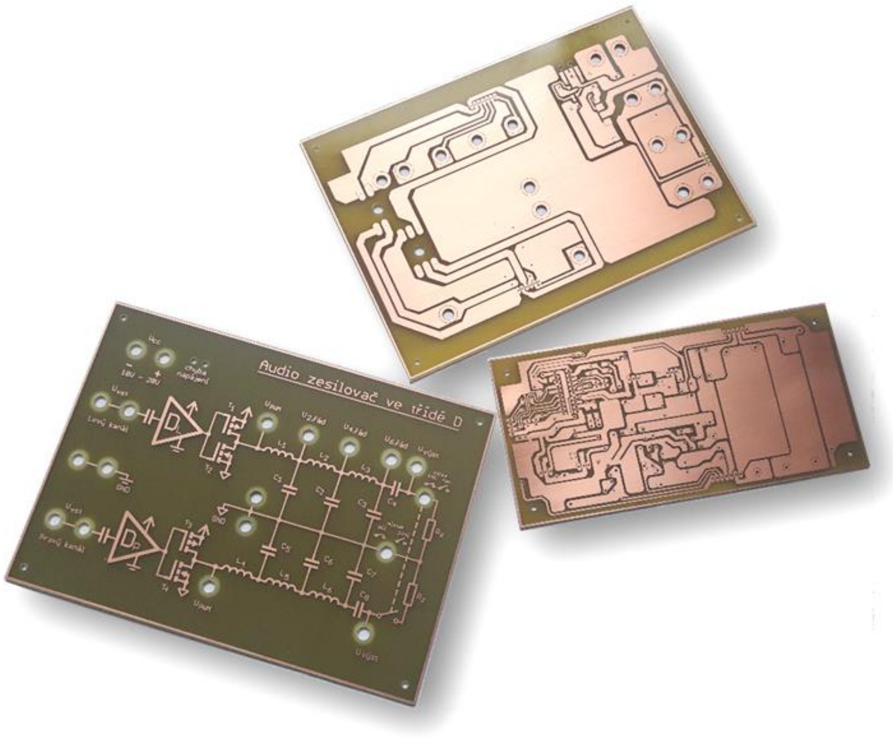
## B.10 Connectors

| **Part** | **Type** | **Package** | **Description** |
|---|---|---|---|
| U1 | 24.246.1 | ID 4 mm | Red banana connector, panel mount |
| U2, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17 | 24.246.2 | ID 4 mm | Black banana connector, panel mount |

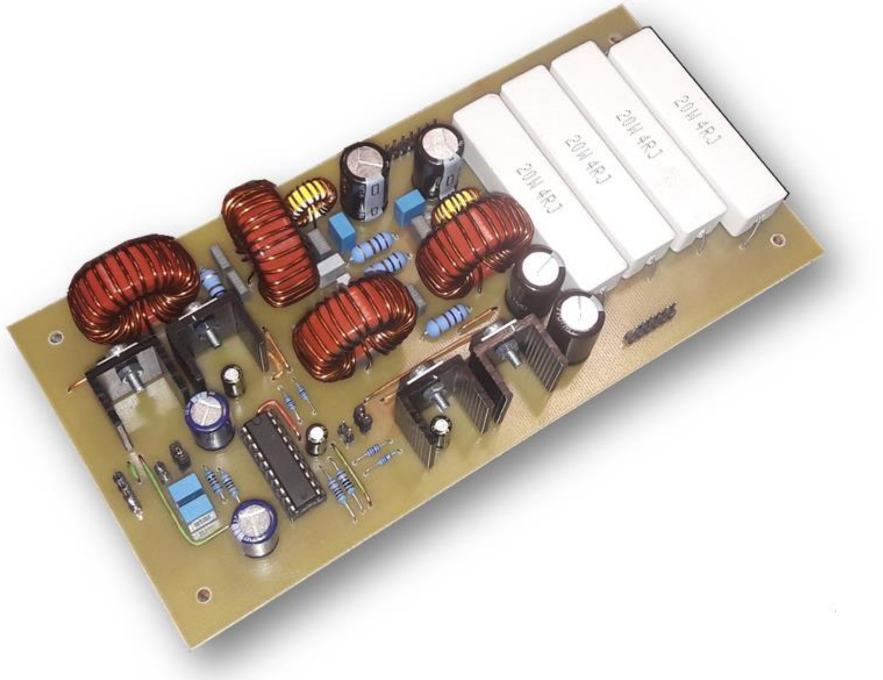
# C PHOTO GALLERY



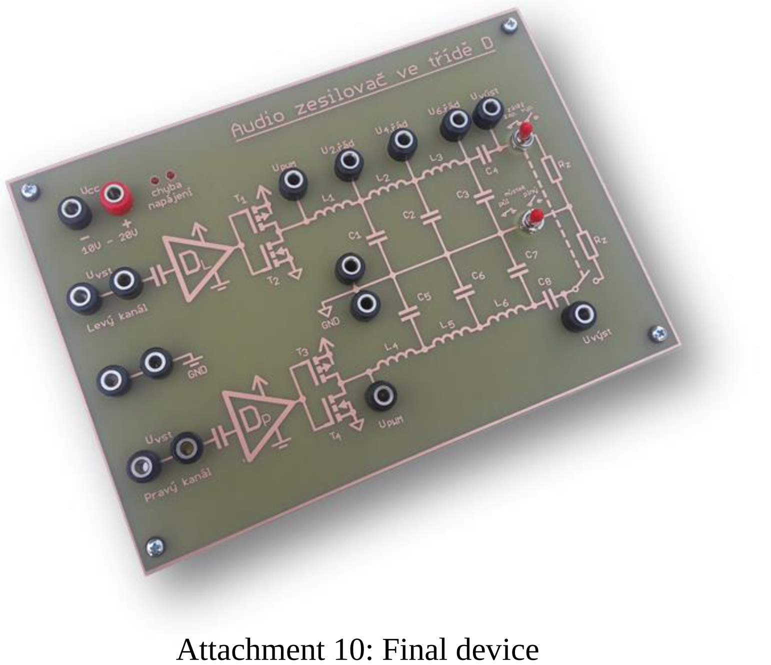
Attachment 8: Prototype of amplifier circuit built on a breadboard




Attachment 7: Brand new PCBs




Attachment 9: PCB with all components placed




Attachment 10: Final device