X-BAND EARTH OBSERVATION SATELLITE SOFTWARE DEFINED RADIO

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Abstract: This article presents the digital baseband receiver for signals from the EOS-PM-1 X-band Earth observing satellite. The conventional SDR is used to provide samples of the baseband signal. The MATLAB software is used for simulating the O-QPSK satellite signal in baseband, algorithms for the Doppler frequency shift and additional frequency offset removal, carrier phase synchronization, symbol timing synchronization and the phase ambiguity removal.

Keywords: Software defined radio, satellite, X-band, Doppler shift, carrier phase synchronization.

1 INTRODUCTION

Remote sensing information is essential for many countries around the world and some of them require everyday real-time local weather data to handle critical situations. Such places cannot afford to wait for the regular data updates provided by the international meteorological institutions and are forced to purchase direct broadcast receiver stations accessing the local weather satellite broadcast. However, commercially available stations can be quite expensive getting up to tens of thousands of euros. It is a goal of this thesis to design a digital baseband receiver capable of real time satellite data reception. This receiver is designed to receive the broadcast signal of the EOS-PM-1 satellite and the implemetation is done using an SDR (Software Defined Radio) and Xilinx Zynq-7000 FPGA.

2 EOS-PM-1 (AQUA)

Aqua is one of the EOS program Earth observing satellites. It is gathering measurements of the Earth's atmosphere using six main on-board instruments and continuously broadcasting the local meteorologic data to the ground stations worldwide. The main downlink parameters are listed in table 1.

Table 1: Main downlink parameters of the EOS-PM-1.

Parameter	Value
Data rate	15 Mb/s ± 1.8 kb/s
Carrier freq.	8160 MHz
EIRP	25 W
Bandwidth (1st to 1st null)	15 MHz
Channel bandwidth	150 MHz
Modulation	SQPSK
Frame length	1024 Bytes
Polarization	RHCP

EOS-PM-1 is streaming data with a fixed data-rate of 15 Mbit/s. The data is Reed Solomon and PRBS encoded and organized into frames, each beginning with a pre-defined synchronization word (the „ASM“). The rectangular pulses are then Offset-QPSK modulated without any pulse-shaping filter so the main spectral lobe is 15 MHz wide.

3 DIGITAL RECEIVER DESIGN

3.1 SDR

The SDR utilization in this project is preliminary. The final design requires ADC – FPGA cooperation on a single development board.

For testing purposes the PXIe-5622 digitizer module will be used as the SDR. The sampling frequency can go up to 150 MS/s and the internal digital structure includes the frequency translator (putting signal into baseband) and decimation filter (reducing the sampling rate without the risk of aliasing).

3.2 SDR BASEBAND SIGNAL

The sampling frequency of the SDR has been set just above 2 samples per symbol (16.6 MSPS) in order to minimise the implementation resources but also to prevent the information loss. The SDR digitizes the intermediate frequency signal (centered at ~20 MHz) and transfers it into the complex baseband signal (see figure 1-left). Such a signal is affected by frequency offset caused by the Doppler frequency shift (figure 1-right).

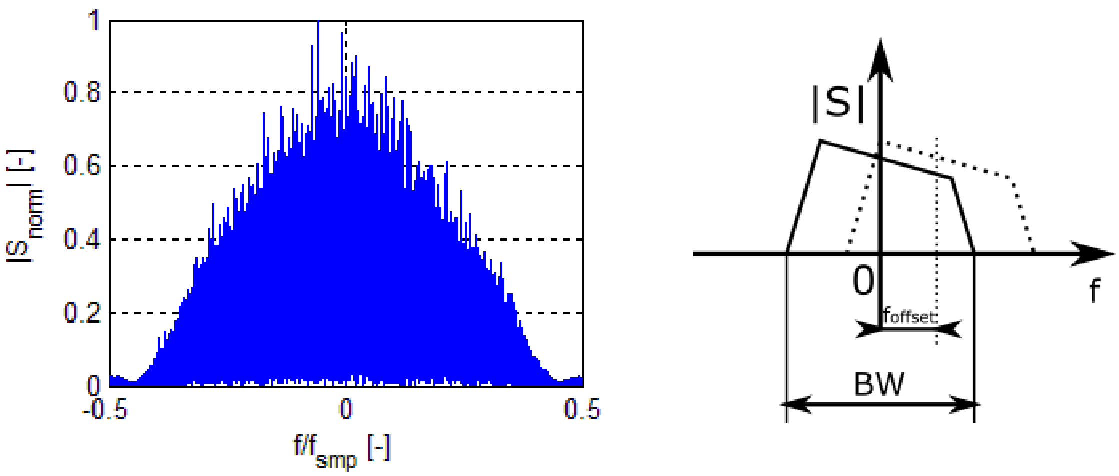

Figure 1: Simulation of the baseband spectrum (left) and the frequency offset illustration (right).

3.3 CARRIER AND SYMBOL SYNCHRONIZATION

The first part of the receiver design is depicted in figure 2. The Costas loop [3][4] maintains the carrier synchronization (first clock domain) and it is capable of compensating the frequency offset (max. estimation 150 kHz). After the Costas loop has locked itself, the symbols need to be resampled so they can be detected more easily (symbol detector requires integer number of samples per symbol). The resampling is done in a feedback loop driven by Gardner Timing Error Detector (TED) [5]. The TED keeps adjusting the Farrow resampler [6] which provides the sample interpolation in the desired sampling moments (highest SNR).

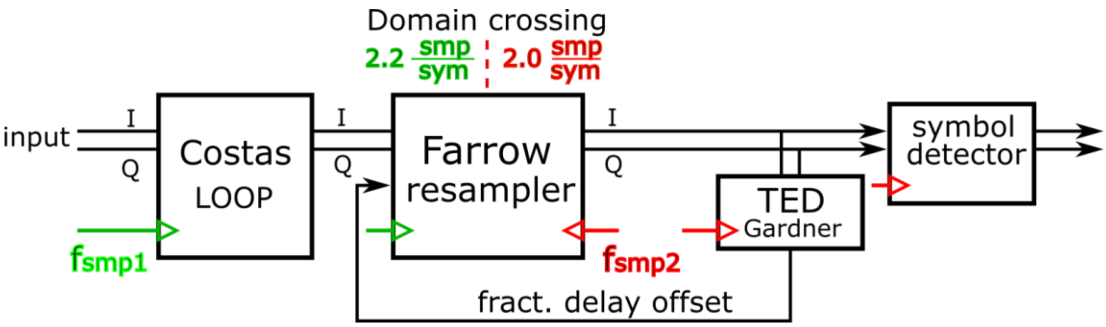

Figure 2: Carrier and symbol synchronization (simplified schematic).

3.4 ASM DETECTION

The ASM detector follows right after the symbol detector and provides essential timing information for the symbol sampling. The exact position of the ASM correlation peak triggers the symbol sampler (picking only the odd/even samples) and the PRBS decoder.

Since the original bitstream has been separated into I and Q channel, the 32-bit ASM must also be separated into two 16-bit words where each has to be correlated with both I and Q channel samples. (see figure 3). Combining all 4 correlation results provides enough information to compensate the phase ambiguity of the OQPSK Costas loop.

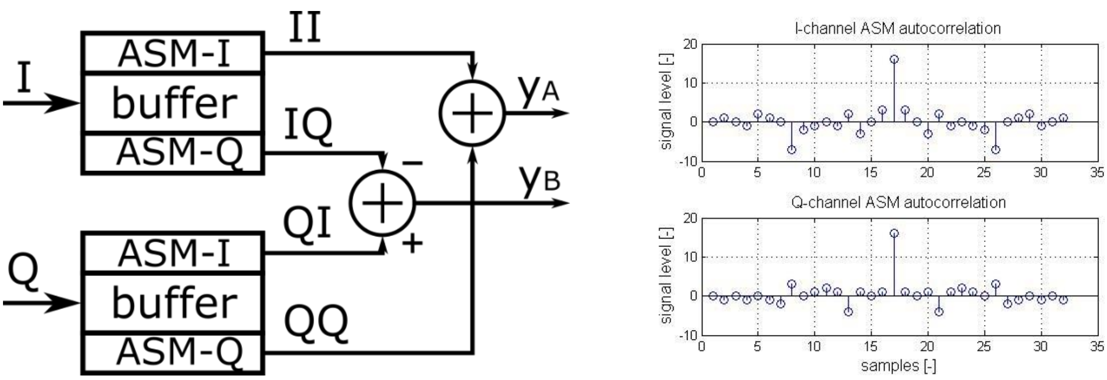

Figure 3: ASM detection block schematic (left), ASM autocorrelations (right).

The correlation peak value is always equal to 16 (32 for y_A and y_B) thanks to the preceding symbol detection block (see figure 4).

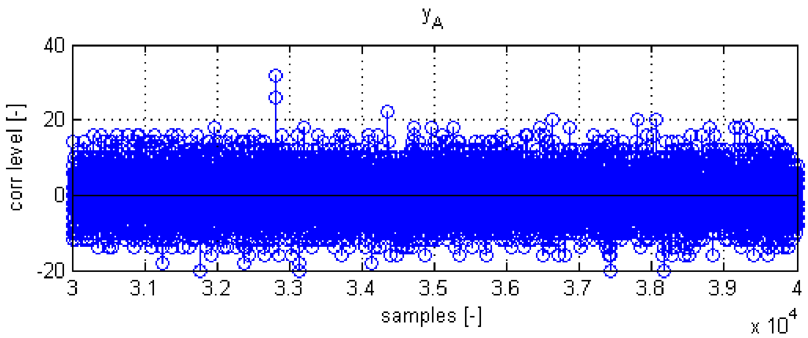

Figure 4: ASM correlation for random data.

4 CONCLUSION

The functionality of the digital receiver has been successfully simulated in MATLAB. The input signal has been modelled using limited information from [1][2]. It remains to be tested on practical data samples whether the signal was modelled correctly or not.

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