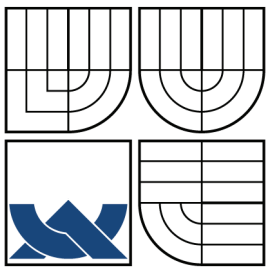

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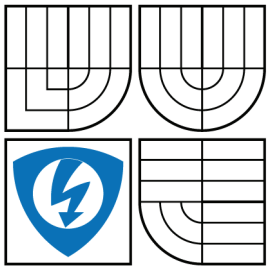

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LINEAR FUNCTION BLOCKS FOLLOWING RECENT TRENDS IN ANALOG CIRCUIT DESIGN

HABILITATION THESIS
HABILITAČNÍ PRÁCE

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BRNO 2015

CONTENTS

PREFACE

Research in analog signal processing is significantly considered in the analyses and application possibilities of different active building blocks (ABBs). Operational amplifier played an important role as an active building block on the market. Therefore, enormous number of publications exist in the literature on various analog electronics circuits using operational amplifiers. However, new integrated analogue circuit applications have emerged and the performance requirements for analogue circuits have changed. Operational amplifiers circuits have limited bandwidth at high closed-loop gains due to the constant gain-bandwidth product of the active element. Furthermore, the limited slew-rate of operational amplifiers affect the large-signal for high-frequency operation. When wide bandwidth, low-power consumption and low-voltage operation are needed simultaneously, the voltage-mode operational amplifier becomes very complex. These disadvantages can be eliminated by using recently introduced high-performance ABBs. By following the most recent trends and progress in this research field, this habilitation thesis is organized as described below.

The first part is focused on first-order all-pass filter (APF) design working in voltage-, current-, mixed-, or dual-mode and fulfill one or simultaneously more from the requirements listed in Section "Accompanying Commentary on the Achieved Results"[1]–[22]. Most of the discussed APFs are single-ended (S-E) topologies [1]–[20]. However, nowadays the fully-differential (F-D) filters are more suited for industrial instrumentation requirements, i.e. in areas such as audio electronics, data transmission, instrumentation, etc. mainly because of their high common mode rejection ratio (CMRR) for rejecting external interference [21], [22]. Hence, F-D APFs are also partially discussed within this section.

The next section discuses typical application area of APFs, i.e. sinusoidal oscillators, which can be designed by cascading the APF to a lossy integrator in a closed loop. Quadrature oscillators are important circuits for various communication applications, wherein there is a requirement of multiple sinusoids that are 90° phase shifted. Hence, the thesis also focuses on oscillator design with specific features and/or using special types of function blocks [2], [3], [23]–[25].

The third part deals with second-order analog frequency filters, where the main stress is on minimal configuration multifunction or universal filter structures design, i.e such topologies that provide at least low-, band-, high-pass or in addition band-stop, and all-pass filter responses, respectively, without changing the circuit topology [26]–[31]. Due to their good frequency selectivity special attention is given to higher-order topologies [32].

Finally, in the last section passive component emulator circuits are discussed. Within this section several grounded voltage controlled positive resistor (GVCPR), lossy/lossless floating/grounded inductance simulators, or novel floating frequency dependent negative resistor (FDNR), and floating capacitance multipliers are designed in active form [33]–[38].

The presented thesis for habilitation consists in total of 38 papers having been elaborated by the author in close collaboration with his highly recognized colleagues since 2011. Here it is worth to mention that 18 papers are published in reputed SCI-E journals with impact factor and ideas were presented in 20 international conference contributions, respectively. To easy finding referred papers the blue-colored backgrounds are used as front pages including the reference number and full citation.

ACKNOWLEDGMENTS

I would like to express my sincerest thanks to *Prof. Ing. Kamil Vrba, CSc.*, former Head of the Department of Telecommunications, Brno University of Technology, for being my mentor since my master thesis and for providing me with the opportunities that I needed for both professional and personal growing. My heartfelt appreciation goes to *Doc. Ing. Jaroslav Koton, Ph.D.*, *Ing. Jan Jeřábek, Ph.D.*, *Ing. Roman Šotner, Ph.D.*, and other colleagues from the university for close collaboration and fruitful discussions made during last years. Special thanks go to *Prof. Dr. Oğuzhan Çiçekoğlu* and *Prof. Dr. Shahram Minaei*, who have been my mentors during my postdoctoral internships at the Beta VLSI Design Laboratory, Boğaziçi University, Turkey and Dept. of Electronics and Communications Engineering, Doğuş University, Turkey, respectively, for their support, valuable guidance, and fruitful discussions from which many of the original ideas have been published and received considerable attention in the literature. My thanks also go to other highly recognized colleagues worldwide *Dr. Abhirup Lahiri* (STMicroelectronics, India), *Assoc. Prof. Bilgin Metin* (Boğaziçi University, Turkey), *Assoc. Prof. Erkan Yuce* (Pamukkale University, Turkey), *Assist. Prof. Umut E. Ayten* (Yıldız Technical University, Turkey), *Assoc. Prof. Mehmet Sağbaş* (Yeni Yüzyıl University, Turkey), *Prof. Dr.* İ*zzet Cem Göknar* (Doğuş University, Turkey), *Prof. Dr. Jiun − Wei Horng* (Chung Yuan Christian University, Taiwan), and others for collaboration, useful discussions, and sharing already published original ideas. Finally and most importantly, this thesis could not have been possible without tolerance, understanding, and support of my family and my loved once.

My thanks are also intended to Czech Science Foundation (GACR) postdoctoral fund no. P102/11/P489, project CZ.1.07/2.3.00/30.0039 of Brno University of Technology, and other grants for financial support that helped to present results of the work at valuable international conferences.

Norbert Herencsár
Brno, April 24$^{\text{th}}$, 2015

ACCOMPANYING COMMENTARY ON THE ACHIEVED RESULTS

Frequency filters are circuits that shape the spectrum of the input signal in order to obtain an output signal with the desired frequency content. Hence, they have wide area of application in instrumentation, automatic control, communication systems, video signal processing, and broadcasting systems. For phase equalization and for a frequency dependent delay design, while the amplitude of the output signal over the desired frequency range is kept constant, all-pass filters (APFs) are generally used. Hence, APFs are basic building blocks that are widely used in analog signal processing. Therefore, considering first-order APFs, during last years the progress in this research area is significant and the biggest challenge was and still is to propose such circuits that fulfill one or simultaneously more from the following requirements: 1. consist of only one active building block (ABB), 2. employ single grounded capacitor, 3. no passive resistors are required i.e. resistorless circuit, 4. provide electronic control of pole frequency (f_{p}) and/or filter pass-band gain (G_0), 5. suitable for low-voltage and low-power operation at higher-frequency region (tens of MHz), and/or 6. partially/fully cascadable.

Using minimal number of ABBs in the filtering topologies it is expected that the total chip area would be smaller in case of on-chip fabrication. It is well-known that the terminal parasitic capacitances of ABBs in series with floating capacitors in the structure may cause additional unwanted pole and degrade the high-frequency behavior of filters. Therefore, the use of grounded capacitor is welcomed and very important from the monolithic integration point of view. The control of f_{p} and/or filter G_0 is also important feature that makes the proposed circuits attractive in many applications. In practice, the adjustment of these parameters can be done by (i) means of transconductance parameter g_{m}, (ii) varying the intrinsic resistance of low-impedance current input of ABBs, (iii) by using n-channel metal-oxide-semiconductor field-effect transistor (NMOS) working in triode operation as voltage controlled resistor (VCR), or (iv) by changing the current and/or voltage gain of ABB. All four possibilities of tuning can be found in copies of published papers enclosed to this thesis.

Recently, there is also an increasing trend on the design of low-voltage circuits with low-power consumption due to the requirement of efficient portable electronic systems with long battery lifetime. From the filters' cascadability point of view, from circuit theory it is well-known fact that the input and output impedances of circuits should be ideally equal to the extreme values (zero $\{0\}$ or infinity $\{\infty\}$ impedances for short), depending on the type of input and output operational

modes. For current-mode (CM) circuits the input and output impedance should be 0 and ∞ while for voltage-mode (VM) circuits ∞ and 0, respectively. Note that due to this property there is no need for additional current followers or voltage buffers for cascading and it decreases the number of active elements in the final solution.

By following the above listed requirements and the most recent trends, the following discussion can be made on achieved results from this research area. With the aim to minimize the silicon area on the chip, in [1] a novel 'voltage differencing' element, namely the voltage differencing inverting buffered amplifier (VDIBA) was introduced. The proposed novel resistorless first-order VM APF using single VDIBA and capacitor provides both inverting and non-inverting all-pass responses simultaneously at two different output nodes and electronic tuning of f_{p} in approx. one frequency decade. It is worth to mention that the achieved results presented in [1] received the Best Paper Award of the 7th International Conference on Electrical and Electronics Engineering (ELECO 2011) in Bursa, Turkey. Later on, upon a request of ELECO 2011 Conference Chair the application possibilities of VDIBA have been further investigated in details [2]. Note that the proposed first-order VM APF using 'voltage differencing' device introduced in [1] employs floating capacitor. Therefore, in order to eliminate this disadvantage, the attention was focused on design of such versatile 'voltage differencing' type ABB concept that allows grounded capacitor usage while keeping simplicity and maximal functionality of applications. The proposed voltage differencing differential difference amplifier (VDDDA) fulfills these requirements [3]. The pole frequency of the VM filter can be easily controlled by means of internal transconductance. In addition, it provides both high-input and low-output impedances, which is important from cascadability point of view, i.e. theoretically fulfills ∞ and 0 impedances at input/output terminals, respectively.

The electronic tuning property f_{p} of APFs was also investigated in realizations employing second-generation current-controlled current conveyors (CCCIIs) [4], variable-gain third-generation current conveyor (GVCCIII) [5], or electronically tunable differential difference current conveyor (E-DDCC) [6]. The proposed circuit in [4] employs two minus-type CCCIIs, has high input impedance for cascadability, and uses a grounded capacitor. The pole frequency tuning is provided by varying the intrinsic input resistance of low-impedance input terminal X of the used ABBs. In 2006, the function block GVCCIII was presented as a new circuit element with voltage gain controllability between Y and X terminals. In the former contribution authors have focused their attention on the design of grounded inductors. During the literature survey it was found that additional applications of this element do not exist. Therefore, a novel solution of APF operating in current-mode was proposed in [5]. The voltage-gain between Y to X terminal can be controlled

by means of two resistors' ratio. The novel first-order CM APF employs single GVCCIII, two external resistors, and single grounded capacitor. In [6], the E-DDCC was design by adopting the controlled current gain principle of the electronically controllable second-generation current conveyor (ECCII) to the differential difference current conveyor (DDCC). In the paper a new CMOS (complementary metal-oxide semiconductor) internal implementation was proposed, which current gain can be tuned with an external current. The advantage features of E-DDCC have been demonstrated on VM APF whose pole frequency is easily tunable.

Simultaneously, the research was also focused on design of cascadable VM APF design employing grounded capacitor and various types of ABBs, namely fully differential current conveyor (FDCCII) [7], differential current conveyor (DCCII) [8], or universal voltage conveyor (UVC) [9]. In the first step, a generalized full admittance network (GFAN) was defined using each ABB. For design of novel circuits employing single ABBs, the computer added design method was used. In [7], the cascadability feature of the proposed APF was demonstrated on electronically tunable high-Q band-pass (BP) filter application, which is frequently used in the intermediate frequency stages of the receiver circuits. In addition, the proposed BPF was made electronically tunable via electronic resistors. The proposed VM APF in [8] increases the application possibilities of the DCCII in the literature. The DCCII is a current-mode active element with current differencing capability, which combines the simplicity of the classical second-generation current conveyor (CCII) with current differencing feature of the current differencing buffered amplifier (CDBA). Therefore, the DCCII behaves as a CDBA for current differencing operation, but it has an additional voltage terminal adopted from CCII, which has high-input impedance and can be useful for cascading VM circuits. The proposed APF includes a single DCCII, a grounded capacitor, and two resistors. Here it is worth to mention that, similarly to several circuits in the literature, the proposed circuit includes a grounded capacitor in series to X terminal, which may affect high frequency behavior of the filter and it requires a simple resistor matching condition. However, both resistors are in series to X terminals, which is advantage, because unwanted effects of the parasitic resistances at X terminals can be compensated by choosing sufficiently high resistor values. In addition, the research was also focused on study of fully cascadable APF design employing UVC [9]. The presented APF circuit features the use of single active element and provides a high impedance input, low output impedance outputs, and a grounded capacitor. Note that the UVC is not only theoretical function block, but for experimental verification purposes it was also designed and developed using the CMOS 0.35 μm technology under the designation UVC-N1C 0520 and produced in cooperation with ON Semiconductor

Czech Republic, Ltd.

In order to reduce the number of transistor count in the applications and subsequently decrease its chip area and power consumption and increase the proposed circuit attractivity for future on-chip integration, special attention was paid to low-transistor count circuit realizations. For this purpose the two n-channel MOSFET-based unity-gain inverting voltage buffer (IVB) and the four MOSFETs-based current follower (CF) with gain four were used. New current-mode [10], voltage-mode [11], [12], [13] AFPs were proposed with single IVB or single CF, respectively. The proposed filter circuit in [10] simultaneously provides both inverting and non-inverting first-order low-pass (LP), high-pass (HP), and APF responses. Major advantages of the presented circuit are low voltage, low noise and high linearity. In order to suppress the effect of non-zero output resistance of the IVB, two compensation techniques, i.e. by changing the gain of the IVB and via resistor matching ratios, were also introduced in [12].

In parallel with low-transistor count APF design based on two n-channel MOS transistor-based IVB, a new linear circuit design technique was introduced. In [13], the number of external resistors in the proposed VM APF was reduced by considering the input intrinsic resistance of the CF as a useful active parameter. In comparison to the CCII-based CF implementations employing large number of MOSFETs, here the used CF is composed of only four MOSFETs, which significantly reduces the chip area. In [14], the first time in the literature, a special type of APF called MOS-only was presented. In this method, instead of passive external capacitors, the parasitic gate-to-source capacitance ($C_{\rm gs}$) of MOS transistors was with advantage used. Moreover, in [15] the main emphasis was on the optimization of the proposed circuits in terms of their use in high frequency range above 200 MHz. The initial design was based on general structure of the two transistors and two admittances. By choosing passive components and considering real behavior of MOSFETs, i.e. parasitic capacitances and output resistances, thanks to systematic design six specific cases for VM APF design were discussed.

Although the above mentioned circuits operate in voltage- or current-mode, in many applications these circuits must be interconnected, which causes some difficulties, which can be overcame by utilization of voltage-to-current ($V-I$) or current-to-voltage ($I-V$) converter interface circuits. During $V-I$ or $I-V$ interfacing it is also possible to perform signal processing at the same time, so that the total efficiency of the electronic circuitry can be increased. Hence, transadmittance-mode (TAM) and transimpedance-mode (TIM) APFs are important circuits that are used in base-band receiver blocks of radio systems. For instance, the mixed-mode APF design possibilities were investigated using recently introduced

ABB such as current backward transconductance amplifier (CBTA) [16] or simple low-voltage CMOS structures of transconductor, IVB, and unity-gain CF [17], [18]. In order to increase the total efficiency of mixed-mode APF topologies, dual-mode structures can be considered. The proposed APF based on single differential-input buffered and transconductance amplifier (DBTA) [19] as an active element, single capacitor, and single resistor works in both voltage- and transadmittance-mode. In addition, due to high-impedance voltage input and low/high output-impedance of voltage/current outputs, it is fully cascadable. Additional dual-mode APF was introduced in [20]. In the paper the voltage gain-controlled modified current feedback amplifier (VGC-MCFOA) was introduced as new ABB with electronic tuning property, where compared to the conventional MCFOA, its voltage transfer from the Y to X terminal can be easily electronically tuned by means of the voltage gain h. As an application example using the presented new ABB a novel APF employing single VGC-MCFOA and four grounded passive elements is proposed. Reported filter structure provides both current- and transimpedance-mode transfer functions at the same configuration simultaneously and its f_{p} can be easily tuned by means of bias currents that adjust the voltage gain of the active element.

All the above discussed APFs are single-ended (S-E) topologies. Nowadays however, the fully-differential (F-D) filters are more suited for industrial instrumentation requirements, i.e. in areas such as audio electronics, data transmission, instrumentation, etc. mainly because of their high common mode rejection ratio (CMRR) for rejecting external interference. The F-D filters directly process the information embedded into a differential signal to achieve a high signal-to-noise ratio and there is also an increasing availability of sensors with differential output and of analog-to-digital converters with differential input. In addition, F-D filters also have higher dynamic ranges than their S-E counterparts. In general, as it is discussed in [22], the conventional F-D circuits are designed by mirroring S-E filter topology about the ground. Therefore, the used ABB may be featured with F-D inputs/outputs. By adopting this technique the paper [22] presents a new realization of F-D first-order CM APF based on a single adjustable current amplifier (ACA), two CFs with gain 2, and one capacitor. The intrinsic resistance tuning of CFs and current gain A of ACA respectively offer both f_{p} tuning and G_0 tunability of the filter, which are the main advantages of the proposed filter topology compared to the literature available ones. On the other hand, for sake of simplicity F-D filter topologies can be also achieved by advantageous usage of the 'differential difference' property of DDCCs. To be specific, the input part of the proposed F-D VM APF in [21] has differential voltage input character of conventional F-D topologies, however, the output responses are taken in two differential voltage nodes

in structure. Thanks to this technique two F-D structures have been proposed with minimal configuration wherein the capacitor is grounded.

Typical application area of all-pass filters is the design of sinusoidal oscillators, which can be implemented by cascading the APF to a lossy integrator in a closed loop [2], [3]. In general, quadrature oscillators are important circuits for various communication applications, wherein there is a requirement of multiple sinusoids that are 90° phase shifted, e.g. in quadrature mixers and single-sideband modulators, or for measurement purposes in the vector generator or selective voltmeters. Therefore, the research was also focused on oscillator design with specific features and/or using special types of function blocks. For example, in [23] it was proved that for compact VM four-phase oscillator design single z-copy voltage differencing transconductance amplifier (ZC-VDTA), two capacitors, and three resistors, all in grounded form, are sufficient. Similarly, a very compact active CMOS-RC realization of sinusoidal oscillator capable of generating four quadrature voltage outputs was proposed in [24]. The oscillator has been designed by cascading of lossless and lossy integrators in loop. The governing laws for the condition of oscillation (CO) and the frequency of oscillation (FO) are single-resistance-controlled (SRC), which allow independent FO tuning. Unlike previously reported SRC-based sinusoidal oscillators based on ABB-based approach, this direct CMOS realization provides a much reduced transistor count circuit and consequently offers a low power solution. In addition, the usefulness of the CBTA was investigated in [25] on CM & VM multiphase sinusoidal oscillator (MSO) structures. The proposed oscillators can generate n current or voltage signals (n being even or odd) equally spaced in phase. For nth-state oscillator design $n + 1$ CBTAs, n grounded capacitors, and single grounded resistor are required. The oscillation frequency can be independently controlled through transconductance of the CBTAs, which are adjustable via their bias currents. The performance of the proposed circuits has been demonstrated on third-stage and fifth-stage MSOs.

Probably, the most discussed and most popular analog filters in the literature are the second-order filters that are also called as biquads. One of the advantage of these circuits is that a general filter of a higher-order can be designed by cascading a number of second-order ones. Based on circuit topologies and complexity the biquads can be divided into several categories. Nowadays the highest attention is paid to such second-order filter structures that can provide at least the basic three standard filter functions, i.e. low-, band-, high-pass or additionally also band-stop and all-pass filter responses without changing the circuit topology. These filtering structures are called multifunction or universal filters, respectively. Similarly, considering the number of inputs and outputs in topologies then biquads can be categorized to so-called

multi-input single-output (MISO) or single-input multi-output (SIMO). First of all, to increase the versatility of the above mentioned VDIBA, in [26] a new VM MISO universal filter was presented. The proposed filter contains only single VDIBA, two capacitors, and one n-channel MOS transistor. Note that the NMOS operates in triode region and it is used for resonance angular frequency f_0 tuning. The filter can be classified as resistorless since in the structure no resistors are needed. Compared with other ABB-based counterparts the VM MISO filter is very simple, it contains only few transistors, and has the smallest size area. Moreover, no component matching is required and it shows low sensitivity performance. Likewise, from simplicity point of view as CM counterpart of the VM MISO in [26] the universal MISO proposed in [27] can be considered. The proposed CM biquad architecture employs single DDCC, two grounded capacitors, two resistors and by appropriate setting of input terminals as open circuit it realizes all five standard filter functions. Although both MISO biquads are of minimal configuration, additional current followers or voltage buffers are required for their cascading. This disadvantage is overcame in [28], however, for the cost of biquad complexity. The designed circuit uses three plus-type differential voltage current conveyors (DVCCs), two grounded capacitors, and two resistors and offers features such as realization of all the standard filter functions, no requirements for component matching conditions, the use of only grounded capacitors, high-input and low-output impedances, and low active and passive sensitivities. Particularly, the SIMO type biquads are more attractive, because they are able to realize several responses simultaneously with the same topology and without changing its configuration. This kind of filter, which finds wide applications in phase-locked loop FM stereo demodulation, touch-tone telephone tone decoding etc., is advantages in consideration of versatility, simplicity, and cost reduction. Advantages of 'voltage differencing' feature of the voltage differencing current conveyor (VDCC) have been demostrated in [29]. The new electronically tunable SIMO using only one VDCC, two grounded capacitors, and two resistors offers the following advantages: the usage of minimum number of electronic active and passive elements, realization of four filter responses simultaneously, electronical adjustability of Q without changing the values of the passive components, low active and passive sensitivities, no need of extra inverting-type input signals for realizing filter function, and finally no component matching conditions. In addition, the two improved SIMOs in [30] simultaneously realize all five standard filter functions and Q and f_0 can be controlled orthogonally, i.e. f_0 can be adjusted arbitrarily and at the same time Q can be set to any value through passive resistor without disturbing f_0. Unfortunately, the complexity of circuit topologies has increased.

One of the best known biquad structure is the Kerwin–Huelsman–Newcomb

(KHN) that enables mutually independent control of the Q and f_0. Recently however, special tunable (reconfigurable) biquad design technique has been introduced, namely frequency-agile filters (FAFs) that have the property of agility, i.e. in order to not disturb the signal processing during the transmission of the signal, the hop between two consecutive frequencies f_1 and f_2 must be able to be carried out very quickly. In general, its implementation is based on such classical second-order frequency filter structure, which provides at least BP and LP responses. Therefore, by following the most recent trend in the literature, new first class 1 CM FAF using ECCIIs, two resistors, and two grounded capacitors has been proposed [31]. The behavior of the initial classical tunable filter and proposed second-order CM FAF has been studied in detail and performance of the new FAF tested by both regular and post-layout simulations. As a conclusion, compared to basic second-order BPF, the centre frequency of the new FAF can be set over more than one decade higher. On the other hand, filters with good frequency selectivity have to be of the order higher than two. During the last decades it was shown that LC ladder structures have minimum sensitivity to component variations in the frequency band of interest. Thus, the performance of these types of passive filter structures is very reliable and stable. Elliptic or so-called Cauer filters represent a specific type of LC ladder filters having the transmission zeros as well as poles at finite frequencies that create equal-ripple variations in both the pass-band and the stop-band and feature faster transition from the pass-band to the stop-band than any other class of network synthesis filters. However, on-chip spiral inductors occupy large chip area and therefore are costly and suffer from substrate resistive losses and capacitive couplings. Moreover, their value in passive form is not easily tunable. Due to these disadvantages, after introducing active filters, it has become a common practice to reproduce the operation of ladder passive filters by means of active filter counterparts to maintain the same low-sensitivity characteristics. In work [32], therefore, two active only grounded-C equivalents of third-order VM elliptic LP LC ladder prototype are proposed. The first active only grounded-C LP filter employing eight CFTAs was proposed by interconnecting CFTA-based active equivalent sub-blocks of passive components, where one of the low-impedance input terminals is not used. Since such feature may cause some noise injection into the proposed circuit, the proposed filter was optimized using Mason-Coates' signal flow graph approach. In several steps the number of ABBs was reduced by two and the unused input terminal was eliminated. Real behavior of the optimized active only grounded-C third-order VM elliptic LP filter is very satisfactory and experimental results using the readily available UCC-N1B 0520 ICs confirm the theoretical study.

The last part of the thesis deals with emulation of passive components in active

form such as grounded voltage controlled positive resistor (GVCPR), lossy/lossless floating/grounded inductance simulators using various ABBs, or novel floating frequency dependent negative resistor (FDNR), and floating capacitance multipliers design. Electronically tunable resistors are widely used in analog signal processing such as in active RC filters with variable f_0, controlled oscillators, variable gain amplifiers, voltage or current dividers, and voltage or current to frequency converters, etc. In [33], the proposed new CMOS-based GVCPR with one control voltage employs only five CMOS transistors. Note that in the structure one of transistors operates in triode region while others in saturation region or OFF. One of the main properties of the novel GVCPR is its ultra low power consumption. However, a single active component matching condition is needed, which can be considered as cost for simplicity. In addition, the superior performance of the designed GVCPR was proved by numeric Figure of Merit calculation. An inductor is also a required element in circuit design. Conventional spiral inductors directly made on chip occupy significant chip area and therefore are too costly and suffer from substrate resistive losses and capacitive couplings. In addition, process tolerances lead to component variations, which cannot easily be tuned in the passive case. Therefore, in recent years, synthetic inductor realizations have been focused on the field of the integrated circuit (IC) design due to the resulting reduction in size and cost effectiveness. In [34], two novel grounded inductance simulator circuits are composed of single first generation current conveyor (CCI), single capacitor, and four or two resistors, respectively. Note that the second inductance simulator employs additional unity-gain voltage follower. In the work a new, differential pair based, low-voltage, high performance and wideband CMOS CCI is also proposed, which shows features such as has high voltage swings (close to supply voltages) between input and output terminals, wideband current and voltage transfer ratios, and due to super source follower configuration very low equivalent impedance of terminal X. The application possibilities of the above discussed DCCII have been increased by designing six novel lossless grounded inductance simulator circuits [35]. Proposed circuits simultaneously employ minimum number of elements, i.e. single DCCII, one capacitor, and two resistors. No passive element matching restriction is needed and all solutions are electronically tunable in case that one of resistors is replaced by MOSFET-based VCR. It is worth noting that each proposed circuit employs floating capacitor, however they can be realized easily with a current IC process that offers double poly (poly1-poly2) or metal-insulator-metal (MIM) capacitor. The performance of the selected inductor simulator was tested in 5th-order high-pass LC passive ladder prototype, in LCR parallel resonant circuit, and in high-pass filter prototype. In order to reduce the disadvantages caused by the

usage of floating capacitor, in [36] new topologies realizing one lossless grounded inductor and two floating, one lossless and one lossy, inductors employing a single DDCC and a minimum number of passive components, i.e. two resistors, and one grounded capacitor are discussed. The floating inductors are based on conventional dual-output DDCC (DO-DDCC) while the grounded lossless inductor is based on a modified dual-output DDCC (MDO-DDCC). Note that MDO-DDCC element has the same terminal voltage-current relations than DO-DDCC except current transfer gain between terminals X and Z+, which is 1/2. From design point of view the proposed lossless floating inductor is obtained from the lossy one by employing a negative impedance converter (NIC). To demonstrate the performance of the proposed grounded inductance simulator, it is used to construct a parallel resonant circuit. With the aim to reduce the used ABBs in previously published CFTA-based floating lossless inductance simulators available in the literature, the work [37] has reported an alternate realization using two z-copy CFTAs and two passive elements. Finally, in [38] a general floating immittance function simulator realizing frequency dependent negative resistor (FDNR), inductor, capacitance multiplier, and resistor was proposed. It is composed of two CBTAs and three passive components that are all grounded. The circuit does not require any component matching conditions and it has good sensitivity performance with respect to tracking errors. Moreover, the proposed FDNR, inductance, capacitor and resistor simulator can be tuned electronically by changing the biasing current of the CBTA or can be controlled through the grounded resistor or capacitor. The high-order frequency dependent element simulator circuit is also presented. Depending on the passive component selection, it realizes high-order floating circuit defining as $V(s) = s^n AI(s)$ or $V(s) = s^{-n} BI(s)$. The performance of the proposed floating FDNR simulator circuit and floating high-order frequency dependent element simulator circuit has been verified.

The theoretical results presented in [1]–[38] were verified by SPICE simulations using CMOS process technology parameters such as TSMC 0.35 μm, TSMC 0.25 μm, TSMC 0.18 μm, IBM 0.13 μm, PTM 90 nm, etc. In some cases, the behavior of the proposed applications was experimentally verified using the readily available UVC-N1C 0520 & UCC-N1B 0520 ICs developed at our department and produced in cooperation with ON Semiconductor Czech Republic, Ltd., via commercially produced chips AD844, OPA660, OPA860, AD830, LT1364, or array transistors CD4007UB. These excellent results were mainly obtained within the Czech Science Foundation (GACR) postdoctoral fund no. P102/11/P489. For the research, infrastructure of the SIX Research Center was used. Moreover, part of the results was used for education purposes and published in textbooks [39] and [40].

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