A Novel Cyclic Time-to-Digital Converter Based on Triple-Slope Interpolation and Time Amplification

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Abstract. *This paper investigates a novel cyclic time-to-digital converter (TDC) which employs triple-slope analog interpolation and time amplification techniques for digitizing the time interval between the rising edges of two input signals (Start and Stop). The proposed converter will be a 9-bit cyclic time-to-digital converter that does not use delay lines in its structure. Therefore, it has a low sensitivity to temperature, power supply and process (PVT) variations. The other advantages of the proposed converter are low circuit complexity, and high accuracy compared with the time-to-digital converters that have previously been proposed. This converter also improves the time resolution and the dynamic range. In the same resolution, linear range and dynamic range, the proposed cyclic TDC reduces the number of circuit elements compared with the converters that have a similar circuit structure. Thus, the converter reduces the chip area, the power consumption and the figure of merit (FoM). In this converter, the integral nonlinearity (INL) and differential nonlinearity (DNL) errors are reduced. In order to evaluate the idea, the proposed time-to-digital converter is designed in TSMC 45 nm CMOS technology and simulated. Comparison of the theoretical and simulation results confirms the benefits of the proposed TDC.*

Keywords

Time-to-digital converter (TDC), cyclic TDC, analog interpolation, pulse multiplier (PM)

1. Introduction

High resolution time-to-digital converter (TDC) has been widely used in many applications such as on-chip time signal measurement systems, biochemical sensor readouts and frequency synthesis circuits [1], All Digital Phase Locked Loops (ADPLLs) [2], [3], laser range finders [4], digital storage oscilloscopes, and capacitive sensor readouts [5]. In these converters, the time interval between two input signals is converted into a digital output code. TDCs can be divided into two main groups: direct conversion and indirect conversion TDCs [6]. Direct conversion TDCs employ delay-line elements which include a chain of buffers or inverters in their structure. These converters are used to measure short time intervals between the rising edges of the input signals [7], [8]. The main disadvantages of direct conversion TDCs are the circuit complexity, which results in high power consumption and high sensitivity to PVT variations [9]. In addition, these converters are sensitive to the mismatch between the elements causing the non-linear factors. In general, the dynamic range of the converters is limited by the number of delay stages. Therefore, the conversion rate is slow [10]. Indirect conversion TDCs can be divided into the ramp TDCs [11], and the multi-slope pulse stretching TDCs [12], [13]. There are also converters that take advantage of the interpolation technique for conversion which is implemented based on multi-slope pulse stretching methods [9], [14], [15]. The interpolation circuits are usually united with the counter-based TDCs to increase the input range to infinity [9]. Indirect conversion TDCs feature low sensitivity to PVT variation, sub-gate resolution, simple circuit structure, low chip area, and good dynamic range. In order to achieve high performance, a high-resolution, high-speed TDC is required. A perfect solution is the employment of a two-step TDC which amplifies the time residue after the coarse conversion and subsequently performs a fine conversion [16]. This paper investigates a novel cyclic TDC that employs analog interpolation and time amplification techniques for digitizing the time interval between the rising edges of two input signals as well as increasing the resolution. The advantages of the proposed 9-bit cyclic TDC are the followings. 1) This converter has a low circuit complexity compared with TDCs previously proposed. 2) The proposed converter does not use delay lines and vernier delay lines (VDL) in its structure, resulting in taking advantage of low sensitivity to PVT variation in the design. 3) It features high resolution and accuracy due to employing two-step and analog interpolation structures. 4) The proposed cyclic TDC reduces the number of circuit elements compared with the previously proposed converters. Therefore: 5) This converter reduces the active chip area and the power consumption. 6) In the proposed converter, there is no apparent mismatch between the circuit elements. Thus, the linear range of the converter is appropriate without extra elements. 7) This converter has a good dynamic range and reduces INL and DNL errors. In the proposed converter, analog interpolation is performed based on

a triple-slope conversion. Simulation results prove that our TDC achieves a resolution of 0.273 ps by 470 μW energy consumption through a 1.8 V power supply. The INL and DNL errors are in the range of +1.1/–0.8 LSB and +1.15/–1.1 LSB, respectively. Also, the dynamic range of the converter is 360 ps.

The basic principles of the time domain 2.5b/stage cyclic structure are described in the following section, while the implementation of the proposed cyclic TDC using the interpolation and time amplification techniques is presented in Sec. 3. Next, Section 4 gives a description of the operation details of the proposed cyclic TDC, and the simulation results are presented in Sec. 5. Section 6 concludes this work.

2. Time Domain Cyclic Structure

Figure 1 shows the block diagram of a cyclic TDC which includes an input pulse generator, a time domain 2.5b TDC and a register and digital error correction logic. At the beginning of the conversion, the pulse generator receives two time input signals (Start and Stop) and generates a pulse whose width is the time interval between the rising edges of the two. The generated pulse is the first time input of the converter and is fed to the cyclic TDC. The detailed circuit implementation and transfer curve of a 2.5b/stage TDC are shown in Fig. 2 and Fig. 3, respectively [13]. The structure of the time domain 2.5b/stage is similar to a conventional 2.5b multiple digital-to-analog converter (MDAC) which is a main block in voltage domain pipeline and cyclic converters [17], [18]. The time domain 2.5b/stage consists of a TDC, a digital-to-time converter (DTC) and a time amplifier (TA) [19]. According to Fig. 2, the TDC can quantize the time input and produce a 2.5b digital output code. Next, according to the output digital code, the DTC produces a time reference which is necessary to generate the time residue. Finally, the time residue is amplified by the TA and fed to the next operation phase. The transfer curve is inverted due to complementary operation of the time-register [13]. Therefore, the following equation is obtained for time output:

$$T_{out} = \begin{cases} 4(4\tau_Q - T_{in}) & 0 \le T_{in} < 3\tau_Q & 000 \\ 4(6\tau_Q - T_{in}) & 3\tau_Q \le T_{in} < 5\tau_Q & 001 \\ 4(8\tau_Q - T_{in}) & 5\tau_Q \le T_{in} < 7\tau_Q & 010 \\ 4(10\tau_Q - T_{in}) & 7\tau_Q \le T_{in} < 9\tau_Q & 100 \\ 4(12\tau_Q - T_{in}) & 9\tau_Q \le T_{in} < 11\tau_Q & 101 \\ 4(14\tau_Q - T_{in}) & 11\tau_Q \le T_{in} < 16\tau_Q & 110 \end{cases} \quad (1)$$

where τ_Q is a quantization level [13]. According to (1), the relationship between T_{in} and T_{out} can be expressed as follows:

$$T_{out} = 4(T_{FS} - T_{in}) = 4T_{res} \quad (2)$$

where T_{res} and T_{FS} are the time residue and the full scale time, respectively [13].

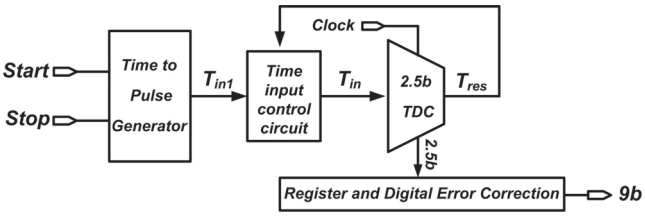


Fig. 1. Block diagram of a cyclic TDC.

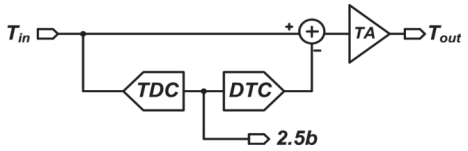


Fig. 2. Block diagram of a time domain 2.5b/stage.

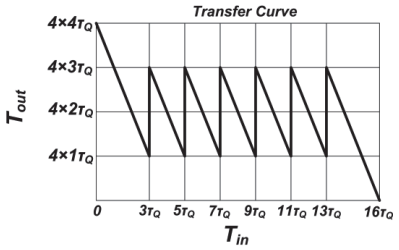


Fig. 3. Transfer curve of a time domain 2.5b/stage.

3. Proposed Cyclic TDC

In this section, the performance of the proposed 9-bit cyclic TDC in different modes of operation is investigated. The block diagram of the 2.5b/stage converter is shown in Fig. 4, along with the corresponding timing diagram depicted in Fig. 5. The proposed TDC consists of a 3-bit digital counter, two comparators, a pulse multiplier, an interpolation capacitor, a constant current source, and some simple control logics. The following subsections describe the converter operation in its different modes. Firstly, the pulse generator produces a pulse whose width is the time interval between the rising edges of two input signals (T_{in}).

3.1 Step 1: Charging the Input Capacitor

In the rising edge of the *Start* signal (or the rising edge of T_{in}), switch S_1 is turned on while switches S_2, S_3, and S_4 are turned off. Hence, the input capacitor (C_{in}) is charged by a constant current source (I_{ref}) linearly. The equivalent circuit for this operating step is illustrated in Fig. 6. Thus further charging of C_{in} is stopped in the rising edge of the *Stop* signal (or the falling edge of T_{in}). At the end of this step, the voltage on C_{in} (V_C) is proportional to T_{in} and obtained as follows:

$$V_{in} = \frac{I_{ref} . T_{in}}{C_{in}} \quad (3)$$

where V_{in} is the voltage on C_{in} at the end of step 1.

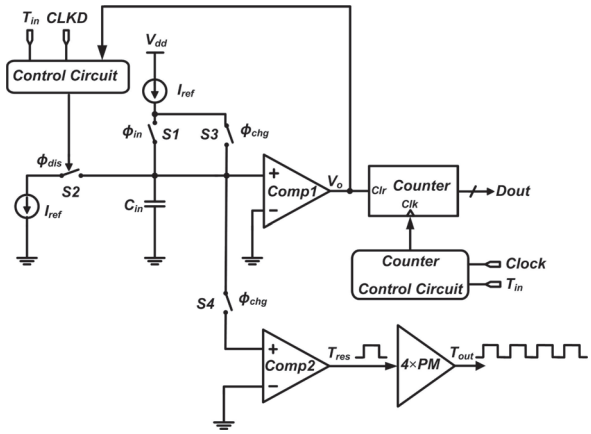


Fig. 4. Block diagram of the proposed 2.5b/stage cyclic TDC.

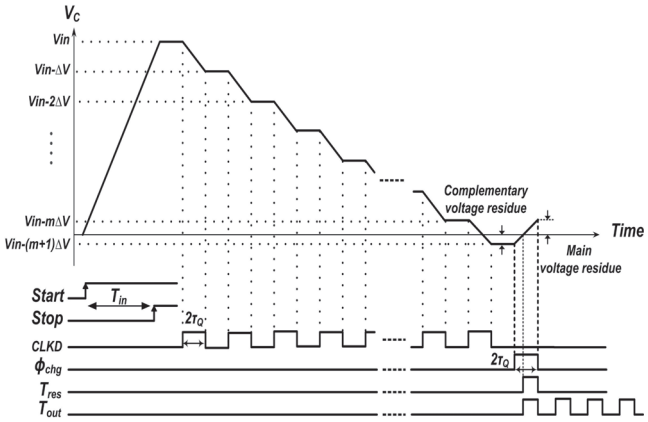


Fig. 5. Timing diagram of the proposed 2.5b/stage cyclic TDC.

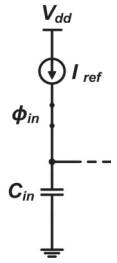


Fig. 6. The equivalent circuit for charging step.

3.2 Step 2: Discharging Input Capacitor and Generating Complementary Voltage Residue

This step is similar to an analog interpolation TDC presented in [10]. In Step 2, an analog interpolator circuit is used for digitizing the time interval between two input signals and producing a digital output code. The proposed TDC performs a triple-slope time stretching for quantizing the time interval and increases the resolution. According to the equivalent circuit of Step 2 shown in Fig. 7, switches S_1, S_3, and S_4 are turned off while S_2 is turned on. As a result, C_{in} is discharged by a constant current source (I_{ref}), alternatively. Analog interpolation is performed by a second reference clock (CLKD) [10]. To quantize an input

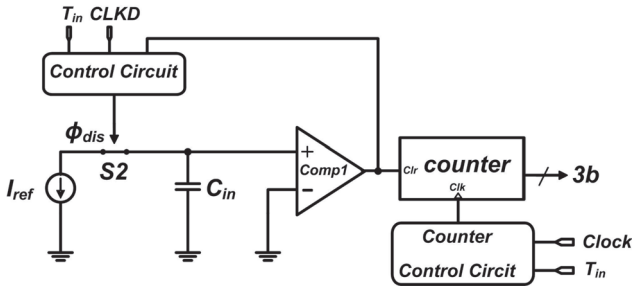


Fig. 7. The equivalent circuit for discharging input capacitor and generating complementary voltage residue step.

pulse, C_{in} is discharged periodically during CLKD and a digital counter counts the number of discharging steps (quantization levels). The voltage drop across C_{in} in each period of CLKD is calculated as:

$$\Delta V = \frac{I_{ref}.(2\tau_Q)}{C_{in}} \tag{4}$$

where ΔV and $2\tau_Q$ are the voltage drop across C_{in} and the pulse width of CLKD in each period, respectively. The full-scale time (T_{FS}) of the proposed cyclic TDC is defined by the total time delay for discharging C_{in}. Therefore, in each step of the operation of the cyclic TDC, T_{FS} is depended to the input signal and calculated as:

$$T_{FS} = 2(m+1)\tau_Q \tag{5}$$

where

$$m = \left[\frac{T_{in}}{2\tau_Q}\right]. \tag{6}$$

At the end of this step, the voltage on C_{in} is calculated as:

$$\begin{aligned} V_{res} &= V_{in} - (m+1)\Delta V = \frac{I_{ref}\cdot T_{in}}{C_{in}} - (m+1)\frac{I_{ref}\cdot 2\tau_Q}{C_{in}} \\ &= \frac{I_{ref}}{C_{in}}\left(T_{in} - 2(m+1)\tau_Q\right) \end{aligned} \tag{7}$$

where V_{res} is voltage residue of the input capacitor and m is the number of CLKD cycles required for discharging C_{in}. At the end of Step 2, according to the proposed TDC operation and (7), V_{res} has a negative voltage value which is proportional to the complimentary time residue. Comparator 1 compares the voltage on C_{in} with '0' and switches its output accordingly. Thus, when the output of comparator 1 begins '0', the digital counter is stopped. A digital register saves the produced 3-bit output in each step. Finally, the digital error correction logic gathers four saved 2.5 bits and produces the final 9-bit output.

3.3 Step 3: Charging Interpolation Capacitor and Generating Main Voltage and Main Time Residue

The equivalent circuit for this operating step is illustrated in Fig. 8. During this step, the main voltage residue

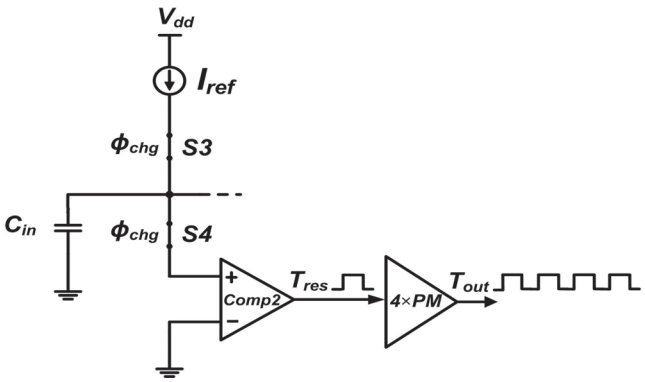


Fig. 8. The equivalent circuit for charging interpolation capacitor and generating main voltage and main time residue step.

and the main time residue are generated from the complementary voltage residue. According to the equivalent circuit of Step 3 shown in Fig. 8, C_{in} is charged by a constant current source (I_{ref}) in a period of CLKD ($2\tau_Q$). At the end of Step 2, voltage on C_{in} was negative, which was equal to the complementary voltage residue. However, at the end of Step 3, the voltage of C_{in} is positive, which is equal to the main voltage residue. Thus:

$$V_{mvr} - V_{res} = \frac{I_{ref}.(2\tau_Q)}{C_{in}} \tag{8}$$

where V_{mvr} is the main voltage residue, thus:

$$V_{mvr} = \frac{I_{ref}}{C_{in}}.[T_{in} - (2m\tau_Q)]\,. \tag{9}$$

Simultaneously, the main time residue is generated by comparator 2. The output of comparator 2 is '1' as long as the voltage of C_{in} is greater than '0'. As can be seen in Fig. 5, in the falling edge of Φ_{chg}, S_4 is turned off and the output of comparator 2 begins '0'. Thus, comparator 2 produces a pulse whose width is the main time residue. The main time residue is calculated as:

$$T_{res} = \frac{C_{in} \cdot V_{mvr}}{I_{ref}} = T_{in} - (2m\tau_Q)\cdot \tag{10}$$

3.4 Step 4: Generating 4×Pulse Multiplier

In this step, the main time residue is amplified by a 4×pulse multiplier (PM) which is the time input for the next cyclic step. As can be seen in Fig. 9, the pulse multiplier includes an OR gate and four delayed signals [13], [19]. 4×PM achieves accurate gain and wide input linear range without calibration. Thus:

$$T_{out} = 4 \cdot T_{res} = 4 \cdot [T_{in} - (2m\tau_Q)]\,. \tag{11}$$

The digital register saves four digital output codes that are produced by the digital counter in four cyclic steps. Finally, the digital error correction logic produces the final 9-bit output.

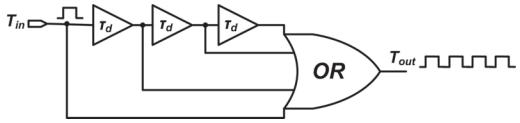


Fig. 9. 4×pulse multiplier.

4. Operation Details of the Proposed Cyclic TDC

An example of a detailed operation of the proposed cyclic TDC is investigated in this section. Consider an input signal of $T_{in} = 9.8\ \tau_Q$ ($0 \le T_{in} \le 16\ \tau_Q$) which is the time interval between the rising edges of two input signals (Start and Stop). Therefore, the digital 9-bit output code for this time input is '100111001'. The operation details of the proposed converter are as follows.

Step 1: Suppose the time interval between the rising edges of the two input signals is $T_{in1} = 9.8\ \tau_Q$. Therefore, $m_1 = [(9.8\ \tau_Q)/(2\ \tau_Q)] = 4$ and the output of the digital counter is '100'. As a result, $T_{FS1} = 10\ \tau_Q$, and the interpolation capacitor is discharged in 5 cycles of CLKD. The voltage of the C_{in} is proportional to $0.2\tau_Q$ (V_{res1}) which is a negative voltage value and is a complementary voltage residue. Thus, the interpolation capacitor is charged for $2\tau_Q$ which produces the main voltage residue. Thus, the main time residue is $T_{res1} = 2\ \tau_Q - 0.2\ \tau_Q = 1.8\ \tau_Q$, and the voltage of C_{in} is proportional to $1.8\ \tau_Q$ (V_{mvr1}). The time residue is amplified by a 4×PM ($4 \cdot 1.8\ \tau_Q = 7.2\ \tau_Q$) and fed to the second step.

Step 2: In the same way, $T_{in2} = 7.2\ \tau_Q$ and $m_2 = [(7.2\ \tau_Q)/(2\ \tau_Q)] = 3$. Thus, the digital output code for the second step is '011'. According to (9), $T_{FS2} = 8\ \tau_Q$ and C_{in} is discharged in 4 cycles of CLKD. Therefore, complementary voltage residue is proportional to $8\tau_Q$ (V_{res2}). Therefore, the interpolation capacitor is charged for $2\tau_Q$ and the main voltage residue is produced (V_{mvr2}). The time residue ($T_{res2} = 1.2\ \tau_Q$) is amplified by a 4×PM ($4 \cdot 1.2\ \tau_Q = 4.8\ \tau_Q$) and fed to the third step. Similar to the two previous steps, step 3 and step 4 are described as the following:

Step 3: $T_{in3} = 4.8\ \tau_Q$, $m_3 = [(4.8\ \tau_Q)/(2\ \tau_Q)] = 2$ and the digital output code for the third stage is '010'. Also, $T_{FS3} = 6\ \tau_Q$, (V_{res3}) and the main voltage residue is (V_{mvr3}). The time residue is $T_{res3} = 0.8\ \tau_Q$ and 4×PM output is ($4 \cdot 0.8\ \tau_Q = 3.2\ \tau_Q$) which is fed to the last stage.

Step 4: $T_{in4} = 3.2\ \tau_Q$, $m_4 = [(3.2\ \tau_Q)/(2\ \tau_Q)] = 1$, and the digital output code for the third stage is '001'. Also, $T_{FS4} = 4\ \tau_Q$, (V_{res4}) and the main voltage residue is (V_{mvr4})**.** The time residue is $T_{res4} = 1.2\ \tau_Q$ and 4×PM output is ($4 \cdot 1.2\ \tau_Q = 4.8\ \tau_Q$).

In each step, the digital output code is saved by a register. Finally, the four generated digital output codes are combined in the digital error correction logic which produces the final 9-bit output. This operation is calculated as:

1	0	0						
		0	1	1				
				0	1	0		
+						0	0	1
1	0	0	1	1	1	0	0	1

Fig. 10. Operation of the digital error correction logic.

As shown in Fig. 10, the generated output digital code obtained from the digital error correction logic in the proposed converter is a correct digital output code.

5. Simulation Results

In this section, the simulation results of the proposed 9-bit cyclic TDC are investigated. The simulation is performed in TSMC 45 nm CMOS technology. Figure 11 shows the layout prototype of the cyclic converter, where the active area is 825 μm^2. In this section, a case ($T_{in} = 9.8\tau_Q$) for simulation results of the converter is presented. Simulation is implemented by the following elements: an input capacitor ($C_{in} = 15$ pF), and a constant current source ($I_{ref} = 40$ mA). To evaluate the proposed TDC operation, $\tau_Q = 35$ ps is used which is equal with a buffer delay in this technology. The digital output codes of the four steps in the cyclic TDC are '100', '011', '010' and '001', respectively gathered in the digital error correction logic and producing a final 9-bit digital output code ('100111001'). In this case, $T_{in} = 9.8\tau_Q = 343$ ps. Thus, the voltage of C_{in} in step 1 is 915 mV. Figure 12 shows the voltage waveforms of C_{in} for the four steps of the proposed cyclic TDC. As shown in Fig. 12, the voltages of C_{in} in steps 2, 3, and 4 are 672 mV, 448 mV and 300 mV, respectively. Also, Figure 13 shows the voltage waveform of C_{in} in the four steps of the proposed 9-bit cyclic TDC. In the analog interpolator circuit, C_{in} is discharged periodically by I_{ref} in $2\tau_Q$ periods. The complementary voltage residue of step 1 is –18.7 mV. Moreover, the complementary voltage residues of steps 2, 3, and 4 are –75.7 mV, –112 mV and –74.6 mV, respectively and are proved by (4-9). Therefore, the main voltage residue of step 1 is 167.2 mV. Also, the main voltages residue of steps 2 and 3 are 111.9 mV and 74.6 mV, respectively. For each step, the output of comparator 2 are amplified by a 4×PM and fed to the next step. Figure 14 shows the output waveforms of the PMs. For this case, the post-layout simulation of the proposed cyclic TDC is shown in Fig. 15. Also, a Monte-Carlo simulation which shows the effect of transistor mismatch is shown in Fig. 16. Comparison of the theoretical and simulation results confirms our TDC operation. The proposed cyclic TDC achieves time resolution of 0.273 ps at a conversion rate of 300 MS/s. A ramp input is applied to measuring the time output, the differential nonlinearity (DNL), and the integral nonlinearity (INL) of the proposed converter in the linearity performance of the corresponding region shown in Fig. 17. As shown in this figure, the cumulative digital output code count with 512 samples is used so that the accuracy of the proposed TDC improves. Figures 18 and 19 show DNL and INL of the converter in the linearity performance of the corresponding region, respectively. It can be seen that the measured INL and DNL of the converter are +1.1/–0.8 LSB and +1.15/–1.1 LSB, respectively. The simulated TDC achieves an input dynamic range (DR) of 360 ps and a time resolution of ($2\tau_Q/(4\times4\times4\times4) = 0.273$ ps). Also, the total power consumption of the cyclic TDC is 470 μW which shows improvement in comparison with the previous cyclic TDC [13], [20].

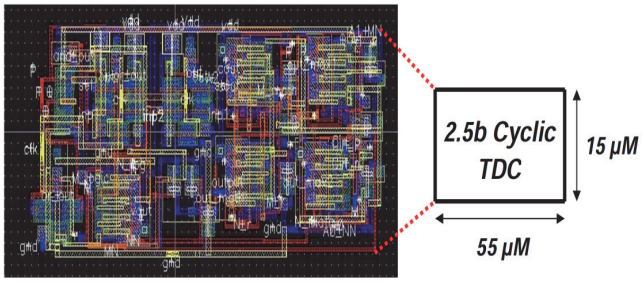
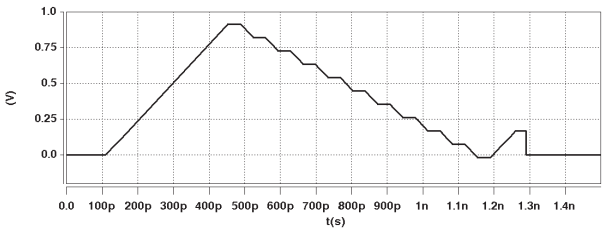
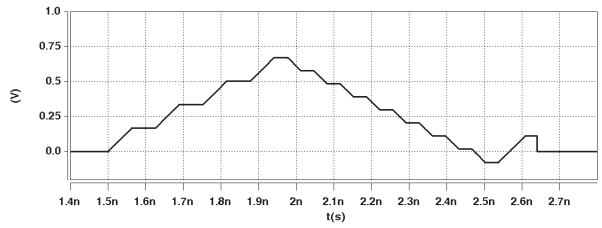


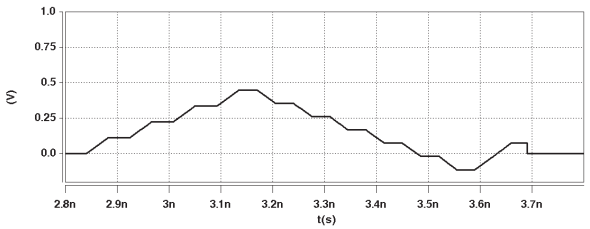
Fig. 11. The layout prototype of the proposed cyclic TDC.



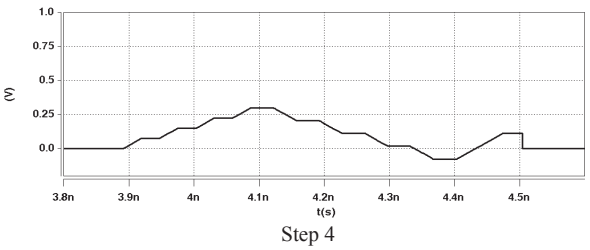
Step 1



Step 2



Step 3



Step 4

Fig. 12. The voltage waveforms of the input capacitor.

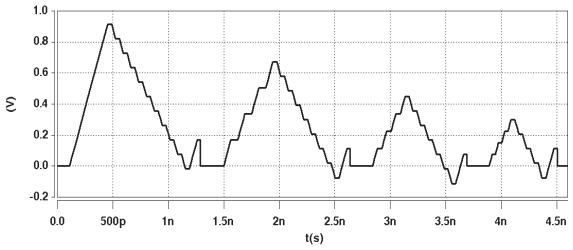
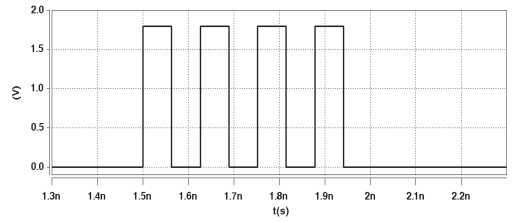
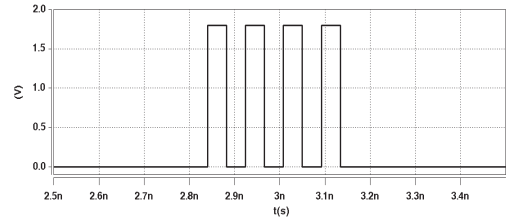


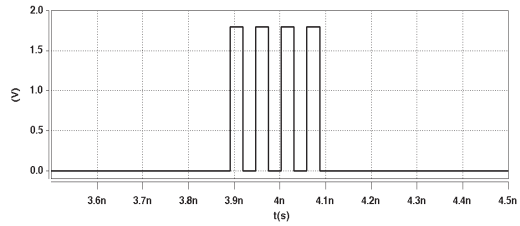
Fig. 13. The voltage waveform of C_{in} in a period of conversion.



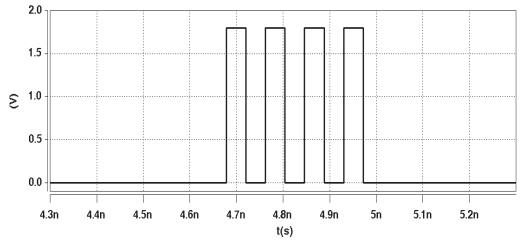
Step 1



Step 2



Step 3



Step 4

Fig. 14. The output waveforms of 4×PM in the proposed cyclic TDC.

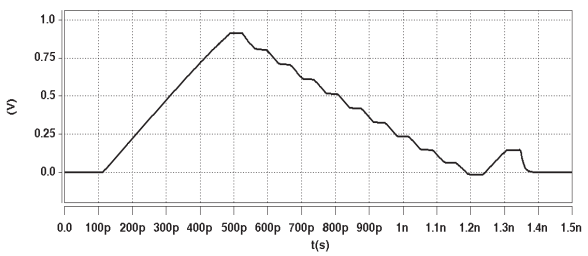


Fig. 15. The post-layout simulation of the proposed cyclic TDC.

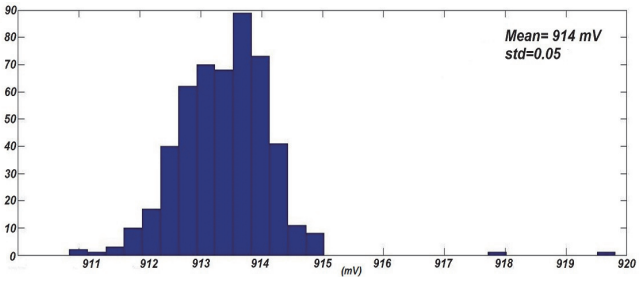


Fig. 16. Monte-Carlo histograms of V_C ($N = 500$ and $\sigma = 0.05$).

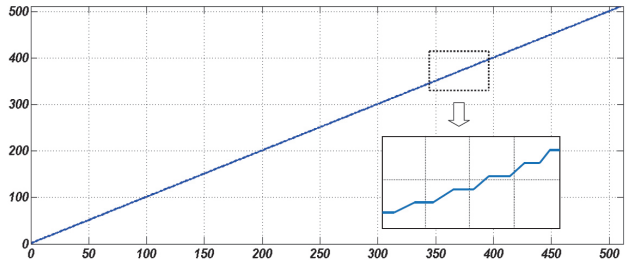


Fig. 17. Output code of the proposed TDC with ramp input.

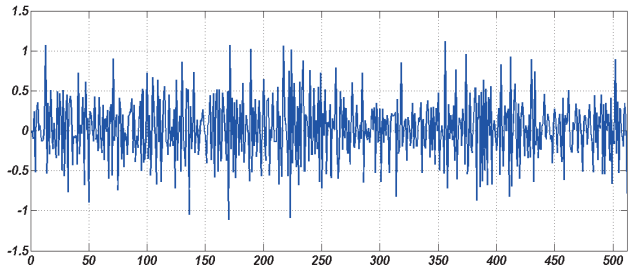


Fig. 18. DNL of the proposed cyclic TDC.

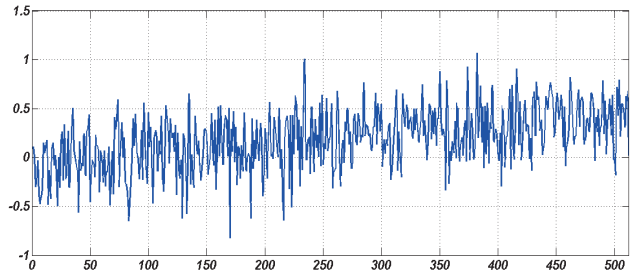


Fig. 19. INL of the proposed cyclic TDC.

	Ref [8]	Ref [9]	Ref [10]	Ref [13]	Ref [19]	This Work
Scheme	Vernier Delay line TDC	Triple Slope Interpolation	Dual Slope Interpolation	Time-Register Pipeline TDC	Two-Step Pipeline TDC	Cyclic TDC based on Interpolation
Resolution	4.8 ps	375 ps	50 ps	1.12 ps	3.75 ps	0.273 ps
Bits	7	10	10	9	7	9
Conversion Rate	50 MS/s	175 MS/s	80 MS/s	250 MS/s	200 MS/s	300 MS/s
Linearity	1 LSB(DNL) 3.3 LSB (INL)	0.68 LSB(DNL) 0.79 LSB (INL)	- LSB(DNL) 1.1 LSB (INL)	0.6 LSB(DNL) 1.7 LSB (INL)	0.9 LSB(DNL) 2.3 LSB (INL)	1.15 LSB(DNL) 1.1 LSB (INL)
Technology	65 nM	0.35 µM	0.35 µM	65 nM	65 nM	45 nM
Power	1.7 mW	1.22 mW	0.75 mW	15.4 mW	3.6 mW	470 µW
Area	0.07 mm^2	0.126 mm^2	0.225 mm^2	0.14 mm^2	0.02 mm^2	825 μm^2
FoM (pJ/conv.step)	1.139	-	-	0.325	0.463	0.0053

Tab. 1. The performance summary and comparison.

The performance of the proposed cyclic TDC is summarized in Tab. 1 with the previously reported high-resolution TDCs. The results confirm the performance of our TDC. Compared with previous works, the proposed cyclic TDC improves circuit complexity, resolution, dynamic range, and chip area.

6. Conclusion

In this study, a novel approach for cyclic TDC is presented which employs interpolation and time amplification techniques for digitizing the time interval between two input signals. The proposed 9-bit cyclic TDC has a simple circuit architecture and does not use delay lines and VDLs in its structure. Therefore, it has a low sensitivity to PVT variations. The proposed TDC uses cyclic, analog interpolation, and two-step structures. Thus, this converter improves time resolution and accuracy. In fact, the analog interpolation is performed based on a triple-slope conversion. Also, the dynamic range of the proposed converter is lower than the TDCs previously proposed. In this converter, the linear range of the converter is increased without extra elements. In addition, the active chip area and the power consumption of the proposed TDC are reduced due to employing a cyclic and triple-slope interpolation structures. Reducing the INL and DNL errors is another advantage of this converter. The theoretical and simulation results confirm the merits of this TDC operation.

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