Review of Doctoral Thesis: “New Methods for Increasing Efficiency and Speed of Functional Verification”

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The submitted doctoral thesis deals with methods for functional verification of digital systems. The growth of design complexity is very fast in semiconductor industry as well as the utilization of modern technologies in safety critical applications. From this perspective, the quality of verification belongs to main concerns in the design of integrated circuits.

The thesis consists of eleven chapters. Chapter 1 states the background and motivation. Chapter 2 describes main verification approaches. Chapter 3 exhaustively explains the principles of the functional verification. Introduction to evolutionary computing can be found in chapter 4. State-of-the-art is described in chapter 5. Chapter 6 defines four goals of the thesis. The following four chapters deal with one thesis goal respectively. Chapter 10 provides summary of presented work and point to topics for future research.

Formal comments follow:

- p. 7 – typo error 2x ...of the system...
- Fig. 2.1 – SDF annotated simulation of post-layout netlist is missing in the design flow diagram
- Section 2.2 – static timing analysis is not mentioned. Logic equivalency check is not mentioned here but its description can be found in section 2.3.2.
- Section 4 – tournament and roulette algorithms are introduced without reference
- p. 35 – missing reference [?]
- Abbreviation CTL* and PLTL are not defined.
- Figure 3.11 seems redundant. The figure itself is not sufficient to uncover details of UVM run phases.
- Section 7.4 presents an interesting application of FPGA-based accelerator but it does not correspond with the thesis goals.

Comments and questions to the presented methods:

1. FPGA-based acceleration

The HAVEN framework presents low-cost alternative to existing hardware emulators on the market. Experimental results show its efficiency for certain kind of applications. In my opinion, the main disadvantage is the necessity to implement verification components (drivers, monitors, assertion checkers) in RTL code which restricts implementation of SystemVerilog behavioral features.

Questions for defense:
How are the assertions translated to RTL?
Do you support acceleration of all SVA features?

2. Automated generation of verification environment

The described method is tailored for a single application – the creation of simulation environment from design architecture specification written in CodAL. I agree that presented approach can decrease verification effort rapidly. On the other hand, I am not able to recognize any outcome which can be applied in general. Similar approaches solving specific tasks are often used in the industry (e.g. DSP ALU generated from XML description).

3. Optimization of Coverage-driven verification

I appreciate that author identified disadvantages of randomly generated stimuli. The utilization of genetic algorithm for constraining of random generators is innovative. Experimental results demonstrate improvement in comparison with the common constrain solvers.

Questions for defense:
Compare main features of the proposed method with Questa InFact tool – present key differences.
How much time (simulation runs) does the tuning of GA parameters require?
Experimental results significantly depend on the definition of coverage requirements – present and comment coverage requirements for Codix RISC.

4. Optimization of Regression Suites

Randomly generated stimuli contain many redundant transactions with minimal impact on the growth of functional coverage. Hence, stimuli optimization seems to be necessary technique for effective usage of randomly generated stimuli. Proposed methods can supplement any generator of random stimuli.

Questions for defense:
Optimization ratio reached in experiments is extremely high – can you evaluate root-cause of this phenomenon? (an excellent optimization algorithm or an extreme redundancy in input data)
Would it be possible to integrate optimization into stimuli generator?

Summary

The theme of thesis complies with doctoral degree program. Published methods offer solution to actual problems. I consider the methods described in chapter 9 and 10 as main contribution of the thesis. The utilization of genetic algorithms in functional verification is a novel approach.

Experiments prove good performance of methods in comparison with industry-standard generators. The list of publications proves author's ability to come up with original results. I also admire engineering skills and effort invested in the implementation of the HAVEN simulation/emulation environment described in chapter 7.

I support Ms. Šimková's candidacy for PhD degree. I recommend this thesis for defense.

In Brno, Nov 12th, 2015

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