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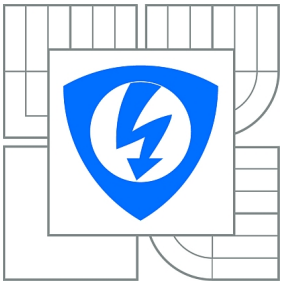

FAKULTA ELEKTROTECHNIKY A KOMUNIKAČNÍCH TECHNOLOGIÍ

ÚSTAV ELEKTROTECHNOLOGIE

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

DEPARTMENT OF ELECTRICAL AND ELECTRONIC TECHNOLOGY

SYSTEM LEVEL ANALYSIS OF THERMAL PROPERTIES OF INTEGRATED CIRCUITS

ANALÝZA TEPELNÝCH VLASTNOSTÍ INTEGROVANÝCH OBVODŮ NA SYSTÉMOVÉ ÚROVNI

BAKALÁŘSKÁ PRÁCE

BACHELOR'S THESIS

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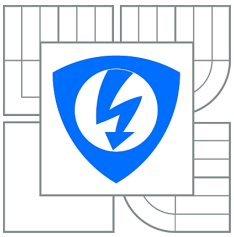

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

Fakulta elektrotechniky a komunikačních technologií

Ústav elektrotechnologie

Bakalářská práce

bakalářský studijní obor
Mikroelektronika a technologie

Student:	Martin Vaněk	***ID:***	146987
Ročník:	3	***Akademický rok:***	2013/2014

NÁZEV TÉMATU:

Analýza tepelných vlastností integrovaných obvodů na systémové úrovni

POKYNY PRO VYPRACOVÁNÍ:

Prostudujte základní principy přenosu tepla a popište tepelné vlastnosti materiálů používaných v elektrotechnice. Seznamte se s metodikou měření tepelných vlastností pouzder součástek a integrovaných obvodů (EIA/JEDEC Standard JESD51).
Navrhněte desky plošných spojů pro měření tepelného odporu pouzder SO14 a SSOP36-EP a sestrojte teplotní komoru splňující požadavky standardu JESD51. Změřte teplotní koeficient vnitřní struktury vybraných integrovaných obvodů, která může být použita pro měření teploty obvodu, a realizujte jednotlivá teplotní měření. Vyhodnoťte získané teplotní parametry daných obvodů a analyzujte preciznost měření z pohledu opakovatelnosti experimentu. Vytvořte dokumentaci popisující použitou metodiku měření a postupy vyhodnocení výsledků.

DOPORUČENÁ LITERATURA:

Podle pokynů vedoucího bakalářské práce.

Termín zadání:	10.2.2014	***Termín odevzdání:***	5.6.2014

Vedoucí práce: Ing. Martin Frk, Ph.D.
Konzultanti bakalářské práce: Ing. Filip Brtáň, ON Design Czech s.r.o.

doc. Ing. Jiří Háze, Ph.D.
Předseda oborové rady

UPOZORNĚNÍ:

Abstract

The major aim of this work is to summarize the basic facts about the heat related topics with focus on applications in electronics and to perform measurements of thermal resistance of integrated circuit packages.

The first part is theoretical and deals with the heat transfer theory, thermal properties of materials and JEDEC methodology for the thermal properties measurements of integrated circuit packages. The second part consists of the natural convection chamber construction, test printed circuit boards design and thermal measurements. In conclusion, methodology for the measurements of junction-to-ambient thermal resistance is summarized together with practical piece of knowledge from the preceding measurements.

This work can serve as the base for further evaluations of integrated circuit thermal parameters and for verification of thermal simulations. It can also help to asses thermal conductivity of printed circuit boards.

Keywords

Conduction, convection, heat, integrated circuit, JEDEC, measurement, printed circuit board, radiation, temperature, thermal

Bibliografická citace díla:

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Prohlášení autora o původnosti díla:

Prohlašuji, že svoji bakalářskou práci na téma „Analýza tepelných vlastností integrovaných obvodů na systémové úrovni“ („System Level Analysis of Thermal Characteristics of Integrated Circuits“) jsem vypracoval samostatně pod vedením vedoucího bakalářské práce a s použitím odborné literatury a dalších informačních zdrojů, které jsou všechny citovány v práci a uvedeny v seznamu literatury na konci práce.

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V Brně dne 3. 6. 2014 .....

Poděkování:

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V Brně dne 3. 6. 2014 .....

CONTENTS

INTRODUCTION

Present electronic trends demand high power devices and high level of integration. This requirements mean concentrating higher power on smaller area. Therefore, it is important to focus not only on the electrical parameters of the developed devices but also on the thermal properties. Poor design can cause safety, reliability and lifetime problems.

It is desirable to have knowledge of the heat transfer processes and the thermal material properties. It is essential to choose appropriate components, materials and to make their proper placement. Especially in the large-scale production, it is crucial to balance the thermal characteristics and the price of the components and materials.

Standards for measurement of the thermal properties of electronic devices are essential. Data acquired by different companies are comparable when following the standards so they can help customers to choose the right product. An example of such a standard is JEDEC standard number 51. It deals with measurement of thermal characteristics of integrated circuit packages.

The aim of this work is to assess the thermal properties of the chosen integrated circuits in conformity with JEDEC standards. Comparison with the datasheet values, repeatability and influence of the printed circuit board are the key areas of this study.

1 HEAT TRANSFER THEORY

Temperature is state of an object that can be measured by the different types of thermometers. It is proportional to internal energy of the object. Increasing internal energy means increasing temperature.

When two objects with different temperature are in contact (e.g. hot iron cube in cold water), their temperature tend to become equal. This phenomenon is caused by heat (thermal energy) flow from iron to water. As is generally known, heat can flow only in direction from a hotter object to a colder one. Spontaneous heat flow in the opposite direction is not possible. Thermometers are based on heat exchange between the thermometer and the measured object.

Heat transfer can be performed in three different ways - thermal conduction, convection and radiation. Each phenomenon is described in the following sections.

1.1 Thermal Conduction

Thermal conduction is a heat transfer process taking place in solids and fluids. This section will focus mostly on heat conduction in solids. Describing this process in fluids is much more complicated because of significant impact of convection.

Thermal energy flows from areas with higher temperature to those with lower temperature. Higher temperature means higher thermal kinetic energy of particles (atoms, molecules, electrons). Particles with higher energy pass a part of its energy on the neighbouring particles. This causes heat spread across the object.

Conduction heat transfer is described by Fourier's law [16]. Its basic form is expressed by the equation 1.1. This equation tells that heat transfer is proportional to the temperature gradient ∇T and coefficient of thermal conductivity k. Minus sign expresses that heat flow is opposite in direction to the temperature gradient.

$$\overrightarrow{q} = -k \cdot \nabla T \tag{1.1}$$

Temperature gradient can be rewritten in a vector form (eqn. 1.2). Using this equation, Fourier's law can be written for x, y and z direction separately (eqn. 1.3). Conditions for heat spread are equal in all directions in homogeneous materials.

$$\nabla T = \overrightarrow{i}\frac{\partial T}{\partial x} + \overrightarrow{j}\frac{\partial T}{\partial y} + \overrightarrow{k}\frac{\partial T}{\partial z} \tag{1.2}$$

$$\overrightarrow{q_x} = -k \cdot \frac{\partial T}{\partial x} \qquad \overrightarrow{q_y} = -k \cdot \frac{\partial T}{\partial y} \qquad \overrightarrow{q_z} = -k \cdot \frac{\partial T}{\partial z} \tag{1.3}$$

Coefficient of thermal conductivity is a material property. It is not constant, but it varies with temperature and pressure (significant mainly for gasses). Higher pressure means that molecules are closer, the mean time between collisions is lower and heat transfer is more intensive. On the other hand, thermal conductivity of solids and liquids

is nearly pressure independent as the majority of these is under standard conditions almost incompressible. Table 1.4 shows thermal conductivity of some materials. As can be seen, thermal conductivity of nylon and diamond vary more then three orders in magnitude.

Tab. 1.4: *Thermal conductivity of materials* [11]

Material	**Thermal Conductivity**	
	$(\mathrm{W} \cdot \mathrm{in}^{-1} \cdot \mathrm{K}^{-1})$	$(\mathrm{W} \cdot \mathrm{m}^{-1} \cdot \mathrm{K}^{-1})$
Air	0,00076	0,00030
Nylon	0,00635	0,00251
Glass	0,02	0,00791
Steel	1,7	0,672
Silicon	2,5	0,988
Aluminium	5,5	2,174
Gold	7,4	2,925
Copper	10,0	3,953
Silver	10,6	4,190
Diamond	16,0	6,324

Calculating heat flow in the real systems is very complex and complicated task. It is usually done by special software for thermal simulations nowadays. For basic calculations of heat flow in solids, equation 1.5 can be used. Q is generated heat (e.g. by an electronic component), k is thermal conductivity, A is a contact area, L is a length of a heat path through the solid (from the place with temperature T_{hot} to the place with temperature T_{cold}) [11].

$$Q = k \cdot \frac{A}{L} \cdot (T_{\mathrm{hot}} - T_{\mathrm{cold}}) \tag{1.5}$$

Example 1:

Let's have a heat source and a heat sink as shown in figure 1.6. The heat source is an ideal source which dissipates all its power through the top surface. Thermal connection between the heat source and the heat sink is considered to be ideal. What will be the temperature difference of the top and bottom surface of the heat sink?

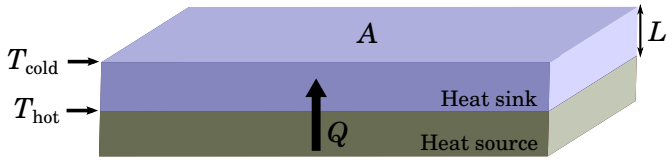


Fig. 1.6: *Heat transfer model of the heat source and the heat sink*

Table 1.8 shows the temperature differences for steel, aluminium and copper. They were calculated using equation 1.7, that is modification of the equation 1.5.

$$\Delta T = T_{\text{hot}} - T_{\text{cold}} = \frac{Q \cdot L}{k \cdot A} \tag{1.7}$$

This calculations are simplified, but they can give us a basic idea of heat transfer in solids. As can be seen in the table, making such a heat sink of copper can lower the temperature difference between the top and the bottom surface more then five times in comparison with steel [11].

Tab. 1.8: *Calculation of the heat conduction*

$Q = 1$ **W** $A = 1$ **cm²** $L = 2$ **mm**			
Heat Sink Material	**Steel**	**Aluminium**	**Copper**
$\boldsymbol{k}$ $(\text{W} \cdot \text{m}^{-1} \cdot \text{K}^{-1})$	0,672	2,174	3,953
$\boldsymbol{T_{\text{hot}} - T_{\text{cold}}}$ (°C)	29,8	9,2	5,1

1.2 Thermal Convection

Thermal convection is a heat transfer process that takes place in fluids (liquids and gasses). Unlike conduction, convection is not associated only with energy transfer but also with mass transfer. Heat convection can be either natural or forced. Natural convection is driven by the density differences associated with the temperature gradients. Higher temperature in most cases means lower density. Forced convection is caused by an external force (wind, fan etc.) [17].

When fluid flows along a solid object, there is friction between them, that causes decrease of velocity of fluid near the solid surface as indicated in figure 1.9. Thin area of thickness δ is called a boundary layer. It was defined as a distance from the surface to a place where the flow velocity reaches 99 % of its maximum [16].

Heat between fluid and solid is exchanged and cooled or heated fluid is moved away by convection. This principle is used for example for cooling of electrical component using fans or cooling by liquid flowing through the pipes. The amount of convective heat transfer is given by Newton's cooling law (eq. 1.10).

$$q = h_c \cdot (T_1 - T_2) \tag{1.10}$$

T_1 is temperature of the surface receiving or giving heat and T_2 is temperature of fluid flowing along the surface. Convective heat transfer coefficient h_c $(\text{W} \cdot \text{m}^{-2} \cdot \text{K}^{-1})$ is also called the convective conductance or the film coefficient [17].

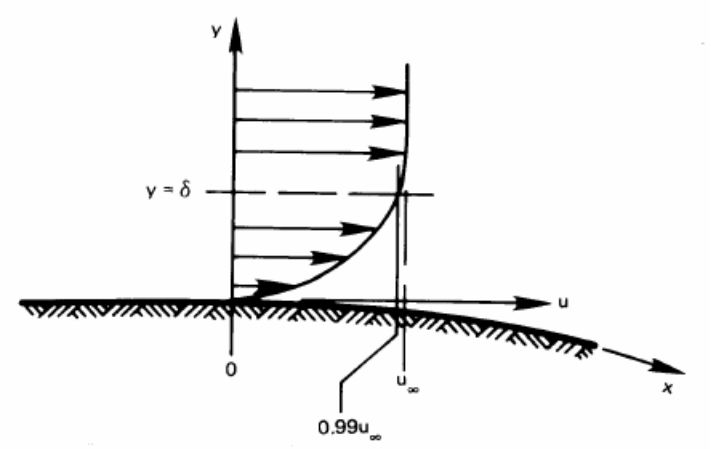


Fig. 1.9: *A boundary layer* [16]

1.3 Thermal Radiation

Each object with temperature above absolute zero (0 K = -273,15 °C) emits some amount of the thermal radiation with a specific wavelength spectrum. Unlike conduction and convection, heat can be transferred also through vacuum by thermal radiation.

Power dissipated from an object by the thermal radiation increases with the fourth power of its absolute temperature T (eq. 1.11). Stefan-Boltzmann constant σ is equal to $5,669 \cdot 10^{-8}$ W $\cdot$ m^{-2} $\cdot$ K^{-4}. Emissivity ε is the material surface property and A is the surface area of the radiating object.

$$P = \sigma \cdot \varepsilon \cdot A \cdot T^4 \tag{1.11}$$

Emissivity value is between 0 and 1. It specifies not only emission but also absorption of the thermal radiation. Ideal emitter (absorber) with emissivity of 1 is called the black body. Real objects has emissivity lower than 1. The black body can be simulated by a cavity with a small hole in it. All incident radiation coming through the hole into the cavity is reflected and absorbed after multiple reflections. Emissivity is not affected only by material but also by the surface texture and varies with wavelength. For example polished copper has emissivity 0,03 and oxidized copper from 0,2 to 0,9 for 1,6 μm wavelength [13].

Thermal (infrared) radiation is an electromagnetic radiation of wavelengths approximately from 0,78 µm up to 1000 µm. Wavelength with the maximal intensity is given by Wien's displacement law (1.12). According to this equation, the highest intensity of thermal radiation of the objects with temperature 20 °C (293 K) is 9,9 µm.

$$\lambda_{\max} = \frac{2,9 \cdot 10^{-3}}{T} \tag{1.12}$$

Example 2:

Let's have a cube with temperature 100 °C = 373 K, emissivity 0,8 and surface area 1 m^2. This cube is placed in a vacuum chamber with temperature 20 °C where heat can be transferred only by radiation. What will be the net radiation in this chamber?

Radiation of the cube:
$P_{\text{cube}} = \sigma \cdot \varepsilon \cdot A \cdot (T_{\text{cube}})^4 = 5,669 \cdot 10^{-8} \cdot 0,8 \cdot 1 \cdot 373^4 =$ **877,9 W**

Net radiation:
$P_{\text{net}} = \sigma \cdot \varepsilon \cdot A \cdot (T_{\text{cube}} - T_{\text{chamber}})^4 = 5,669 \cdot 10^{-8} \cdot 0,8 \cdot 1 \cdot (373 - 293)^4 =$ **1,9 W**

Heat radiated by the cube is more than 870 W. The cube is also absorbing energy radiated from the walls of the chamber so the net radiation is 1,9 W. The net radiation expresses the difference between radiated and absorbed power. This means that the cube emits quite a large amount of energy but nearly the same energy is absorbed at the same time. Thus, the cube is slightly cooling and the chamber is slightly warming. After some time both objects will have the same temperature and the net radiation will be zero [12].

2 THERMAL PROPERTIES OF MATERIALS

2.1 Thermal Conductivity

As mentioned in the first chapter, thermal conductivity expresses how well heat is conducted in the material. High coefficient of thermal conductivity is usually advantageous for the electronic applications. Cooling is better and the temperature gradients are smaller. Thermal conductivity is therefore an important property for the thermal management of the devices.

As apparent from table 2.1, thermal conductivity of the materials used in electronics can vary more than two orders in magnitude. High thermal conductivity of metals is given by the free electrons which take part in the heat transfer process. On the other hand, thermal conductivity of polymers is very low.

Tab. 2.1: *Thermal conductivity (at 20 °C)* [9]

Material	**Thermal Conductivity** ($W \cdot m^{-1} \cdot K^{-1}$)
Alumina substrate (96% Al_2O_3)	22,3 [14]
Rigid FR4 standard PCB	0,25 to 0,5 [15]
Fe	80,5
Cu	386,7
Al	236,1
Au	317,7
Ag	428,8
Sn	65,2
Pb	35,4
63Sn-37Pb (UNS L54915)	57,8
96Sn-4Ag	57,3
Si	152,6
Ge	62,4
GaAs	52,7
HDPE (homopolymer)	0,49 [8]
C-PVC	0,14 [1]

2.2 Specific Heat

Specific Heat is a material property expressing how much thermal energy is needed for 1 K temperature increase or decrease for each kilogram of material. It can be calculated from the heat capacity divided by the atomic weight. There are several factors influencing

the specific heat. The most important one is the lattice vibration. There are also some abnormalities - for example iron(or other ferromagnetic materials) have very high specific heat at Curie temperature. Magnetic moments become randomly oriented at this temperature and ferromagnetic properties of material change to paramagnetic. Another parameter influencing the specific heat is the crystal structure [2].

Table 2.2 shows the specific heat of the chosen materials. The values are valid at 20 °C, unless otherwise stated. Specific heat of aluminium is high in comparison with other listed metals and even FR4 needs less energy to heat up.

Tab. 2.2: *Specific heat (at 20 °C)* [9]

Material	**Specific Heat** ($J \cdot kg^{-1} \cdot K^{-1}$)
FR4	840
Al_2O_3 (alpha)	764
Fe	446
Cu	383
Al	894
Au	129
Ag	235
Sn	228
Pb	129
63Sn-37Pb (UNS L54915)	219
96Sn-4Ag	242
Si	707
Ge	319
GaAs	330
HDPE	2250 (at 23 °C) [8]

2.3 Coefficient of Thermal Expansion

Coefficient of thermal expansion expresses how much the dimensions of an object change with temperature. There are quite significant differences in thermal expansion of material used in electronics. Therefore the designer should be aware of this while choosing components and materials for his devices. Different coefficients of thermal expansion can cause thermo-mechanical stress that can lead to a failure especially in the devices working in a wide temperature range. Thermo-mechanical stress can give rise for example to degradation of the soldered joints.

Temperature distribution is also important, because not only the different coefficients of thermal expansion but also the temperature differences are responsible

for thermo-mechanical stress. Thus, temperature gradients should be kept as small as possible. Some materials are anisotropic. It means that their coefficients of thermal expansion are not same in all directions.

Coefficients of thermal expansion of chosen materials are listed in the table 2.3. Anisotropic structure of FR4 material for the printed circuit boards (PCBs) causes the big difference of the coefficient of thermal expansion in the z direction in comparison with x and y direction.

Tab. 2.3: *Linear coefficient of thermal expansion (at 20 °C)* [9]

Material	**Coefficient of Thermal Expansion** ($ppm \cdot K^{-1}$)
Alumina substrate (96% Al_2O_3)	8 [14]
Rigid FR4 standard PCB (x direction)	17 [15]
Rigid FR4 standard PCB (y direction)	12 [15]
Rigid FR4 standard PCB (z direction)	70 [15]
Fe	11,85
Cu	16,67
Al	23,00
Au	13,88
Ag	19,03
Si	2,56
Ge	5,69
GaAs	5,76
Sn	23,21
Pb	29,15
63Sn-37Pb (UNS L54915)	23,88
96Sn-4Ag	21,50
HDPE	120 [8]
C-PVC	60 [1]

3 JEDEC METHODOLOGY FOR THE THERMAL MEASUREMENT OF COMPONENT PACKAGES

JESD51 Standard (EIA/JEDEC Standard No. 51) describes methodology for the thermal measurement of component packages of single semiconductor devices. This methodology is distributed among several documents which deal with many different areas - thermal measurements (test methods), thermal environments, component mounting and device construction.

Junction temperature and thermal resistance are the key thermal parameters. Junction temperature determines performance and reliability of the device and thermal resistance characterise the heat transfer from the die. Standards for the thermal measurements were made because thermal resistance is not constant and is influenced by many factors. If measurements meet the standards, acquired data of different devices are comparable. Table 3.1 shows the basic JESD51 documents. Some of them are described in the following sections. There are few other documents describing for example measurements with multichip packages or light emitting diodes [7].

3.1 EIA/JEDEC Standard No. 51-1

This document defines a standard electrical test method (ETM) that can be used for measurements of the thermal characteristic of a single integrated circuit. Described method is applicable to a single die devices - either thermal test die or active integrated circuit device. Thermal measurements are affected by many factors (measurement method, environment, selection of junction temperature sensor etc.). Thus, it is important to follow the standards to gain accurate data.

The thermal resistance of a semiconductor device is usually described by equation 3.2. $R_{\theta JX}$ (or θ_{JX}) expresses what will be the temperature difference between the junction and the specific environment for each watt of dissipated thermal energy. T_J is temperature of the junction and T_X is temperature of the specific environment. P_H is power dissipation of the device. Letters "X" in the equation can be substituted by C (case), B (board) or A (ambient) according to the chosen environment.

$$R_{\theta JX} = \frac{T_J - T_X}{P_H} \tag{3.2}$$

$$T_J = T_{J0} + \Delta T_J \tag{3.3}$$

Junction temperature T_J is determined by the initial temperature T_{J0} and the temperature increase ΔT_J after applying the heating power (eq. 3.3). Appropriate structure inside the semiconductor device is used for sensing of the junction temperature. It is usually a semiconductor diode (e.g. protection diode or bulk diode). As the I-V characteristic

Tab. 3.1: *EIA/JESD51 documents*

Standard No.	**Topic**
51	Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)
51-1	Integrated Circuits Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device)
51-2A	Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)
51-3	Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
51-4	Thermal Test Chip Guideline (Wire Bond Type Chip)
51-5	Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms
51-6	Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)
51-7	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
51-8	Integrated Circuit Thermal Test Method Environmental Conditions - Junction-to-Board
51-9	Test Boards for Area Array Surface Mount Package Thermal Measurements
51-10	Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements
51-11	Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements
51-12.01	Guidelines for Reporting and Using Electronic Package Thermal Information
51-13	Glossary of Thermal Measurement Terms and Definitions

of a diode is temperature dependent, forward voltage can be used as temperature-sensitive parameter (TSP).

Temperature difference can be calculated from the temperature-sensitive parameter change (eq. 3.4). As mentioned before, change in TSP can be represented by the change of the voltage drop across the forward biased diode. K is a constant defining relationship between the junction temperature change and TSP change. Measurement current should be chosen large enough to produce a suitable voltage drop across the diode but small enough not to cause self heating that would spoil the measurement.

$$\Delta T_{\mathrm{J}} = K \cdot \Delta TSP \tag{3.4}$$

There are two approaches to the electrical test method - static mode and dynamic mode. Static mode is defined by the simultaneous heating and junction temperature measurement. This mode is suitable for the thermal test dies. Dynamic mode is characterised by switching between heating period and temperature measurement period. Most of the active integrated circuits desire this approach. Both approaches are described in the JEDEC standard [3].

3.2 EIA/JEDEC Standard No. 51-2A

This standard is called Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air). As apparent from the name this document specifies natural convection (still air) environment for the thermal measurements.

It is defined as a closed box with the inside dimensions 305 mm × 305 mm × 305 mm. The box and the support fixture shall be made of materials with thermal conductivity less than 0,5 $W \cdot m \cdot K^{-1}$ (e.g. polycarbonate, polypropylene, wood or plywood). Required minimum enclosure wall thickness is 3 mm. Construction of the enclosure and test fixture is shown in figures 3.6, 3.7 and 3.5.

Test fixture is constructed that the tested device is in the geometrical center of the chamber. The edge connector should ensure horizontal position of the test printed circuit board within ±5°. The test boards are defined by the corresponding JESD51 documents. Ambient temperature thermocouple should be placed according to figures 3.6 and 3.7. Accuracy of the temperature measurement should be less than 1 °C. The ambient room temperature for the test should be between 15 °C and 30 °C. Description of the thermal test environment is followed by the measurement procedure and methodology. Thermal characterization parameters junction-to-top of package and junction-to-board are also described in JESD51-2A [10].

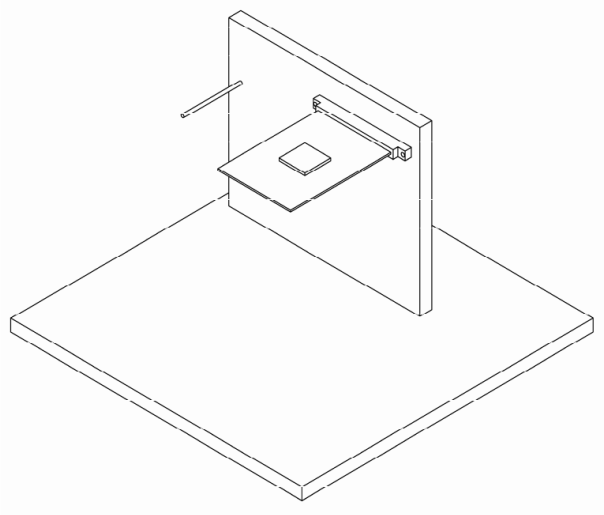


Fig. 3.5: *Isometric view of the test fixture without the enclosure* [10]

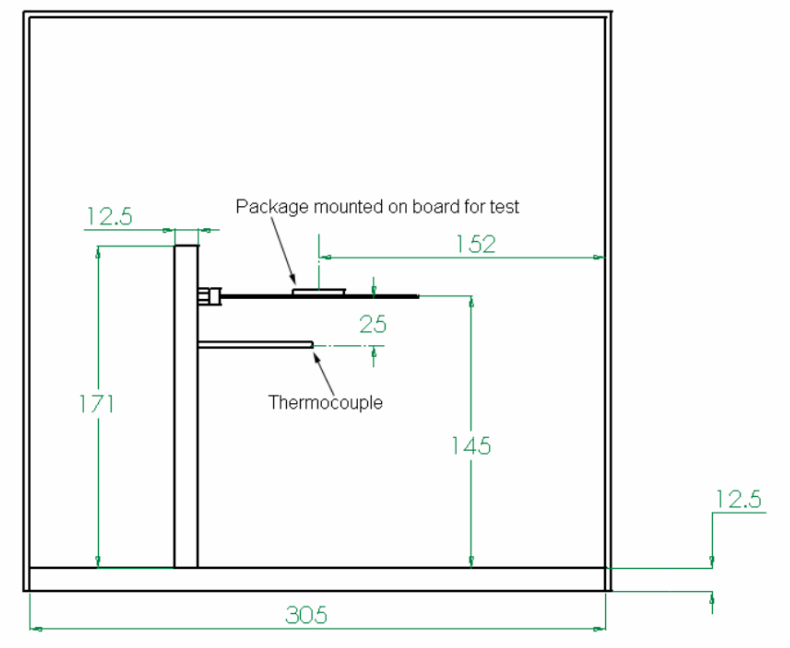


Fig. 3.6: *Side view of the test fixture and enclosure (dimensions in mm)* [10]

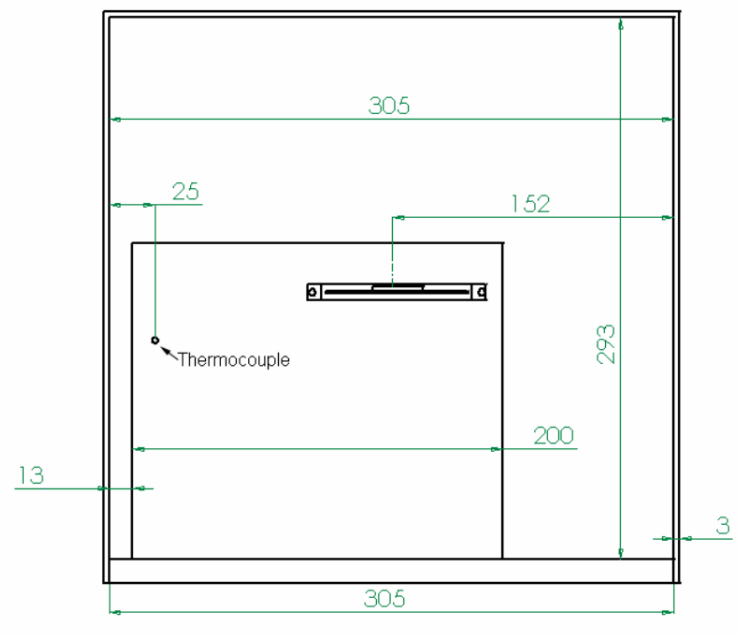


Fig. 3.7: *End view of the test fixture and enclosure (dimensions in mm)* [10]

4 NATURAL CONVECTION CHAMBER CONSTRUCTION

The natural convection chamber (thermal chamber) is constructed according to the JEDSD51 requirements. This means that the inside volume is approximately one cubic feet (dimensions vary less than 10 % from the given values) and the basic construction materials have low thermal conductivity.

The top enclosure is made of extruded polymethyl methacrylate (PMMA) Altuglas EX. Its thermal conductivity is 0,19 $W \cdot m^{-1} \cdot K^{-1}$ and thickness is 5 mm. The support structure for the PCB and the bottom part is made of 12 mm thick plywood. Panel from thin plywood accommodates thirty-six 4 mm banana sockets that are connected with card edge connector through the 36-wire flat cable. There are four rubber feet in the corners of the bottom board to increase thermal isolation. Schematic pictures of the chamber can be seen in figures 4.1 and 4.2. Only dimensions that determine the chamber volume are shown (for other dimensions see section 3.2). Photos of the chamber with and without PMMA enclosure can be seen in figures 4.3, A3 and A4.

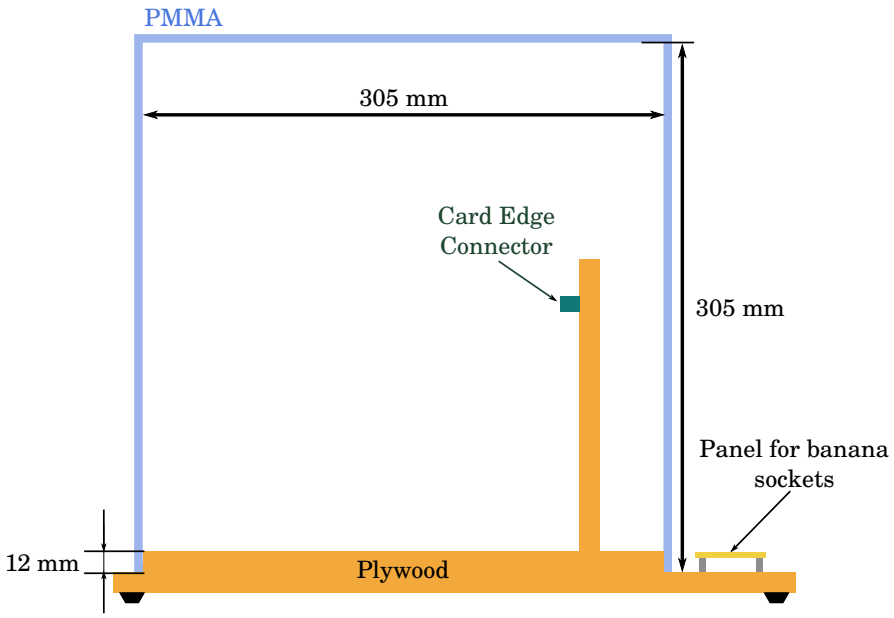


Fig. 4.1: *Natural convection chamber - side view*

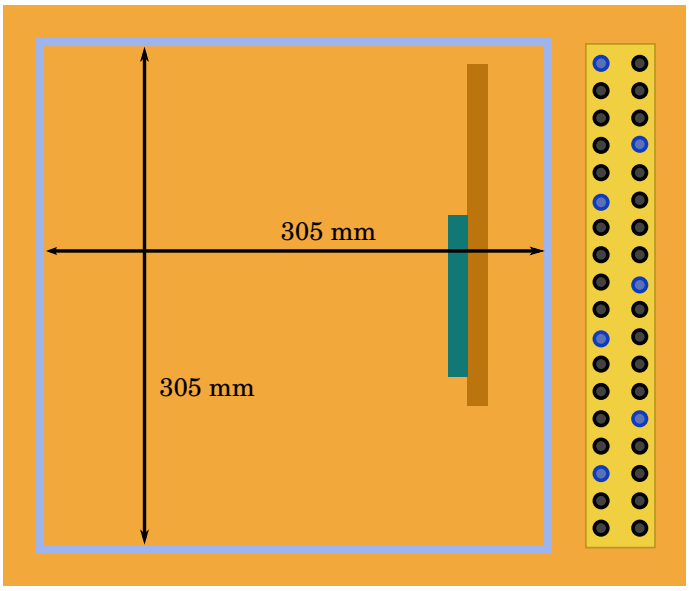


Fig. 4.2: *Natural convection chamber - top view*

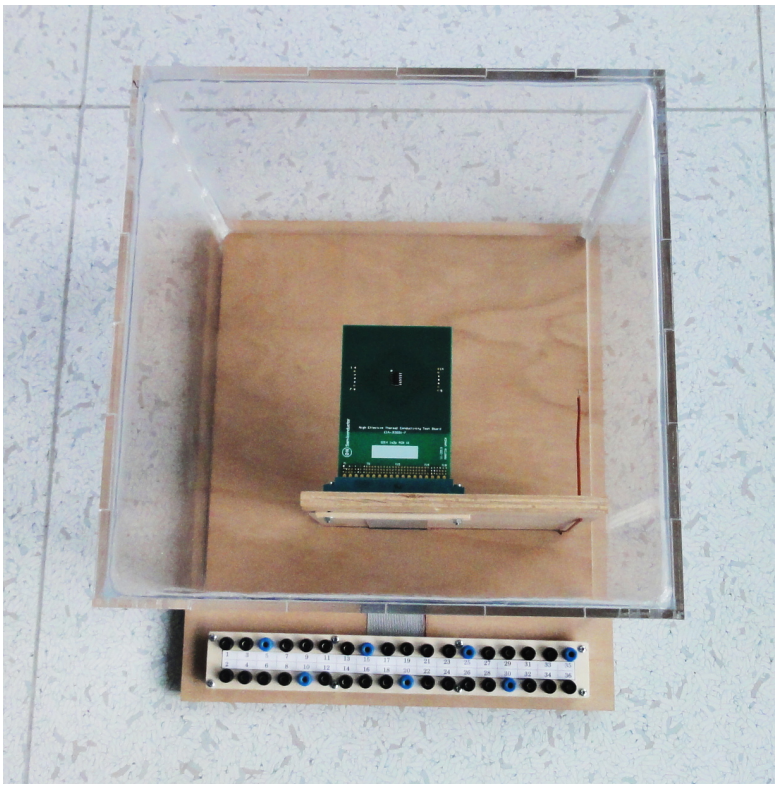


Fig. 4.3: *Natural convection chamber (with enclosure)*

5 DESIGN OF THE PRINTED CIRCUIT BOARDS FOR THE THERMAL MEASUREMENTS

5.1 JESD51 Requirements

The aim of this chapter is to design the printed circuits boards (PCB) for later measurements of the thermal properties of the semiconductor integrated circuit packages SSOP36-EP (SSOP package with the exposed pad) and SO14. Two types of the PCBs for both packages are to be designed - low effective and high effective thermal conductivity test boards for leaded surface mount packages. The design should meet the requirements for the measurements according to the EIA/JESD51 - Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).

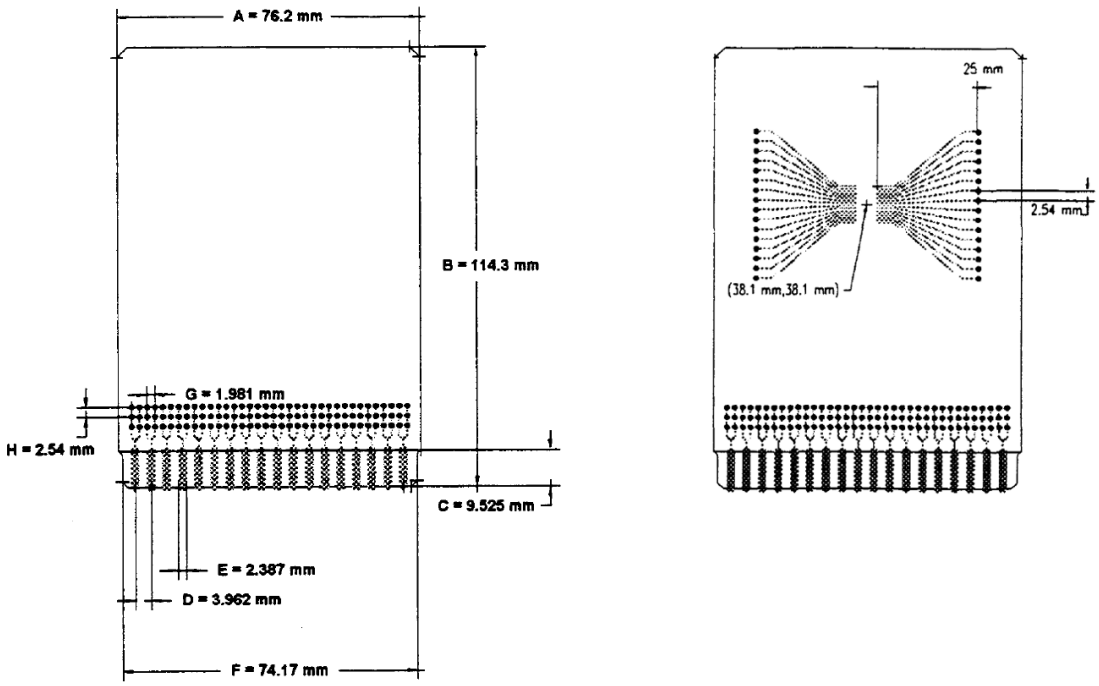
Low effective thermal conductivity test boards for leaded surface mount packages are described in the JEDEC standard number 51-3. This document standardizes the PCB design for the measurements of the Junction-to-Ambient (θ_{JA}) thermal characteristics of the integrated circuit (IC) packages. It is desirable to have such industry standard because the PCB has a dramatic impact on the measurements (more than 60 %). This specification is intended for surface mount components of a lead pitch greater than 0,35 mm and a body size up to 48 mm.

Low effective thermal conductivity test board is a board with one signal layer in fan-out area (no power and ground planes). The PCBs designed according to this standard should perform less than 10% PCB related error in θ_{JA} measurements for a given package geometry. The PCB design rules are listed in table 5.1. If the board is intended for high temperature applications (>125 °C) different material can be substituted for FR4. This change must be reported (especially the thermal conductivity of the material) and measurement correlation between these materials must be established.

Tab. 5.1: *Thermal PCB general design rules*

Description	**Value**
Board Material	FR4
Board Dimensions (package length < 27 mm)	76,2 × 114,3 mm (3.0"× 4.0")
Board Thickness	1.57 mm (0,062")
Minimum Fan-out Trace Length	25 mm (0,98")
Trace Thickness	0,071 mm (0,0028") ± 20 %
Trace with in Fan-out Area(for 0,5 mm pin pitch)	0,254 mm (0,01") ± 10 %
Fan-out Via Spacing	2,54 mm (0,1")
Fan-out Via Land	1,27 mm (0.05")
Fan-out Via Drill Hole	0,83 mm (0,033")
Solder Mask	Optional

Figure 5.2 shows recommended thermal PCB layout for packages with length less than 27 mm. An analysed device is centered in the square area 76,2 mm × 76,2 mm furthest from the edge connector. Fan-out traces must be only on the top layer and must be longer than 25 mm. The edge connector can be modified to meet the company requirements. More via rows along the edge connector are allowed. Traces to the edge connector outside the fan-out can be either on top or bottom layer [6].



(a) *Board dimensions* **(b)** *Fan-out parameters*

Fig. 5.2: *Recommended PCB design* [6]

High effective thermal conductivity test board design for the leaded surface mount packages is described in the JEDEC standard number 51-7. The PCBs meeting the requirements of this standard consists of 2 signal and 2 planes(power and ground) as shown in figure 5.3. PCB related variations in measured θ_{JA} are expected to be less than 10 % with test boards designed according to this standard. Board dimensions are the same as for low effective thermal conductivity test board (JESD 51-3). The drill holes of the vias should not have less then 0,85 mm diameter and 1,25 mm diameter solder land. Isolation clearance between the buried planes and the vias drill holes should be 0,7 mm or less. Beside the clearance areas the buried planes shall be unbroken. The ground and power plane should end 1 mm from the board edge and should not be present in the edge connector area. Power supply of the device can be connected to the ground and power plane through the fan-out vias. In the corners of the buried planes vias are allowed for the power and ground wiring. Other parameters (board material, minimum fan-out trace length, device

position and trace width) are the same as for low effective thermal conductivity test board. All details for the PCB design can be found in the corresponding documents [5].

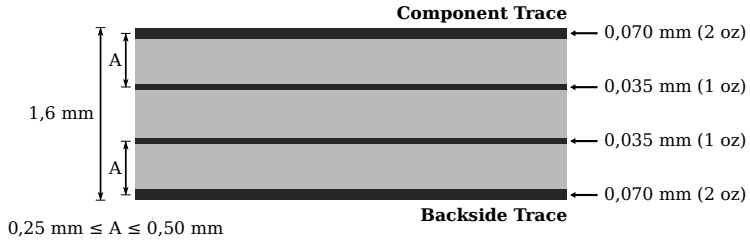


Fig. 5.3: *High effective conductivity test board* [5]

JEDEC standard No. 51-5 is the extension of thermal test board standards which is intended for packages with direct thermal attachment mechanism. The thermal attach pad dimensions must not be more then 1 mm greater than the dimensions of the thermal attachment structure of the integrated circuit. Thermal attach pad smaller than the attachment structure is not allowed. Thermal vias are used only for multi-layer test boards and must provide the thermal contact to the top buried plane. Thermal vias are placed in the grid 1,2 mm × 1,2 mm and for universal or nested test board designs each via is placed in the center of the square with 1 mm side length (Fig. 5.4). Their diameter is 3 mm and minimal Cu plating thickness shall be 0,025 mm. Isolation clearance between the vias and the bottom burried plane should not be less than 0,6 mm and isolation regions should not merge [4].

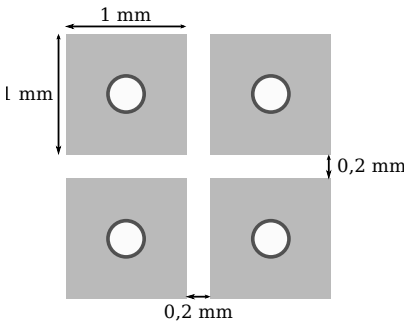


Fig. 5.4: *Thermal vias pattern for universal or nested design* [4]

5.2 Printed Circuit Board Design for SO14 and SSOP36-EP Packages

Figures 5.5 and 5.6 show the top and bottom layer of the low effective thermal conductivity test board for the SO14 integrated circuit packages. Except for the top silk screen, top and bottom layers are same for the low and high effective thermal conductivity test boards. Pictures A5, A6, A7 and A8 show the layers of the high effective thermal conductivity test board, that consists of top, bottom and two inner layers. All layers are shown from the top view.

Top and Bottom layer of the low effective thermal conductivity test board for the SSOP36-EP packages are on the pictures 5.7 and 5.8. The exposed pad of the device under test should be soldered to the thermal attachment area to ensure a good thermal connection. Following figures (A9, A10, A11 and A12) show the layers of the high effective thermal conductivity test board. Some test boards are slightly modified according to the company requirements.

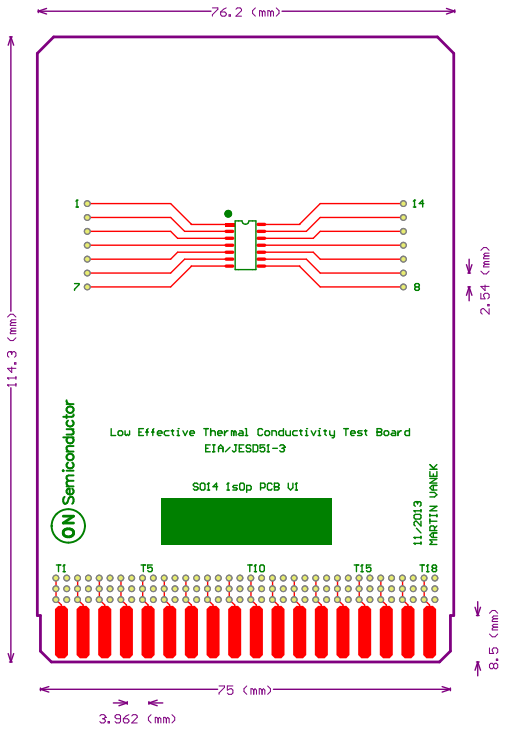


Fig. 5.5: *SO14 low effective thermal conductivity test board - top layer*

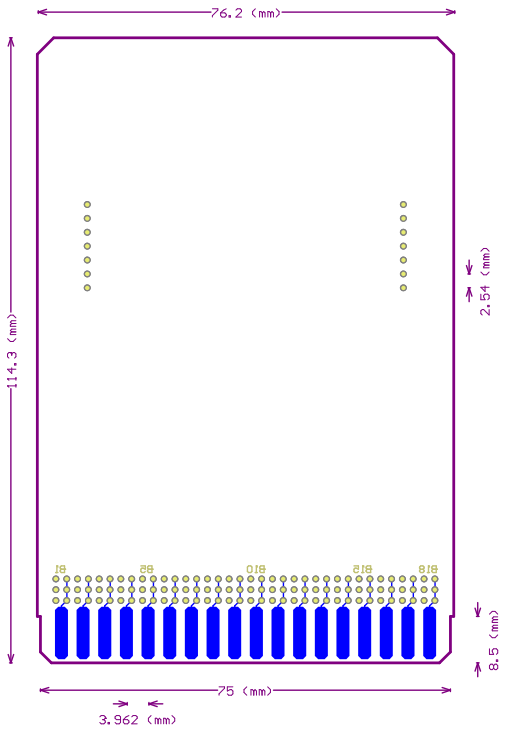


Fig. 5.6: *SO14 low effective thermal conductivity test board - bottom layer*

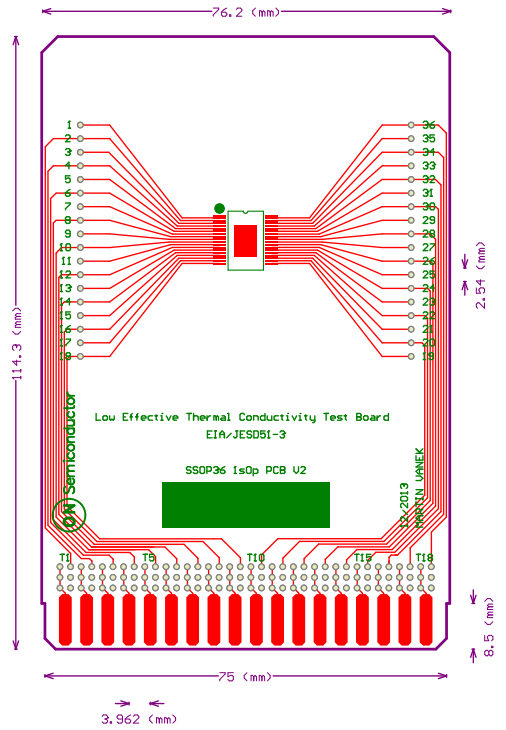


Fig. 5.7: *SSOP36-EP low effective thermal conductivity test board - top layer*

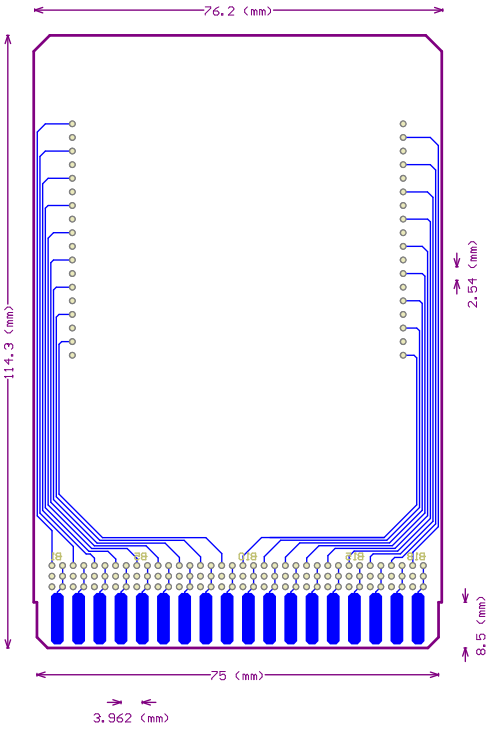


Fig. 5.8: *SSOP36-EP low effective thermal conductivity test board - bottom layer*

6 MEASURING OF TEMPERATURE COEFFICIENT OF A SEMICONDUCTOR STRUCTURE

Device NCV7430 was selected for this measurement. It is an automotive LIN (local interconnect network) RGB LED driver in SO14 package. Temperature coefficient of the structure between LED2C and LED2R pins was chosen for the evaluation. Graph 6.1 shows the V-I characteristic of this structure at approximately 25 °C ambient temperature. Positive terminal of the voltage source was connected to the LED2R pin.

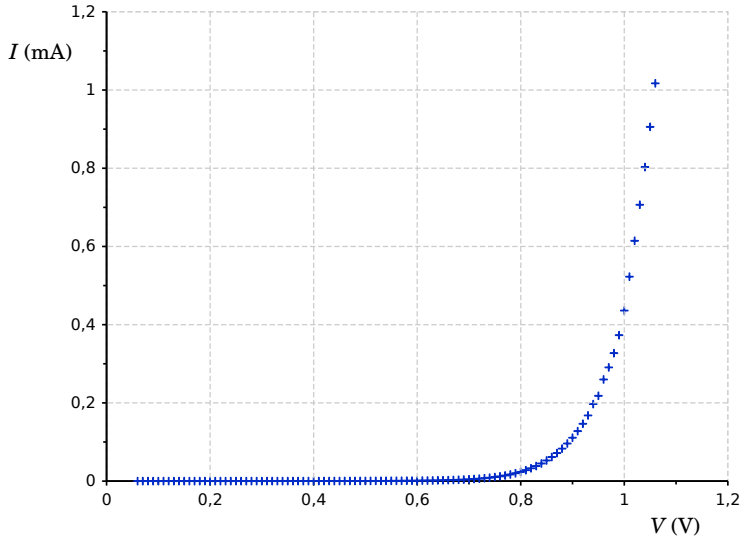


Fig. 6.1: *V-I characteristic of LED2C - LED2R structure of NCV7430*

Set-up of the measurement is shown in figure 6.2. Device under test (DUT) NCV7430 is placed between two temperature sensors LM35D in SO8 packages. These sensors convert measured temperature to voltage (10 mV/°C in used temperature range). A thermocouple was soldered to the board and connected to the calibrated converter. This PCB with the DUT and the temperature sensors was placed in the temperature forcing system. Supply voltage of the temperature sensors was set to +5V. Measuring devices, current source and temperature forcing system were connected to the computer by the GPIB (IEEE 488) to automate the measurement. Temperature was set in 10 °C intervals from 90 °C down to 10 °C. There was a 7 minute stabilization delay after each temperature change. Ten measurements were performed at each temperature with interval of 30 seconds between them. Each measurement consisted of applying 24 different values of current to the measured structure. Voltage drop across the structure, current flowing through the structure, and voltage values from the temperature sensors were measured for each current.

A set of values for each temperature was calculated to evaluate the measurement. This consists of current through the structure, voltage drop across the structure

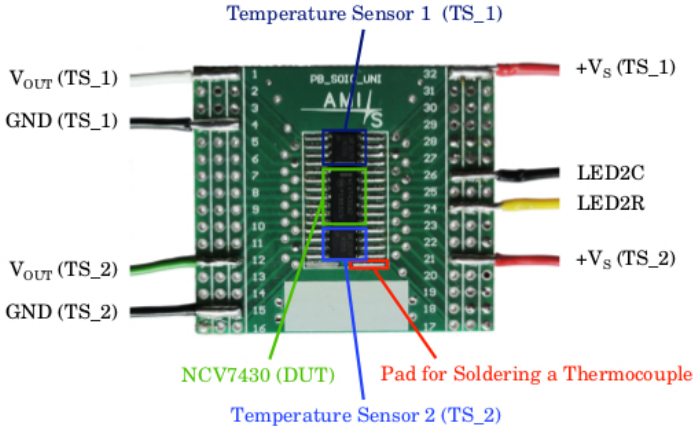


Fig. 6.2: *Setup of the thermal measurement*

and temperature. Current and voltage values were calculated as the average of ten measurements. Temperature was calculated as the average value of the measured data from both temperature sensors LM35D. This was done for all values of temperature. Calculated temperature vary less than 0,4 °C from the average values measured by the thermocouple. Graph 6.3 shows temperature dependent V-I characteristic of the structure between LED2C and LED2R pins of the NCV7430 device. As apparent from the graph, voltage drop across the structure decreases with increasing temperature at the constant current.

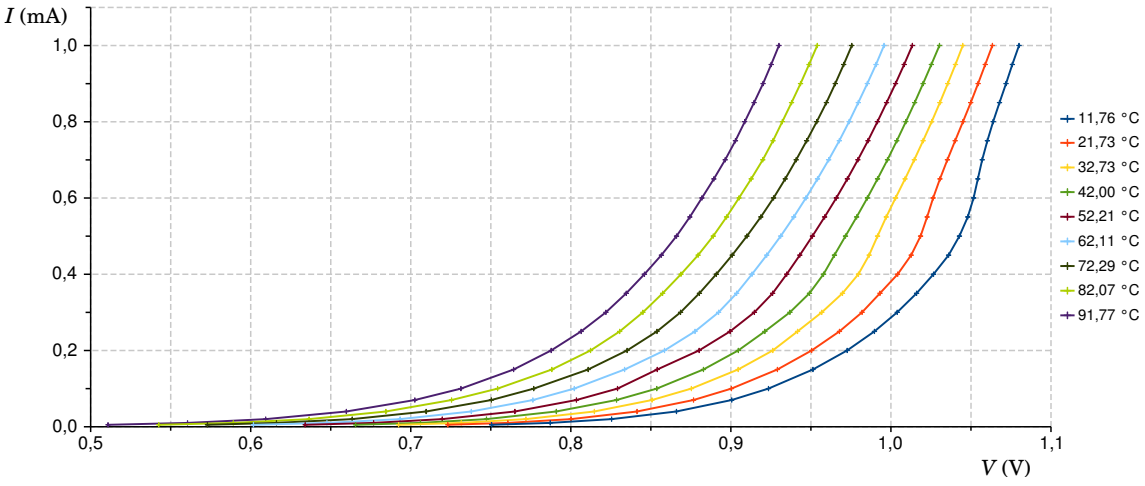


Fig. 6.3: *Temperature dependence of LED2C - LED2R characteristic*

Graph 6.4 depicts dependence of voltage drop on temperature for chosen currents. Linear regression lines were used for assessment. Slope of the line expresses the voltage change corresponding to 1 °C temperature change. Values for all currents are listed in table 6.5 together with mean absolute error (MAE), minimal and maximal error. MAE describes deviation of the measured values from the linear regression. The smallest MAE was

calculated for the 400 µA (gradient is $-2,25$ mV/°C). Maximal error for this current was 0,61 mV. This value represents temperature error less than 0,3 °C. It means that according to this measurement 400 µA through LED2C - LED2R structure is suitable current for sensing of internal temperature of the NCV7430 device.

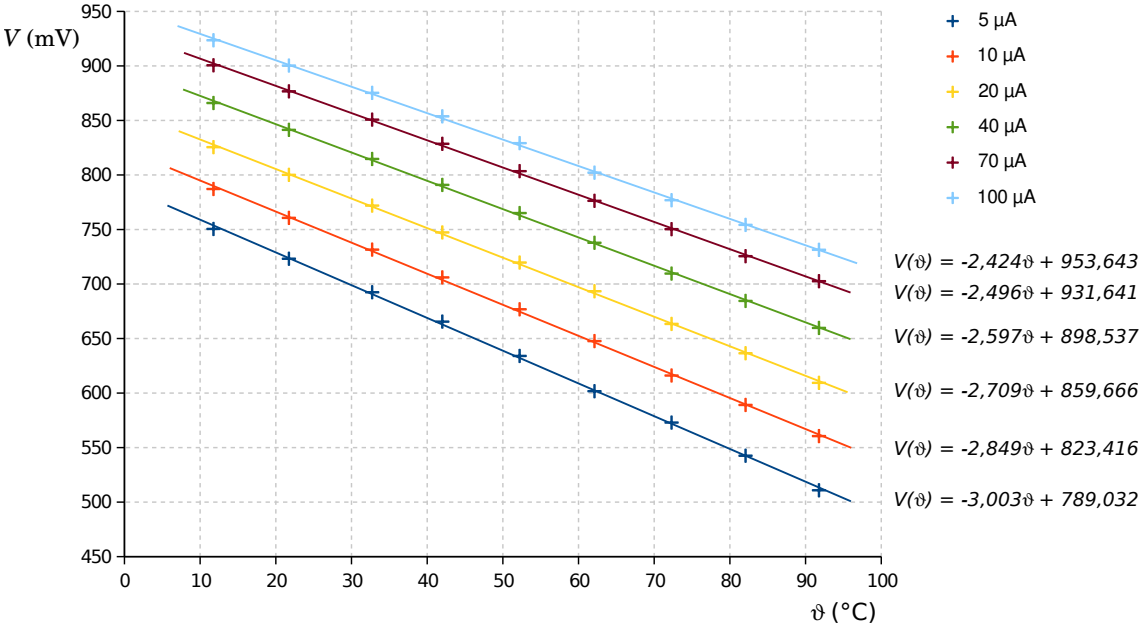


Fig. 6.4: *Temperature dependence of the voltage drop across LED2C - LED2R*

Tab. 6.5: *Table of the voltage gradients and errors*

I	**Gradient**	**Mean Absolute Error**	**Minimal Error**	**Maximal Error**
µA	$mV \cdot °C^{-1}$	mV	mV	mV
5	-3,00	1,59	0,02	3,18
10	-2,85	1,54	0,51	2,76
20	-2,71	1,29	0,39	2,28
40	-2,60	1,18	0,47	2,13
70	-2,50	1,07	0,02	2,19
100	-2,42	1,15	0,17	2,10
150	-2,34	1,09	0,28	3,32
200	-2,30	0,77	0,26	1,76
250	-2,72	0,90	0,01	2,07
300	-2,26	0,93	0,34	1,73
350	-2,62	0,72	0,36	1,20
400	**-2,25**	**0,38**	**0,01**	**0,61**
450	-2,22	1,11	0,03	2,33
500	-2,16	1,53	0,42	3,11
550	-2,11	1,74	0,52	3,55
600	-2,06	1,82	0,32	2,95
650	-2,00	1,74	0,56	3,25
700	-1,95	1,63	0,11	4,07
750	-1,92	1,86	0,11	4,75
800	-1,90	2,18	0,30	5,34
850	-1,88	2,40	0,37	5,73
900	-1,86	2,58	0,32	6,03
950	-1,84	2,82	0,22	6,50
1000	-1,83	2,98	0,28	6,85

7 THERMOCOUPLE CALIBRATION

The aim of the calibration was to evaluate the accuracy of two K-type thermocouples together with the FLUKE 80TK converter (converts thermocouple temperature to voltage with 1 mV $\cdot$ °C^{-1} ratio). Thermocouples were inserted into the water thermostat together with the PT100 temperature sensor (resistance temperature detector made of platinum) connected to a precise thermometer. Temperature from the PT100 was considered as the accurate value that served as a reference for the thermocouples.

Graph 7.3 shows the dependency of the absolute error of the thermocouples (together with the converter) on the reference temperature. As can be seen from the graph, temperature measurement error is less than 1 °C (both thermocouples meet JEDSD-51 requirements). Equations of the correction curves can be used for the acquired temperature corrections. Equation for the first thermocouple (TC1) correction curve is 7.1 and 7.2 for the second thermocouple (TC2).

$$\Delta\vartheta_{TC1} = -3,13 \cdot 10^{-4}\vartheta^2 + 3,36 \cdot 10^{-2}\vartheta - 0,107 \tag{7.1}$$

$$\Delta\vartheta_{TC2} = -3,08 \cdot 10^{-4}\vartheta^2 + 2,41 \cdot 10^{-2}\vartheta + 0,115 \tag{7.2}$$

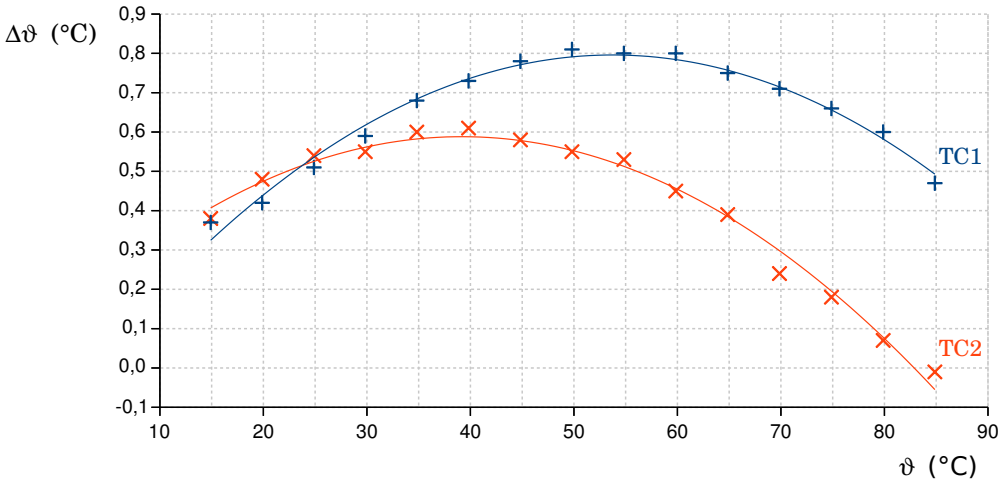


Fig. 7.3: *Thermocouple correction curves*

8 MEASUREMENT OF JUNCTION-TO-AMBIENT THERMAL RESISTANCE

Junction-to-ambient thermal resistance ($R_{\theta JA}$ or θ_{JA}) characterises the package of the electronic device (transistor, integrated circuits etc.). Lower thermal resistance means easier cooling of the device. Thermal resistance is usually given in $K \cdot W^{-1}$ or $°C \cdot W^{-1}$. It is not a constant, but it is influenced by many factors - air flow along the device, PCB design, attachment to the PCB, heat sink etc. Thus, it is important to follow the standard requirements (e.g. JESD51) to get a data that can serve as comparison of the devices and their packages.

8.1 Measurements with NCV7430 in SO14 Package

NCV7430 is an automotive LIN RGB LED driver that can be used to control RGB light emitting diodes in various applications. Junction-to-Ambient thermal resistance of the NCV7430 integrated circuit is 100 $K \cdot W^{-1}$ according to the datasheet [18]. This value was simulated for the high thermal conductivity test board that conforms JESD51 requirements.

Structure LED2R - LED2C was chosen for sensing of temperature inside the NCV7430. This structure was analysed in chapter 6. According to the previous measurements, LED2R - LED2C structure temperature dependency was characterised for 0,4 mA current. Temperature sensitive parameter (TSP) was voltage drop across the structure. Measured temperature coefficient was approximately $-2,04$ mV $\cdot$ $°C^{-1}$. The measurements were made for both rising and falling temperature, but the data collected from the falling temperature were more linear so they were used for calculations. The difference was probably caused by the temperature forcing system. The characteristics must be measured for each analysed sample because the values of TSP can vary.

Heating by applying power between GND pins 5 and 7 was chosen because the supply voltage affects of the chosen sensing structure. Schematic of the setup is shown in figure 8.1.

First measurement was done to estimate the time needed to get the steady state when applying the heating power. It was done on the 1s0p (one signal layer and no inner copper layers) thermal conductivity test board. Time measurements were not precise but it has no impact on the thermal resistance accuracy. The dependency of calculated θ_{JA} on measurement time can be seen on figure 8.2. According to the acquired data, 15 minutes should be enough to get the accurate value of θ_{JA}.

Following measurements of θ_{JA} were made for different levels of heating power. Before applying the power, thermal equilibrium inside the natural convection chamber was evaluated. Heating power was then applied and all needed values were recorded. Afterwards, thermal resistance was calculated for t_1 (15 minutes), $t_2 = 1,1 \cdot t_1$ (16,5 minutes) and $t_3 = 1,2 \cdot t_1$ (18 minutes). Steady-state thermal resistance has been reached

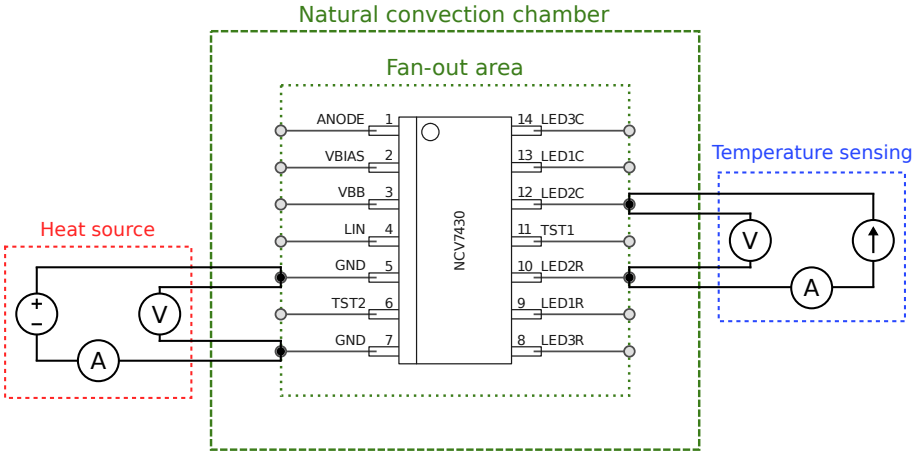


Fig. 8.1: *Schematic of setup #1*

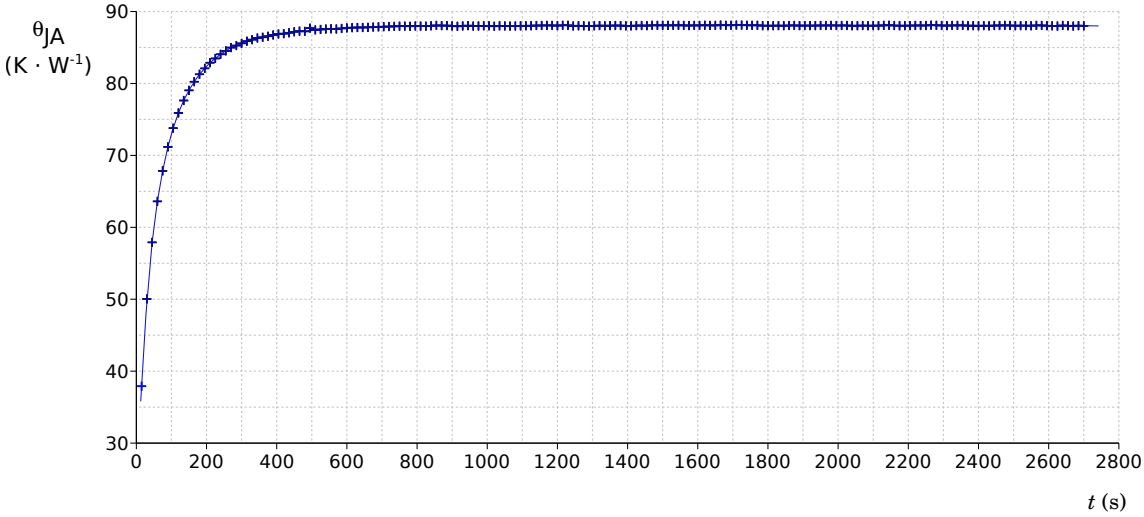


Fig. 8.2: *Steady state evaluation (NCV7430)*

if equations 8.3 and 8.4 are true. Value of junction-to-ambient thermal resistance is then $\theta_{\mathrm{JA}}(t_3)$.

$$|\theta_{\mathrm{JA}}(t_1) - \theta_{\mathrm{JA}}(t_2)| \leq 0,01 \cdot \theta_{\mathrm{JA}}(t_1) \tag{8.3}$$

$$|\theta_{\mathrm{JA}}(t_1) - \theta_{\mathrm{JA}}(t_3)| \leq 0,01 \cdot \theta_{\mathrm{JA}}(t_1) \tag{8.4}$$

Table 8.6 shows applied heat power, calculated temperature increase inside the device and junction-to-ambient thermal resistance. Thermal resistance slightly increases with rising power. Thermal resistance of the device on the 1s2p thermal test PCB was approximately 45 % lower than on the 1s0p PCB. Compared to the datasheet, measured thermal resistance is two times smaller. This significant deviation is probably caused by

the wrong selection of the heating structure. The heat source is probably too distant from the sensing structure and heating might be done only by wire bonds and ground metallisation. This causes that temperature of the hot spot and sensing structure could be different and value of the thermal resistance is spoiled. Equations 8.5 show an example of the $\theta_{\mathrm{JA}}(t_3)$ calculation for the first row of the table. Heating power is calculated as product of current flowing between GND pins 5 and 7 and voltage drop across this structure.

$$\begin{aligned} \theta_{\mathrm{JA}} &= \frac{T_{\mathrm{I}} + \Delta V_{\mathrm{s}} \cdot K - T_{\mathrm{F}}}{P_{\mathrm{H}}} \\ \theta_{\mathrm{JA}} &= \frac{27,10 + [(-63,50) \cdot (-0,4894)] - 27,12}{0,351} \\ \boldsymbol{\theta_{\mathrm{JA}}} &= \mathbf{88 \ \ K \cdot W^{-1}} \end{aligned} \tag{8.5}$$

Tab. 8.6: *Junction-to-ambient thermal resistance of NCV7430 (setup #1)*

Heat Power (mW)	$\boldsymbol{\Delta\vartheta}$ (°C)	$\boldsymbol{\theta_{\mathrm{JA}}}$ ($\mathrm{K \cdot W^{-1}}$)
1s0p PCB		
351	31,1	**88**
380	34,6	**90**
408	37,7	**92**
442	41,4	**93**
1s2p PCB		
416	20,9	**50**
448	22,9	**51**

Because the datasheet value of the thermal resistance was twice as high as the measured one, new set-up for measurement was created. GND - TST1 structure was chosen for temperature sensing. Before measuring the temperature sensitive parameter, independence of this structure on supply voltage was evaluated. Graph 8.7 shows the measurement of the temperature sensitive parameter. Voltage drop is measured at 0,4 mA.

Figure 8.8 shows the measurement setup. Filtering 100 nF ceramic capacitor between VBB (pin 3) and GND (pin 7) is not shown. Heat inside the IC is generated by driving four 1N4148 diodes, that substitute the light emitting diode. At the beginning of the measurement, sensing current is applied. After reaching thermal equilibrium in the natural convection chamber (sensing voltage drop change in 5 minutes is less then equivalent of 0,2 °C or less) LED2 driver is turned on (the device is controlled over the LIN). The power dissipation in the device is calculated as supply power minus diodes and resistor power.

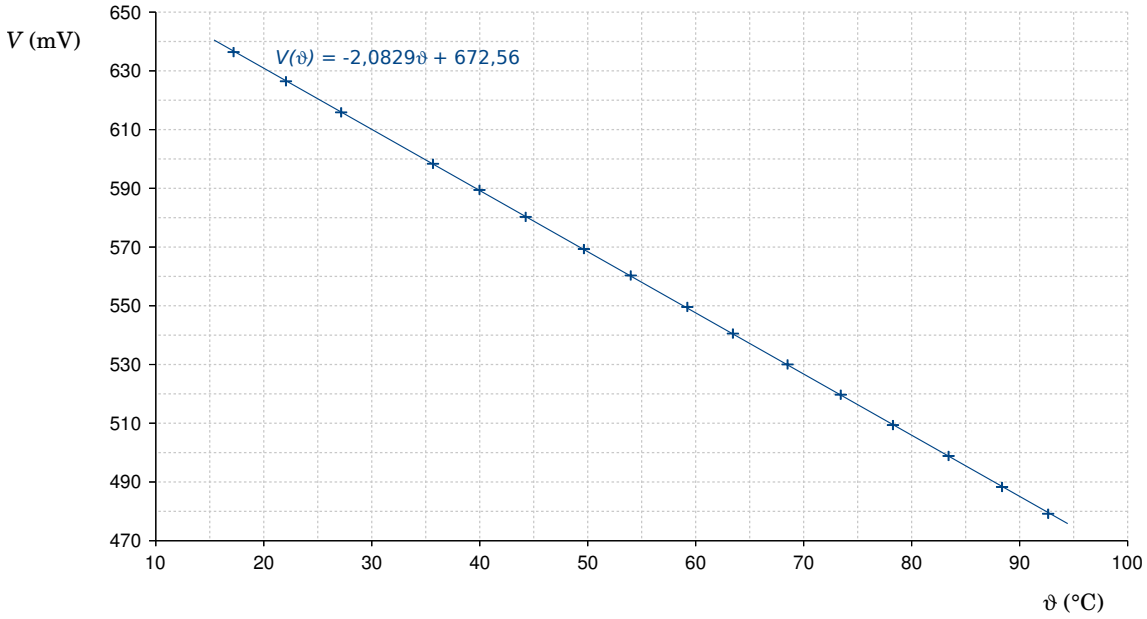


Fig. 8.7: *Temperature sensitive parameter measurement*

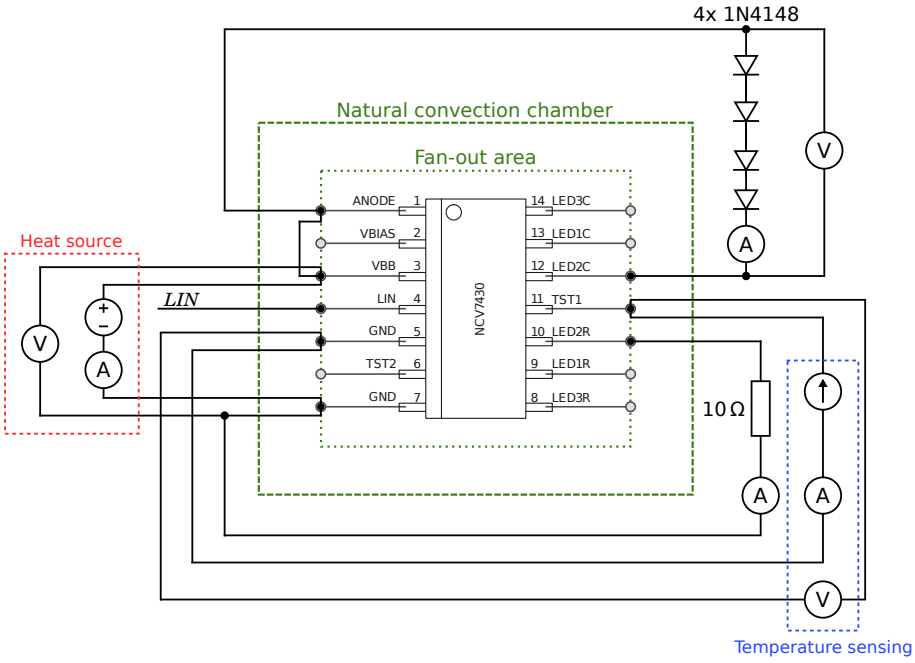


Fig. 8.8: *Schematic of setup #2*

Table 8.10 shows calculated values of the junction-to-ambient thermal resistance. First part shows the values for the low effective thermal conductivity test board. Thermal resistance was almost constant in the whole range of applied power.

The most of measurements were made on the 1s2p thermal conductivity test board. There is almost 40% drop of thermal resistance in comparison with 1s0p PCB. Four dif-

ferent samples were used for the measurements. As can be seen in the table, repeatability of the measurements is very good. The difference between the smallest and highest calculated thermal resistance is 2 $\mathrm{K} \cdot \mathrm{W}^{-1}$. Equations 8.9 show the calculations for the first row of the table.

$$\begin{aligned} \theta_{\mathrm{JA}} &= \frac{T_{\mathrm{I}} + \Delta V_{\mathrm{s}} \cdot K - T_{\mathrm{F}}}{P_{\mathrm{H}}} \\ \theta_{\mathrm{JA}} &= \frac{26,94 + [(-91,64) \cdot (-0,4848)] - 26,98}{0,396} \\ \boldsymbol{\theta_{JA}} &= \mathbf{112 \ \ K \cdot W^{-1}} \end{aligned} \tag{8.9}$$

Tab. 8.10: *Junction-to-ambient thermal resistance of NCV7430 (setup #2)*

Sample # (-)	**Heat Power** (mW)	$\boldsymbol{\Delta\vartheta}$ (°C)	$\boldsymbol{\theta_{JA}}$ ($\mathrm{K} \cdot \mathrm{W}^{-1}$)
1s0p PCB			
1	396	44,4	**112**
1	468	52,1	**111**
1	503	56,1	**111**
1	504	56,2	**111**
1s2p PCB			
1	503	34,8	**68**
1	611	41,7	**68**
1	611	41,9	**69**
1	612	42,2	**69**
1	612	42,5	**69**
1	684	46,7	**68**
2	483	32,7	**68**
2	482	32,8	**68**
2	587	39,7	**68**
2	587	39,5	**68**
3	497	34,3	**68**
3	497	33,8	**68**
3	604	41,2	**68**
3	604	41,4	**68**
4	507	34,7	**68**
4	616	41,9	**68**
4	725	49,1	**67**
4	835	56,4	**67**
4	946	63,6	**67**

8.2 Measurements with NCV7707 in SSOP-EP Package

NCV7707 is an integrated driver for automotive body control systems. It is designed to control several loads in the front door of a vehicle. Datasheet value of the junction-to ambient thermal resistance is 42 °C · W^{-1} for the 1-layer PCB and 19,5 °C · W^{-1} for the 4-layer PCB. This values are based on 76,2 x 114,3 mm FR4 printed circuit boards. Copper thickness of 1-layer PCB is 72 µm and copper area coverage is 20 %. The inner layers of the 4-layer PCB are made of 36 µm copper with 90 % area coverage (other parameters are same as for the 1-layer PCB). [19]

Two structures were chosen for temperature sensing. One near the heat source and the other on the opposite side of the IC. The chosen structures can be seen on figure 8.11. According to the analysis, SCLK-VCC structure is independent of both heating and sensing by the GND-ECFB. Sensing voltage across the GND-ECFB is influenced by heating signal and also by SCLK-VCC sensing. The temperature sensitive parameters were analysed together to suppress the effect of SCLK-VCC sensing (figures A13 and A14).

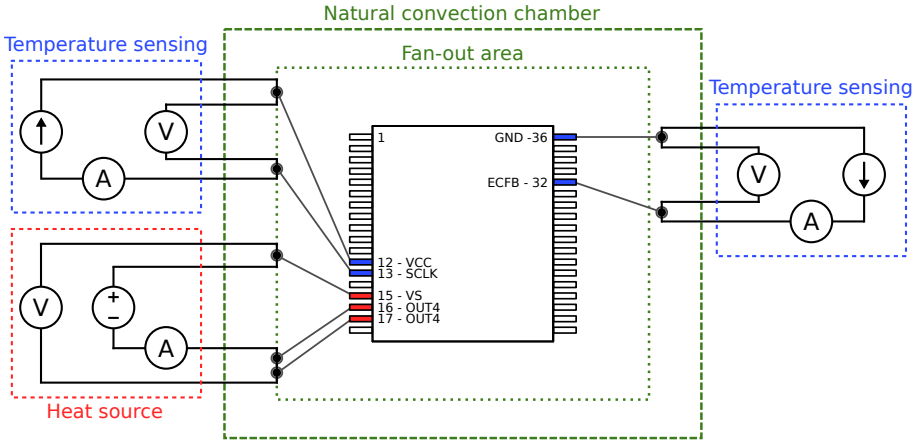


Fig. 8.11: *Schematic of measurement setup*

Figure 8.12 shows the voltage across the GND-ECFB structure during the heat power switching on (measurements were done with sample #2). Horizontal dashed lines show the voltage level before and after switching. The behaviour of GND-ECFB was characterised for different switching levels of heating power and correction curve was made (figure 8.13). Figure 8.14 depicts the evaluation measurement of the steady state time (data from SCLK-VCC are shown). To reduce time needed for the further measurements, 10 minutes was considered as sufficient time to reach steady-state (15 minutes were used for measurements with NCV7430). Steady-state conditions 8.3 and 8.4 were checked for all measurements to ensure reliability of the results.

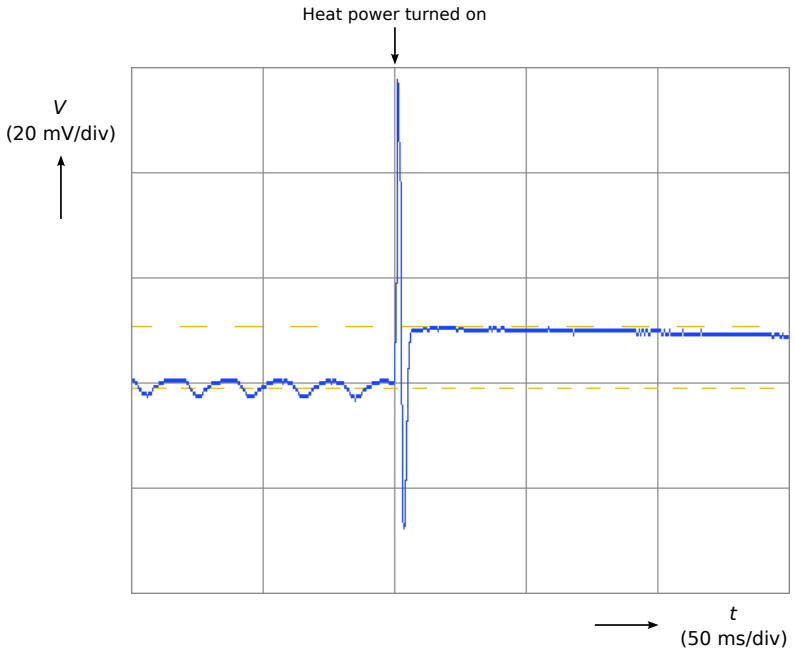


Fig. 8.12: *GND-ECFB voltage*

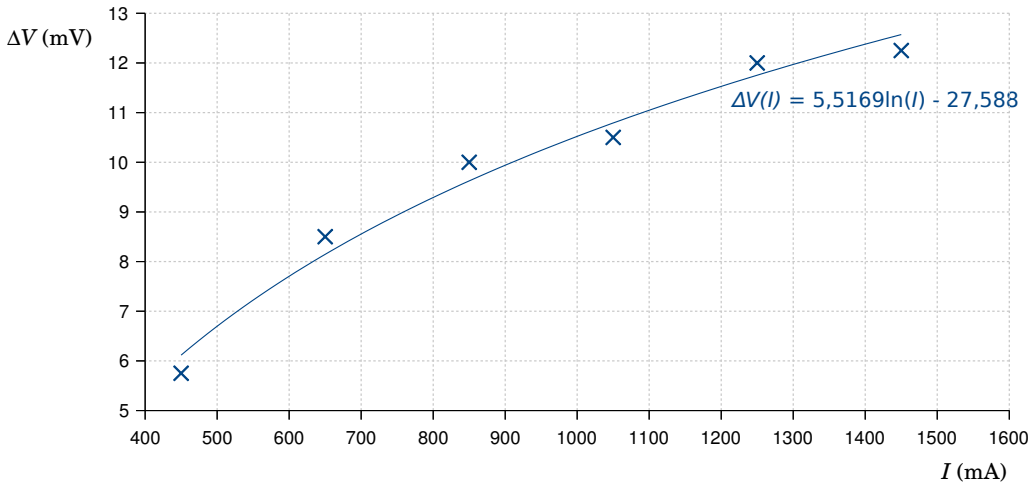


Fig. 8.13: *GND-ECFB voltage shift error*

Table 8.15 shows the results for measurements on the low effective thermal conductivity test board. Values $\Delta\vartheta_1$ and $\theta_{\mathrm{JA\_1}}$ are based on SCLK-VCC sensing, values $\Delta\vartheta_2$ and $\theta_{\mathrm{JA\_2}}$ on GND-ECFB sensing. Calculated junction-to-ambient thermal resistance varied from 70,8 K · W^{-1} to 75,9 K · W^{-1}. Higher values correspond to the lower heat power. Datasheet thermal resistance for the 1s0p test PCB is 42 K · W^{-1}. The deviation is probably caused by different copper coverage area. Original JEDS-51 test board has much less than 20% copper coverage area. Soldering exposed pad of the IC to the test board has very low effect on thermal resistance (around 1 K · W^{-1}). Some of the temperature

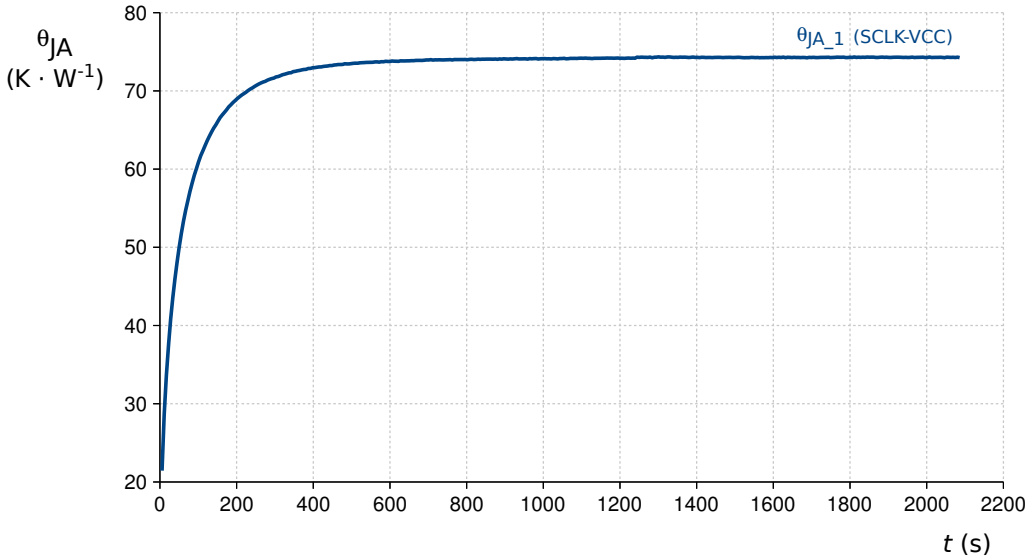


Fig. 8.14: *Steady state evaluation (NCV7707)*

differences sensed by the GND-ECFB (structure more distant from the heat source) are slightly higher than the differences sensed by the SCLK-VCC. It is probably caused by the inaccurate data corrections of the GND-ECFB.

Tab. 8.15: *Junction-to-ambient thermal resistance of NCV7707 (1s0p PCB, sample #1)*

Soldered Exposed Pad	**Heat Power** (mW)	$\Delta\vartheta_1$ (°C)	$\Delta\vartheta_2$ (°C)	θ_{JA_1} (K · W^{-1})	θ_{JA_2} (K · W^{-1})
no	350	26,9	26,8	**75,9**	**75,5**
no	434	32,7	32,7	**75,0**	**74,9**
yes	517	38,0	38,3	**73,2**	**73,7**
yes	517	37,7	38,0	**73,1**	**73,7**
no	518	38,4	38,5	**74,0**	**74,2**
no	519	38,7	38,6	**74,1**	**73,9**
no	606	44,7	44,9	**73,3**	**73,7**
no	691	50,4	50,9	**72,6**	**73,3**
no	781	56,5	57,1	**72,0**	**72,8**
no	781	56,4	57,1	**71,9**	**72,9**
yes	781	55,4	56,3	**70,9**	**72,0**
yes	781	55,4	56,3	**70,8**	**72,0**
yes	784	56,0	56,5	**71,1**	**71,8**

Tables 8.16 and 8.17 show the measurement results for the high effective thermal conductivity test board (1s2p). Measurements were done with two different samples of NCV7707. First one is the same as was used with the 1s0p test PCB. In comparison with the 1s0p test PCB, calculated thermal resistance for the 1s2p PCB is more than twice as small. Values for the measurements with the exposed pad not soldered to the PCB varied form 31,2 K · W^{-1} up to 35,1 K · W^{-1}. The highest value was measured for the smallest heat power (sensed temperature increase was less than 20 °C - minimum temperature increase recommended by the JESSD-51).

Soldering NCV7707 exposed pad to the PCB caused approximately 7 K · W^{-1} decrease of junction-to-ambient thermal resistance. Despite the decrease, it is still more than 6,5 K · W^{-1} higher than the datasheet value. Superscripts in the first column of 8.17 table express the number of resoldering. For the last soldering, very small amount of solder paste was used for exposed pad attachment. As can be seen from the results, soldering process has negligible effect in comparison with PCB design. Repeatability of measurements was very good while using the same heating power.

Tab. 8.16: *Junction-to-ambient thermal resistance of NCV7707 (1s2p PCB, sample #1)*

Soldered Exposed Pad	**Heat Power** (mW)	$\Delta\vartheta_1$ (°C)	$\Delta\vartheta_2$ (°C)	θ_{JA_1} [K · W^{-1}]	θ_{JA_2} [K · W^{-1}]
no	363	12,9	12,5	**35,1**	**34,0**
no	450	15,9	15,3	**34,8**	**33,5**
no	539	19,1	18,2	**34,8**	**33,5**
no	539	19,0	18,2	**34,7**	**33,3**
no	630	21,8	20,8	**34,4**	**32,8**
no	724	24,9	23,6	**34,2**	**32,4**
no	819	28,1	26,5	**34,0**	**32,1**
yes	825	22,6	21,4	**27,0**	**25,6**
no	916	31,2	29,4	**33,8**	**31,9**
yes	924	25,0	23,6	**26,8**	**25,3**
yes	924	25,0	23,7	**26,8**	**25,3**
no	1014	34,4	32,3	**33,8**	**31,6**
yes	1026	27,6	26,0	**26,7**	**25,1**
no	1116	37,5	35,1	**33,4**	**31,3**
yes	1127	30,1	28,2	**26,5**	**24,9**
yes	1127	30,1	28,3	**26,5**	**24,9**
no	1218	41,2	38,4	**33,5**	**31,2**
yes	1231	33,2	31,0	**26,4**	**24,7**
yes	1234	33,0	30,7	**26,4**	**24,5**
yes	1340	35,6	33,1	**26,2**	**24,4**

Tab. 8.17: *Junction-to-ambient thermal resistance of NCV7707 (1s2p PCB, sample #2)*

Soldered Exposed Pad	**Heat Power** (mW)	$\boldsymbol{\Delta\vartheta_1}$ (°C)	$\boldsymbol{\Delta\vartheta_2}$ (°C)	$\boldsymbol{\theta_{JA\_1}}$ ($K \cdot W^{-1}$)	$\boldsymbol{\theta_{JA\_2}}$ ($K \cdot W^{-1}$)
yes[1]	365	10,3	10,3	**27,5**	**27,5**
yes[2]	542	15,1	14,9	**27,5**	**27,1**
yes[2]	729	20,1	19,4	**27,3**	**26,3**
yes[2]	923	25,3	24,1	**27,1**	**25,8**
yes[3]	1125	31,4	29,8	**27,5**	**26,2**
yes[3]	1125	31,2	29,7	**27,4**	**26,0**
yes[1]	1126	30,3	27,7	**26,3**	**24,0**
yes[1]	1126	29,9	27,3	**26,3**	**23,9**
yes[2]	1126	30,6	28,7	**26,7**	**25,1**
yes	1127	29,6	27,1	**25,9**	**23,7**
yes	1127	29,7	27,9	**26,2**	**24,6**
yes	1128	30,0	28,1	**26,4**	**24,7**
yes	1129	30,0	28,0	**26,3**	**24,5**
yes	1129	30,0	28,0	**26,3**	**24,6**
yes[2]	1338	36,2	33,8	**26,7**	**24,9**
yes[1]	1339	35,1	31,9	**26,1**	**23,7**

9 THERMAL RESISTANCE MEASUREMENTS AND EVALUATION METHODOLOGY

This chapter summarizes steps for thermal resistance measurements and its evaluation together with practical advice. This work focuses on junction-to-ambient thermal resistance measurement in the natural convection chamber. For the accurate thermal measurements it is essential to have a natural convection chamber, thermal conductivity test boards and temperature sensors meeting the JESD51 requirements. After choosing the integrated circuit for evaluation, subsequent steps may follow.

1 Choice of Temperature Sensing structure

This step is very important for further measurements and their accuracy. Temperature sensitive parameter (TSP) is used for temperature sensing inside the integrated circuit. It is usually a voltage drop across some internal structure that is accessible from the IC pins. It can be for example bulk diode or ESD protection.

Before measuring temperature dependence of the chosen structure, it is useful to check if the structure is not affected by the signal that will be used for heating the IC. In such case it is recommended to choose another structure. If there is no other available structure, influence of the heating signal has to be studied thoroughly to avoid measurement errors.

Before thermal measurements it is appropriate to measure the volt-ampere characteristics of the structure. It can help to choose the sensing current. Voltage drop caused by the current should be higher than cut-in voltage (under cut-in voltage, small current source inaccuracy could cause error in voltage drop measurement). It depends on structure, but 0,4 mA sensing current should be large enough to gain suitable voltage drop. It is important to bear in mind that high current can cause self heating of the sensing structure.

2 Measurement of K Factor

Integrated Circuit should be placed in the temperature forcing environment to measure temperature dependence of the chosen structure. It is desirable to measure the TSP in the whole temperature range that will be used for further measurements.

Temperature of the integrated circuit can be measured by thermocouple attached to the integrated circuit. Thermocouple accuracy should be better than 1 °C. To gain accurate data, sufficient time should be used for temperature stabilization after each temperature change. Afterwards, measurement of the TSP can be done (sensing current can be turned on during the whole measurement). It is suitable to record more values for each temperature to reduce the effect of the temperature forcing system instability.

Data evaluation consists of few steps. First one is averaging of measured values (temperature and TSP) if multiple measurements were done for each temperature. Calculated values can be plotted as a graph of TSP (mostly voltage) temperature dependence. Reciprocal of the linear best fit regression line slope is the K factor usually given in $°C \cdot V^{-1}$.

3 Measurement of Junction-to-Ambient thermal resistance

An analysed device must be soldered to the high effective or low effective thermal conductivity test board that conforms the JESD-51 requirements. All deviations from the standard must be stated in the measurement report. Wiring should be done to enable four wire measurements. Forcing and sensing wires should meat at the fan-out vias to minimize the measurement error.

After placing thermal conductivity test board with the device to the natural convection chamber, initial thermal equilibrium must be evaluated. It is done by measuring the temperature sensitive parameter. Its change in five minutes interval must be less than equivalent of 0,2 °C.

Initial temperature and value of TSP are recorded after reaching initial equilibrium. First measurement should be done for long time (e.g. 30 minutes) to estimate sufficient time for the steady-state thermal resistance. It can be read from the graph of time dependence of thermal resistance calculated using the equation 9.1, where T_I is initial temperature, ΔTSP is change of the TSP caused by heating, K is ratio of junction temperature change to TSP change, T_F is final ambient temperature and P_H is heat power.

$$\theta_\mathrm{JA} = \frac{T_\mathrm{I} + \Delta TSP \cdot K - T_\mathrm{F}}{P_\mathrm{H}} \tag{9.1}$$

To ensure reliability of the results, steady state should be evaluated after each measurement (equations 8.3 and 8.4). Measurements of the TSP and ambient temperature are taken after t_1, $(1,1 \cdot t_1)$ and $(1,2 \cdot t_1)$ (t_1 is estimated time of steady-state thermal resistance). If junction-to-ambient thermal resistance values calculated for each time comply with 8.3 and 8.4, value for $(1,2 \cdot t_1)$ is taken as a final result. If the steady-state conditions aren't met, new measurement with longer time has to be done.

Table 9.2 shows an example of the report from measurement of the junction-to-ambient thermal resistance. Highlighted rows must be filled. Report would be useless without one of these pieces of information (package type is not necessary if the device is manufactured only in one package type). Filling the rest of the table is recommended, because it specifies measurement conditions and can serve for example for the correlation measurements. Attaching schematics of the measurement setup can be beneficial, too.

Tab. 9.2: *Recommended θ_{JA} measurement report*

Date	
Measured by	
Analysed device	
Package type	
Sample designation	
Measurement environment	Natural convection / Forced convection
Test board type	1s0p / 1s2p ...
Sensing structure	
Sensing current	
***K* factor**	
Heating structure	
Heating power	
Initial temperature	
Final ambient temperature	
Initial value of TSP	
Final value of TSP	
Junction temperature increase	
Heating time	
Steady-state evaluation	
Junction-to-ambient thermal resistance	
Notes	

CONCLUSION

This work consists of two main parts. The first one is theoretical and deals with the heat transfer related topics. The second part contains the natural convection chamber construction, printed circuit board design and evaluation of thermal properties.

Measurements have shown that the crucial moment is selection of the sensing and heating structures. Temperature sensitive parameter should be electrically independent of heating, otherwise proper analysis of the heat signal influence is necessary. Repeatability of measurements was very good for the constant heat power.

Measurements with NCV7430 in SO14 package were done with two setups (different sensing and heating structures). The ground structure was used for heating in the first setup because of the supply voltage impact on the temperature sensitive parameter. Values of junction-to-ambient thermal resistance gained with the second setup should be more precise (heat source was a LED driver near the sensing structure). Simulated value from the datasheet (100 K $\cdot$ W^{-1}) is more than 30 K $\cdot$ W^{-1} higher than the measured one. Significant influence of the printed circuit board was observed for both setups. High effective thermal conductivity test board (PCB with 2 inner layer) causes approximately 40% decrease of thermal resistance in comparison with low effective thermal conductivity test board (PCB without inner layers). This shown that the printed circuit board plays an important role in the thermal performance of the devices. Thermal properties of different samples were almost identical.

Door-module driver NCV7707 is manufactured in SSOP36 package with an exposed pad. According to the datasheet, junction-to-ambient thermal resistance is 42 K $\cdot$ W^{-1} for the 1-layer PCB and 19,5 K $\cdot$ W^{-1} for the 4-layer PCB with 20% copper coverage area of signal layers and 90% copper coverage area of inner planes (both different from the standard JESD-51 test boards). Analysed device was tested on both low and high effective thermal conductivity test boards. Thermal resistance varied from 70,8 K $\cdot$ W^{-1} to 75,9 K $\cdot$ W^{-1} on the 1s0p test PCB. Variations were caused by the different heat power. Soldering exposed pad to the PCB caused approximately 1 K $\cdot$ W^{-1} decrease of thermal resistance. High effective thermal conductivity test board (1s2p) caused more than 47% decrease of thermal resistance. Calculated temperature difference between two sensing structures was rising with increasing heat power. It was 2,4 °C for the highest applied heat power (1s2p test PCB, sample #2).

Results of the measurements can be used for evaluation of the thermal simulations accuracy. It can also help to design PCBs preventing overheating of the devices.

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ABBREVIATIONS AND ACRONYMS

C-PVC	Chlorinated Polyvinyl Chloride
DUT	Device Under Test
EIA	Electronic Industries Alliance
EP	Exposed Pad
ETM	Electrical Test Method
FR4	Flame Retardant 4 (PCB material)
GPIB	General Purpose Interface Bus
IEC	International Electrotechnical Commission
IR	Infrared
JEDEC	Joint Electron Devices Engineering Council
JESD	JEDEC Standard
LIN	Local Interconnect Network
MAE	Mean Absolute Error
NTC	Negative Temperature Coefficient
PCB	Printed Circuit Board
PTC	Positive Temperature Coefficient
SO	Small-Outline (integrated circuit package type)
SSOP	Shrink Small-Outline Package
TC	Thermocouple
TSP	Temperature Sensitive Parameter
1s0p	Printed circuit board with one signal layer and without inner layers
1s2p	Printed circuit board with one signal layer and two inner copper layers

LIST OF SYMBOLS

A (m^2)	Area
h_c $(\mathrm{W} \cdot \mathrm{m}^{-2} \cdot \mathrm{K}^{-1})$	Convective heat transfer coefficient
I (A)	Current
k $(\mathrm{W} \cdot \mathrm{m}^{-1} \cdot \mathrm{K}^{-1})$	Coefficient of thermal conductivity
K $(\mathrm{K} \cdot \mathrm{V}^{-1})$	Ratio of junction temperature change to TSP change
L (m)	Length
P (W)	Power
$\vec{q}$ $(\mathrm{W} \cdot \mathrm{m}^{-2})$	Heat flux
Q (W)	Heat
$R_{\theta \mathrm{JX}}$ $(\mathrm{K} \cdot \mathrm{W}^{-1})$	Thermal resistance
t (s)	Time
T (K)	Absolute temperature
ΔT (K)	Temperature difference
∇T $(\mathrm{K} \cdot \mathrm{m}^{-1})$	Temperature gradient
V (V)	Voltage
ε (-)	Emissivity
ϑ (°C)	Temperature
$\Delta \vartheta$ (°C)	Temperature difference
θ_{JX} $(\mathrm{K} \cdot \mathrm{W}^{-1})$	Thermal resistance
θ_{JA} $(\mathrm{K} \cdot \mathrm{W}^{-1})$	Junction-to-ambient thermal resistance
λ (m)	Wavelength
σ $(\mathrm{W} \cdot \mathrm{m}^{-2} \cdot \mathrm{K}^{-4})$	Stefan-Boltzmann constant

LIST OF FIGURES

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APPENDIX

Photos of Natural Convection Chamber

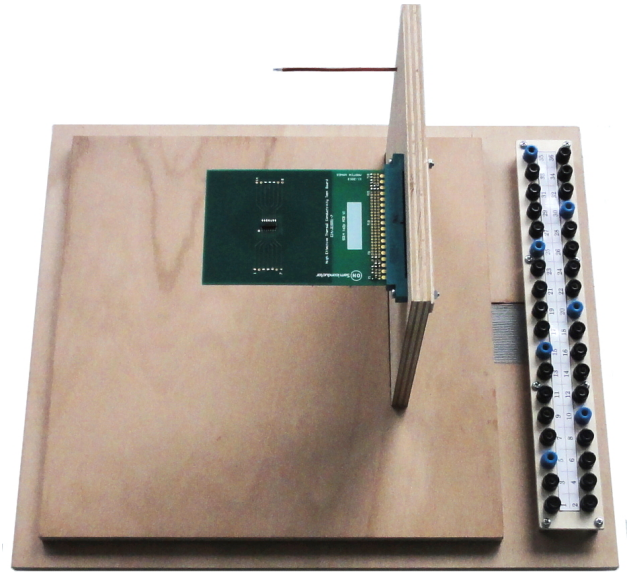

Fig. A3: *Natural convection chamber (without enclosure #1)*

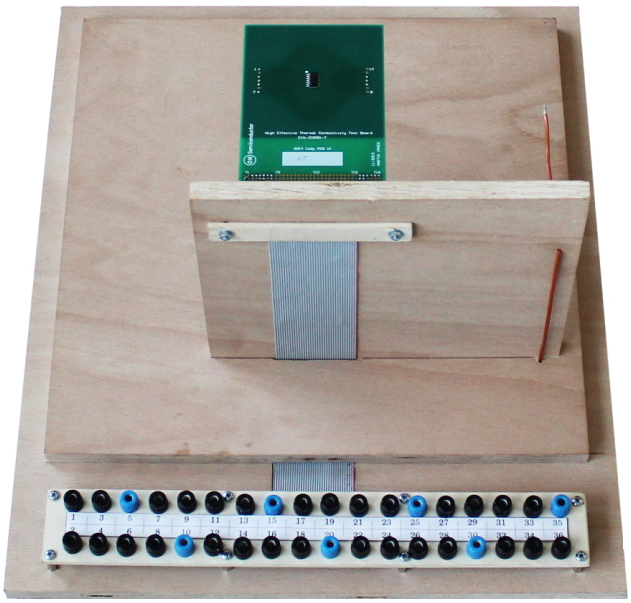

Fig. A4: *Natural convection chamber (without enclosure #2)*

High Effective Thermal Conductivity Test Boards

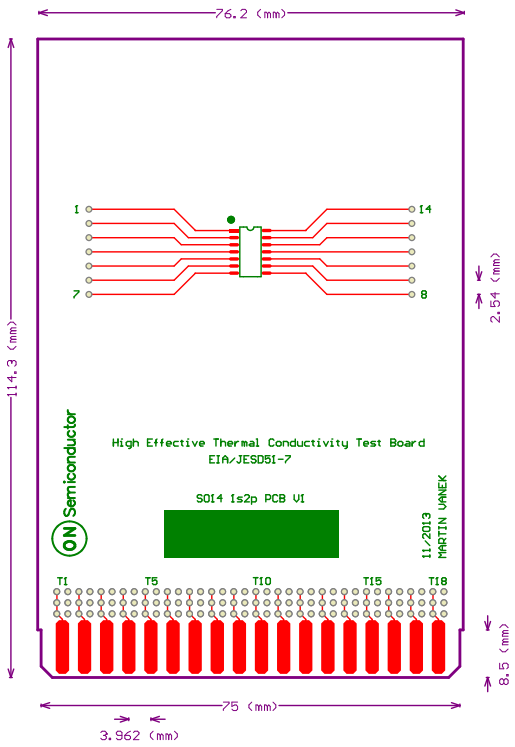

Fig. A5: *SO14 high effective thermal conductivity test board - top layer*

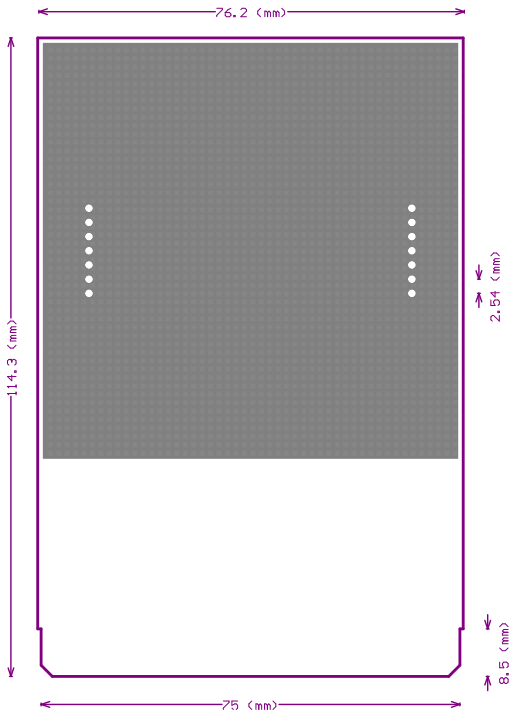

Fig. A6: *SO14 high effective thermal conductivity test board - inner layer 1*

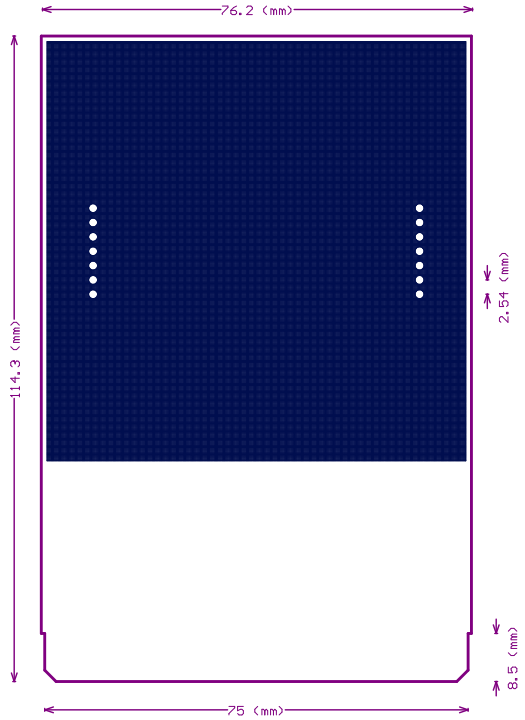

Fig. A7: *SO14 high effective thermal conductivity test board - inner layer 2*

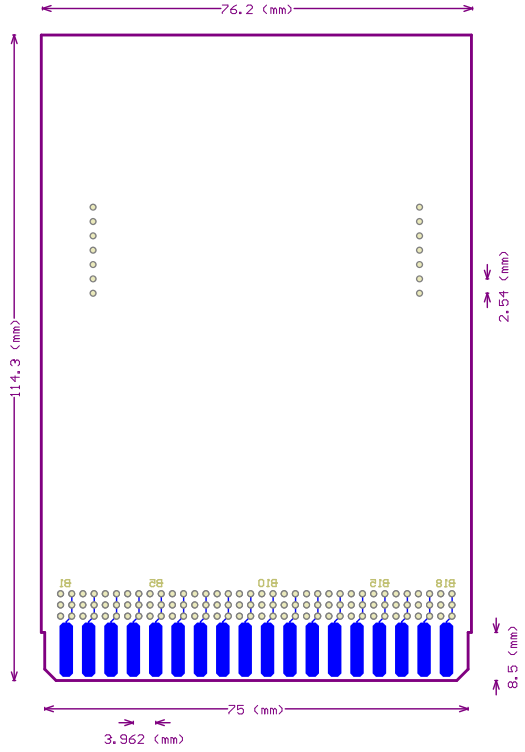

Fig. A8: *SO14 high effective thermal conductivity test board - bottom layer*

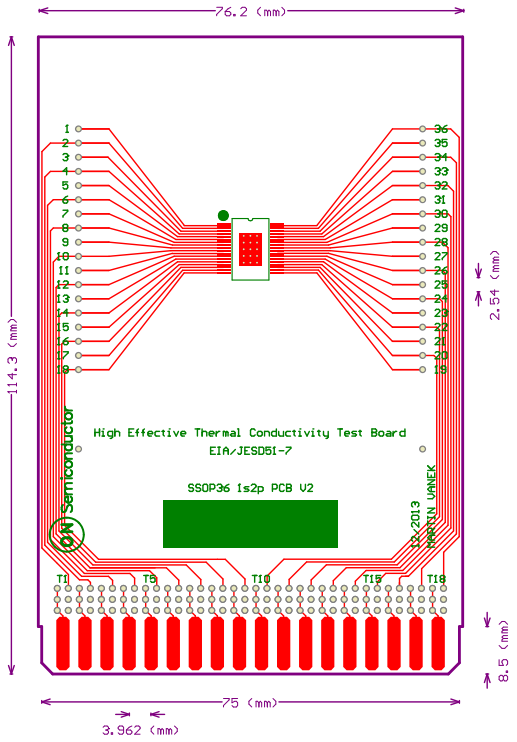

Fig. A9: *SSOP36-EP high effective thermal conductivity test board - top layer*

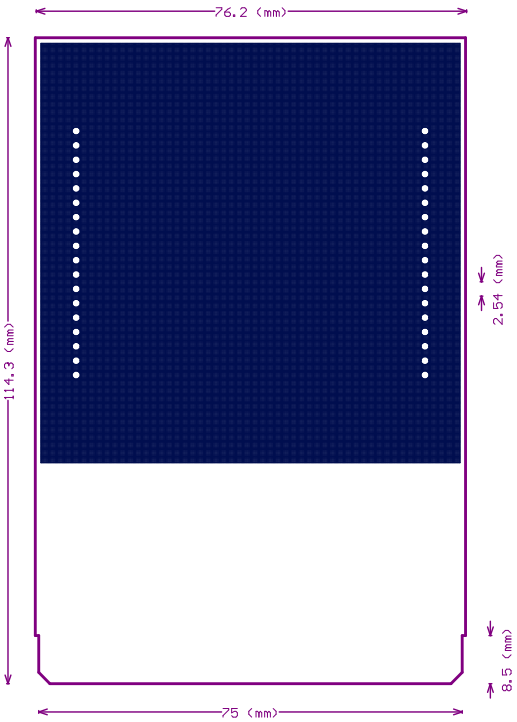

Fig. A10: *SSOP36-EP high effective thermal conductivity test board - inner layer 1*

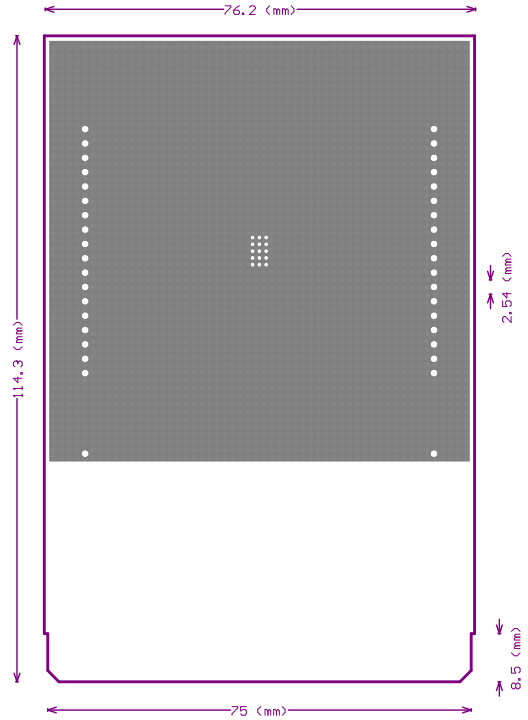

Fig. A11: *SSOP36-EP high effective thermal conductivity test board - inner layer 2*

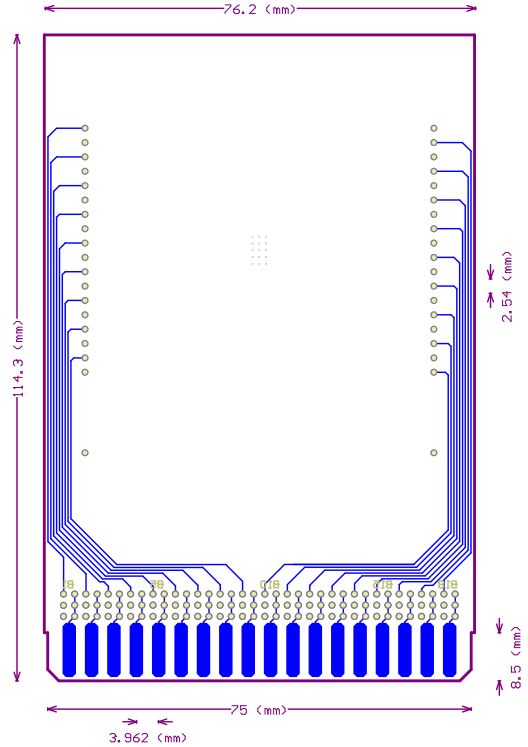

Fig. A12: *SSOP36-EP high effective thermal conductivity test board - bottom layer*

Temperature Sensitive Parameters Evaluation

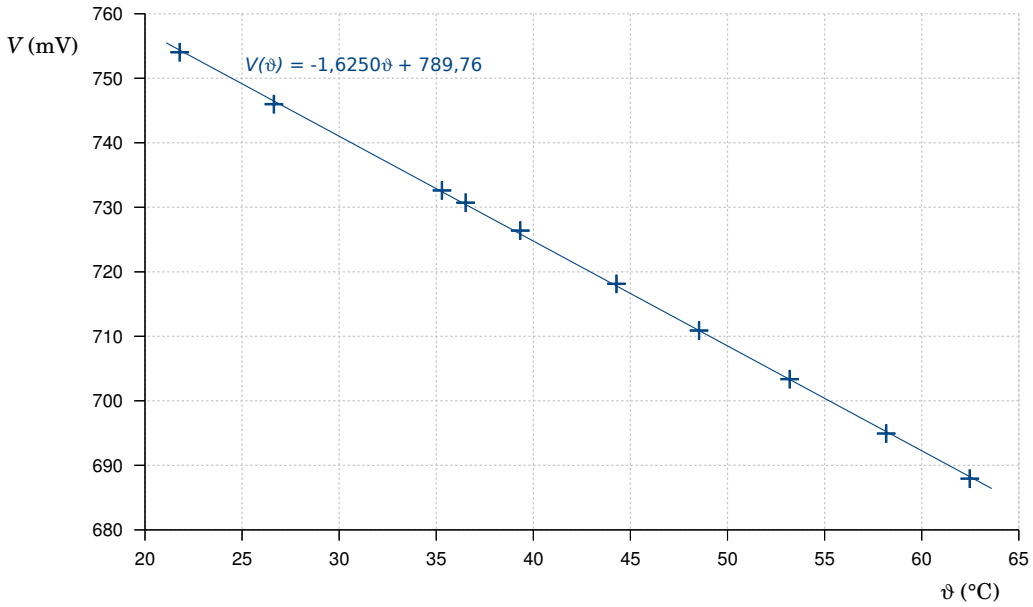

Fig. A13: *SCLK-VCC temperature sensitive parameter (sample #1)*

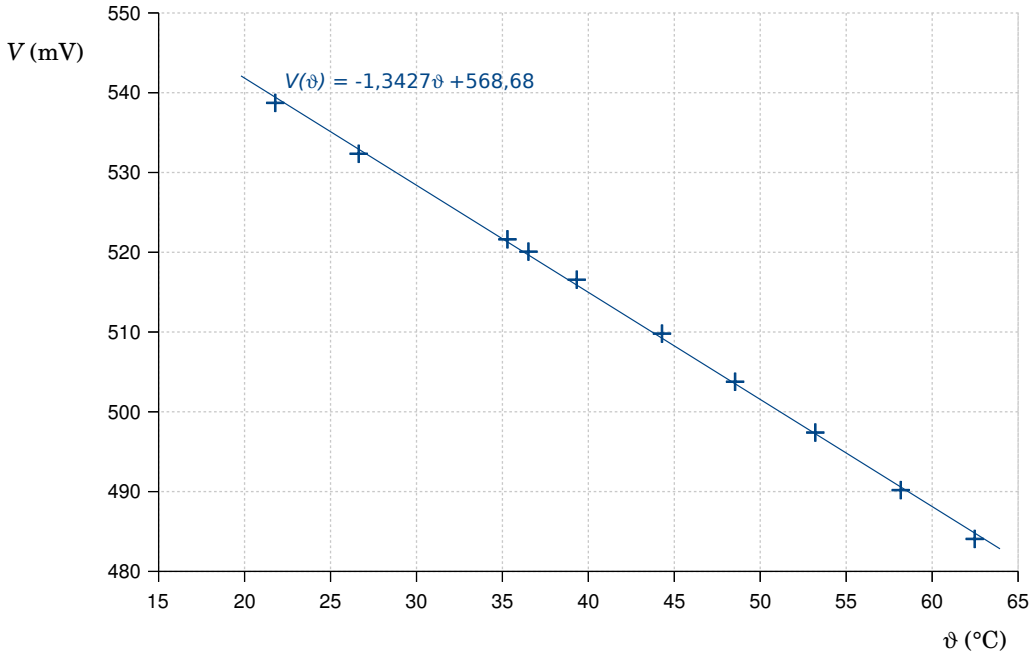

Fig. A14: *GND-ECFB temperature sensitive parameter (sample #1)*