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Designing Series of Fractional-Order Elements

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Abstract In this paper we propose an efficient approach to design fractional-order elements' (FOEs) series, while using a very limited set of "seed" FOEs. The proposed approach follows the idea of general immittance inverter/converter, whereas a suitable circuit solution employing operational transconductance amplifiers is also presented and can be used for the design of grounded fractional-order elements with the fractional order α being in the range $[-2, 2]$. The proposed circuit may simply be extended to design fractional-order elements from wider range of α to follow designers' requirements. To show the efficiency of the described technique, the use of only up to two "seed" FOEs with properly selected fractional order α_{seed} as passive elements results in the design of a series of 17 FOEs with different α being in the range $[-2, 2]$. Cadence post-layout simulation results are presented that prove operability and robustness of our design concept. Basic fractional 1.75-order low-pass filter is also presented to show the utilization of a FOE being implemented by the proposed GIC.

Keywords Fractional-order element · Transformation · Immittance inverter/converter · OTA

1 Introduction

During the last few decades, fractional-order calculus gained significant attention in various engineering areas, as e.g. in control or modelling it provides beneficial properties compared to classic integer-order systems [6], [22]. The efficient utilization of fractional-order calculus and systems may also be observed in agriculture [27], biology [9], electrical engineering [4] or cryptography

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[28]. Dealing signal processing, controller, or generally analogue function block design, the fractional-order element (FOE) as discrete element (together with other passive and active elements) becomes essential for the implementation of the required circuit solution. However, the presence of FOE as readily available discrete element is not common yet. In [20] a comprehensive survey of recent progress and possible design techniques and approaches to implement FOEs of capacitive type are described, but all of them are still at the stage of laboratory experiments and samples used by the individual research groups. Therefore, to design and mainly evaluate the performance of fractional-order systems, the required FOEs (capacitive-type) are nowadays suitably emulated by RC networks, like Foster, Cauer or Valsa topologies, [5], [16], [26], [12], [18].

In [25], a systematic procedure for designing Foster-I, Foster-II, Cauer-I and Cauer-II RC networks, which approximate the capacitive FOE with generally any values of its parameters (i.e. the pseudo-capacitance C_α and the fractional-order α) in a required frequency range is presented. However, the values of individual resistors and capacitors of the RC network must be precise to obtain the required accuracy of the approximation [25]. Requiring new values of C_α and/or α also requires to determine new values of individual resistors and capacitors of the RC network. Additionally as also shown in [11], values of α being close to zero (0) or unity (1) results in very high ratio in values of resistors and capacitors in the RC network. As consequence, individual research groups dealing with fractional-order circuits design mostly use their "tuned" RC network with fix C_α and α for all their designs, which does not much contribute to the spread of the beneficial features of fractional-order approach among the research community.

Although variety of systems and their parameters may be broad, similarly as in classic circuit design defined series in values of resistors and capacitors are used, we propose a concept of designing a series in fractional order α of fractional-order elements. The advantage is that using only a very limited number of "seed" ("tuned") fractional-order elements, a high number of final FOEs with different fractional order α can be obtained thanks to suitable transformation of the initial discrete elements. Employing transconductance operational amplifiers (OTAs), a general immittance inverter/converter is proposed that together with a selected "seed" FOE is further analysed to prove the operability of the presented concept. Our preliminary results were already presented in [13], whereas here the ideas and reached results are more elaborated and extended. Having the active elements designed in CMOS TSMC 0.18 μm technology, post-layout simulations of the final structure are also presented and discussed to further support the theoretical assumptions. Using single "seed" FOE with it fractional order 0.25 we show the potential of the proposed concept in obtaining a series of 17 new FOEs, primarily different in their fractional order being in the range of $[-2, 2]$. Additionally, a frequency filter is designed as an example of possible utilization of the synthesized FOE.

2 General description of fractional-order elements

The fractional-order elements (FOE) (also referred to as Constant-Phase Elements (CPEs) [10], Elements with Fractional Impedance (EFI) [14], or Fractors [2]), are either of capacitive or inductive type and hence, the fractional-order (also simply denoted as fractional) capacitor C_α and fractional inductor L_β with their impedance are defined as follows [25]:

$$Z_{C\alpha}(\omega) = \frac{1}{\omega^\alpha C_\alpha} \exp\left(-j\alpha\frac{\pi}{2}\right), \tag{1}$$

and

$$Z_{L\beta}(\omega) = \omega^\beta L_\beta \exp\left(j\beta\frac{\pi}{2}\right), \tag{2}$$

where $0 < \alpha < 1$ and $0 < \beta < 1$ are the fractional orders, and C_α and L_β are the pseudo-capacitance and pseudo-inductance specified with their units $[\mathrm{F/s}^{1-\alpha}]$ and $[\mathrm{H/s}^{1-\beta}]$, respectively. The phase of the impedance is for both types of fractional elements constant in whole frequency range, whereas according to (1) it equals to $-\alpha\pi/2$ for fractional capacitor and according to (2) it equals to $\beta\pi/2$ for fractional inductor.

As presented in [25], the fractional capacitor and its pseudo-capacitance C_α may be at specific frequency ω_0 represented as capacitor with capacitance C that features the same impedance at ω_0:

$$C = \frac{C_\alpha}{\omega_0^{1-\alpha}}, \tag{3}$$

whereas an equivalent inductor with its inductance L featuring the same impedance at frequency ω_0 as the fractional inductor with its pseudo-inductance L_β may be specified as:

$$L = \frac{L_\beta}{\omega_0^{1-\beta}}. \tag{4}$$

From the above definitions and nomenclature of capacitive and inductive type FOEs it may be evident that their description can be simplified. Assuming $\beta = -\alpha$ then for positive and negative values of α the fractional capacitors and inductors are assumed, respectively. Such simplification in nomenclature is further assumed in this paper and hence only α is used.

3 Concept of designing FOEs' series

The idea of designing a series in fractional order α of FOEs stems in efficient utilization of immittance inverter/converter to which a "seed" fractional-order element is connected. The utilization of general immittance inverter/converter in designing fractional-order elements was already discussed e.g. in [8], [24], [23], or [1], where operational amplifier based Antoniou's general immittance converter (GIC) is used. The approach discussed e.g. in [23] generally enables to obtain at the input of the GIC new FOE with fractional order being in the

range $[-2, 2]$, however always assumes unique and different fractional-order element with specific value of α (in the paper values 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8 were assumed). The papers [8], [24], and [1] utilize GIC for the design fractional inductors only. Hence, here we further develop the idea of using GIC to design a series of FOEs using a very limited count of initial "seed" FOEs.

Assume a general function block as shown in Fig. 1 that is represented by suitable interconnection of four general admittances Y_1, Y_2, Y_3 and Y_4 to an active/passive network, whereas the active elements may be of arbitrary type. Let the input impedance of such general function block be defined as:

$$Z_{\mathrm{IN}} = \frac{Y_1 Y_3}{Y_2 Y_4} \frac{1}{g}, \tag{5}$$

where g is a transconductance specific for the active/passive network. The external general admittances Y_1, Y_2, Y_3 and Y_4 may be represented by any type of passive element, such as conductor (G), inductor (L), capacitor (C), or fractional-order element (FOE). Assuming only the phase of the input impedance Z_{IN} represented by the fractional order α, it can be written:

$$\alpha = -\alpha_1 - \alpha_3 + \alpha_2 + \alpha_4, \tag{6}$$

whereas α_i represents the order of the specific admittance Y_i based on its type, i.e. for conductor $\alpha_i = 0$, for inductor $\alpha_i = -1$, for capacitor $\alpha_i = 1$ and for fractional-order element $\alpha_i = \alpha_{\mathrm{FOE}}$ $(-1 < \alpha_{\mathrm{FOE}} < 1)$.

Replacing the general admittances Y_1, Y_2, Y_3 and Y_4 by selected types of passive elements, one of the following types of passive (synthetic) element specified with its fractional order α can generally be obtained at the input of the immittance inverter/converter:

- frequency dependent negative resistor - type I (FDNR-I) with $\alpha = 2$,
- fractional FDNR-I, i.e. $1 < \alpha < 2$,
- capacitor C, i.e. $\alpha = 1$,
- capacitive FOE, i.e. $0 < \alpha < 1$,
- conductor G, i.e. $\alpha = 0$,
- inductive FOE, i.e. $-1 < \alpha < 0$,
- inductor L, i.e. $\alpha = -1$,
- fractional frequency dependent negative resistor - type II (FDNR-II), i.e. $-2 < \alpha < -1$, or
- FDNR-II, i.e. $\alpha = -2$.

The frequency dependent negative resistor - type I (FDNR-I), in the literature also referred to as the D element [3], exhibits purely real negative resistance that decreases in magnitude with increasing frequency, and is commonly used for frequency filter design, e.g. [17], whereas FDNR-II also exhibits purely real negative resistance but its magnitude increases with increasing frequency.

As mentioned in section 1, there are techniques to approximate the required FOE with specific parameters directly using a suitable RC network. However, for each different circuit implementation another FOE with different

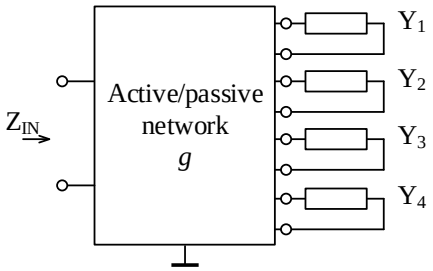


Fig. 1 General view on immittance inverter/converter.

parameters is required. This fact results in limited performance analysis of fractional-order circuits as the research groups use their "tuned" FOE with trimmed values of resistors and capacitors in the specific RC network approximating the FOE. Such "tuned" FOEs may be advantageously used as "seed" FOEs in immittance inverter/converter and based on (6) result in a series of fractional-order elements primarily with different fractional order α.

Such utilisation of "seed" FOE is very efficient as shown below. Assume a "seed" FOE with fractional order $\alpha_{\text{seed}} = 0.25$ that together with classic conductor and capacitor is used to replace the external admittances Y_1, Y_2, Y_3 and Y_4 from Fig. 1. Various combinations of these three types of passive elements (always assuming to employ up to two capacitors and/or two "seed" FOEs) result in one of the 17 different values of fractional order α of the input impedance Z_{IN} from the range $[-2, 2]$ as listed in Table 1. Note that also other combinations of passive elements than listed in Table 1 may be described, however the final value of α will be still one of the 17 already present.

Next to obtaining a series in fractional-order α specifying the value of constant phase of the input impedance Z_{IN}, through appropriate setting of the conductance G_i, capacitance C_i and/or of the transconductance g of the active/passive network the magnitude of the input impedance may also be set arbitrary although the pseudo-capacitance $C_{\alpha\text{seed}}$ of the "seed" FOE is fix. It also may be evident that it is not a must to use the same "seed"FOEs while replacing selected general admittances Y_1, Y_2, Y_3 and Y_4. For example, assuming "seed" FOEs with $\alpha_{\text{seed1}} = 0.25$ and $\alpha_{\text{seed2}} = 0.0625$ results even in 51 different values of fractional order α of input impedance Z_{IN} again from the range $[-2, 2]$. These features make the concept of using "seed" FOEs in an immittance inverter/converter much more robust as this approach very easily results in the possibility to obtain new FOEs featuring required parameters.

4 Proving the concept

The theoretical concept of obtaining a series in fractional order α of fractional-order elements is further verified by proposing an immittance inverter/converter and analysing its performance. As active elements, the operational transcon-

Table 1 Variant combinations of admittances Y_i and their α_i vs. final fractional order α of Z_{IN} for $\alpha_{\mathrm{seed}} = 0.25$.

α_1	α_2	α_3	α_4	α	Z_{IN} type
0	1	0	1	2.00	FDNR-I
0.25	1	0	1	1.75	fractional FDNR-I
0.25	1	0.25	1	1.50	
0	1	0	0.25	1.25	
0	1	0	0	1.00	capacitor C
0.25	1	0	0	0.75	capacitive FOE
0	0.25	0	0.25	0.50	
0	0.25	0	0	0.25	
0	0	0	0	0.00	conductor G
0.25	0	0	0	−0.25	inductive FOE
0.25	0	0.25	0	−0.50	
1	0.25	0	0	−0.75	
1	0	0	0	−1.00	inductor L
1	0	0.25	0	−1.25	fractional FDNR-II
1	0.25	1	0.25	−1.50	
1	0.25	1	0	−1.75	
1	0	1	0	−2.00	FDNR-II

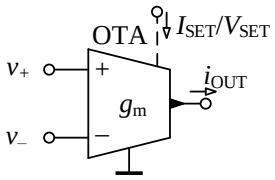


Fig. 2 Schematic symbol of OTA.

ductance amplifiers (OTAs) are used. Generally OTA (Fig. 2) is a voltage-controlled current source and is defined by the following expression [19]:

$$i_{\mathrm{OUT}} = g_{\mathrm{m}}(v_+ - v_-), \tag{7}$$

where g_{m} is the transconductance of the active element and most commonly is also understood to be adjusted by an external dc current I_{SET} (or dc voltage V_{SET}).

The proposed solution of the immittance inverter/converter employing seven OTAs is shown in Fig. 3. Basically, it can be divided into upper and lower section, composed of OTAs (and corresponding admittances) indexed by odd and even numbers, respectively. Both sections result in an impedance, whereas admittances Y_2 and Y_4 are converted and admittances Y_1 and Y_3 are inverter to the input of the GIC. Based on mathematical algebra and using

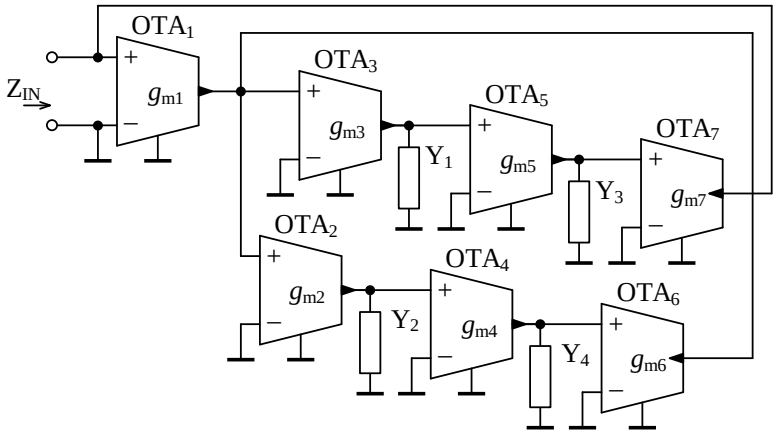


Fig. 3 Proposed immittance inverter/converter.

(7), the input impedance of the proposed circuit solution can be then derived as:

$$Z_{\mathrm{IN}} = \frac{Y_1 Y_3}{Y_2 Y_4} \frac{g_{\mathrm{m2}} g_{\mathrm{m4}} g_{\mathrm{m6}}}{g_{\mathrm{m1}} g_{\mathrm{m3}} g_{\mathrm{m5}} g_{\mathrm{m7}}}. \tag{8}$$

Comparing (5) and (8), it is evident that the input impedance of the proposed immittance inverter/converter (8) fully corresponds with the theoretically required input impedance defined by (5) to follow the proposed concept since:

$$\frac{1}{g} = \frac{g_{\mathrm{m2}} g_{\mathrm{m4}} g_{\mathrm{m6}}}{g_{\mathrm{m1}} g_{\mathrm{m3}} g_{\mathrm{m5}} g_{\mathrm{m7}}}, \tag{9}$$

and hence it is proved that the above described concept of designing a series in values of fractional order α in the range of $[-2, 2]$ of fractional-order elements is feasible. Additionally, assuming OTAs as active elements, from (8) or (9) it can be seen that the also the module of the input impedance can be set for individual values of α and hence the obtainable series new FOEs further increases.

The circuit from Fig. 3 may simply be extended to provide wider range of achievable values of α by expanding the upper and lower (i.e. with odd and even indexes) cascade of admittances and OTAs. The extra added passive and active elements cause continuation of products of admittances Y and transconductances g_{m} in (8). The range of α of such extended immittance inverter/converter is then $[-m, n]$, where m is the number of admittances with odd index (i.e. in the upper cascade) and n is the number of admittances with even index (i.e. in the lower cascade).

5 Simulation results

To verify the behaviour of the proposed immittance inverter/converter, post-layout simulations were performed. Below, the employed OTA designed in

TSMC 0.18nm CMOS technology is described and followed with the post-layout simulation results and performance evaluation of the whole circuit.

5.1 Employed OTA cell

The OTA cell employed in the immittance inverter/converter was adopted from the work [21] and its behavioural structure is shown in Fig. 4. It has two pairs of differential voltage inputs, which are fed into two differential summation blocks. The outputs of these blocks are multiplied first mutually and then with a constant k resulting into two differential output currents with the same magnitude and different direction. The external connection of the terminals of this cell as OTA is apparent from Fig. 4.

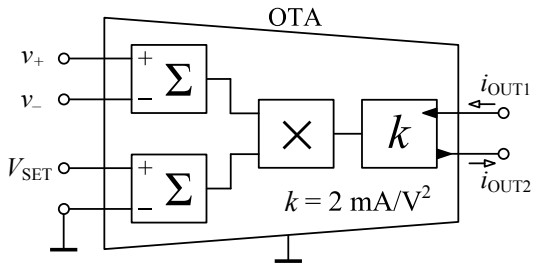


Fig. 4 Behavioral structure of the used OTA cell.

The following relation holds for the output currents

$$i_{\mathrm{OUT1}} = i_{\mathrm{OUT2}} = kV_{\mathrm{SET}}(v_+ - v_-), \tag{10}$$

where the constant $k = 2$ mA/V^2. Following (7), the relation between g_{m} and V_{SET} is given by:

$$g_{\mathrm{m}} = kV_{\mathrm{SET}}. \tag{11}$$

The simulated dependence of the value of transconductance g_{m} on control voltage V_{SET} is depicted in Fig. 5 proving the relation (11) and the possibility of electronic setting of g_{m}. It can be observed that the characteristic is linear for V_{SET} ranging from 0 to 0.5 V.

5.2 Performance analysis of the immittance inverter/converter

To show the design of a series of FOEs, the "seed" FOE with fractional order $\alpha_{\mathrm{seed}} = 0.25$ and at central frequency $f_0 = 1$ kHz featuring equivalent capacitance 159.2 nF, i.e. based on (3) having the pseudo-capacitance $C_{\alpha\mathrm{seed}} = 112.3\ \mu\mathrm{F/s}^{0.75}$, is used. Also here we face the issue that a suitable

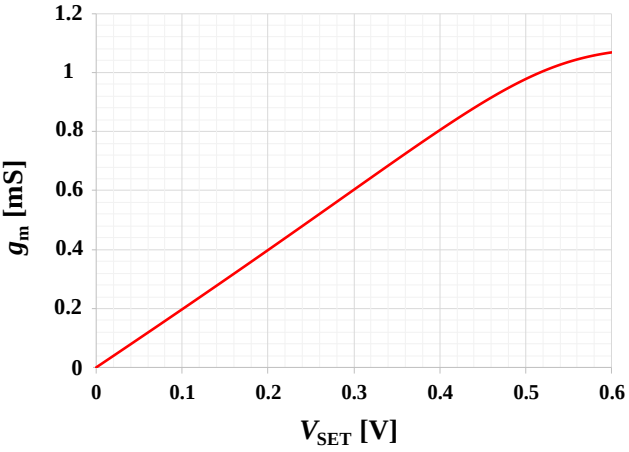


Fig. 5 The dependence of the parameter g_{m} on V_{SET} of the OTA cell.

"seed" FOE is not commercially available. Therefore, we approximate the required "seed" FOE using 5th-order Foster-II topology as shown in Fig. 6, whereas the values of resistors and capacitors were determined using the approach as described in [25] and are summarized in Table 2.

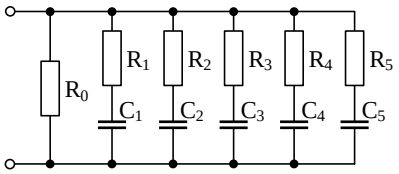


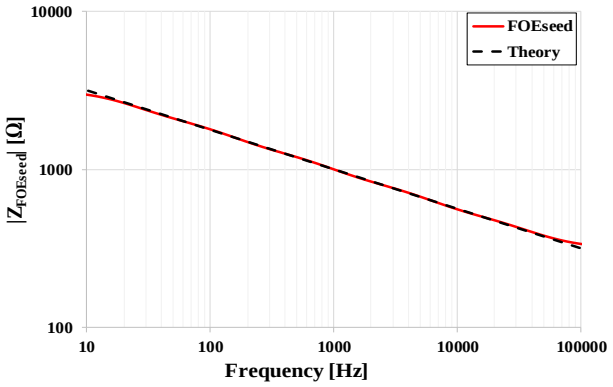
Fig. 6 5th-order Foster-II RC network used to approximate "seed" FOE

Table 2 Values of resistors and capacitors in Foster-II topology according to Fig. 6; $C_{\alpha\mathrm{seed}} = 112.3\ \mu\mathrm{F/s}^{0.75}$, $\alpha_{\mathrm{seed}} = 0.25$.

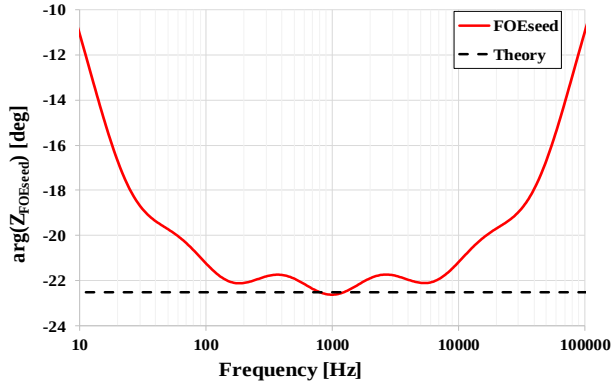
R_0 [kΩ]	3.16	C_1 [nF]	4.00
R_1 [kΩ]	0.79	C_2 [nF]	14.2
R_2 [kΩ]	1.41	C_3 [nF]	55.6
R_3 [kΩ]	2.28	C_4 [nF]	219
R_4 [kΩ]	3.65	C_5 [nF]	814
R_5 [kΩ]	6.19		

The properties of the approximated "seed" FOE can be determined from Fig. 7 showing the magnitude $|Z_{\mathrm{FOEseed}}|$ and the phase shift $\arg(Z_{\mathrm{FOEseed}})$ by red color, whereas the theoretical values (based on (1)) are shown by black

dashed lines. The absolute errors of the impedance magnitude and phase of the approximated "seed" FOE from the theoretical values are depicted in Fig. 8.



(a)



(b)

Fig. 7 (a) magnitude and (b) phase shift of the "seed" FOE from Fig. 6

The resulting magnitude and phase frequency characteristics of the input impedance of the immittance inverter/converter (Fig. 3) are presented in Fig. 9. The individual curves correspond to the resulting FOE variants summarized in Table 1. The approximated "seed" FOE with $\alpha_{\mathrm{seed}} = 0.25$ described above along with the resistors ($\alpha = 0$, $R = 1$ kΩ) and capacitors ($\alpha = 1$, $C = 159.2$ nF, i.e. $|Z_{\mathrm{C}}| = 1$ kΩ at frequency 1 kHz) are used to substitute the admittances Y_1 to Y_4 in the default circuit from Fig. 3 in accordance with Table 1. The transconductances g_{m1} to g_{m7} were set to be 1 mS.

The ideal results (black dashed curves) in Fig. 9 were obtained using ideal elements in Fig. 3 and "seed" FOEs emulated with the Foster-II structure in

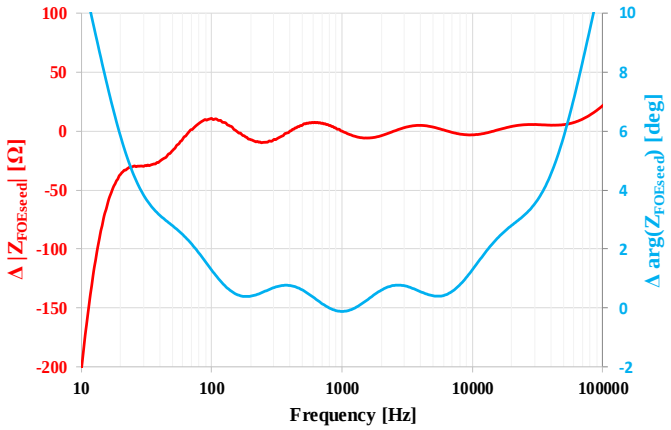
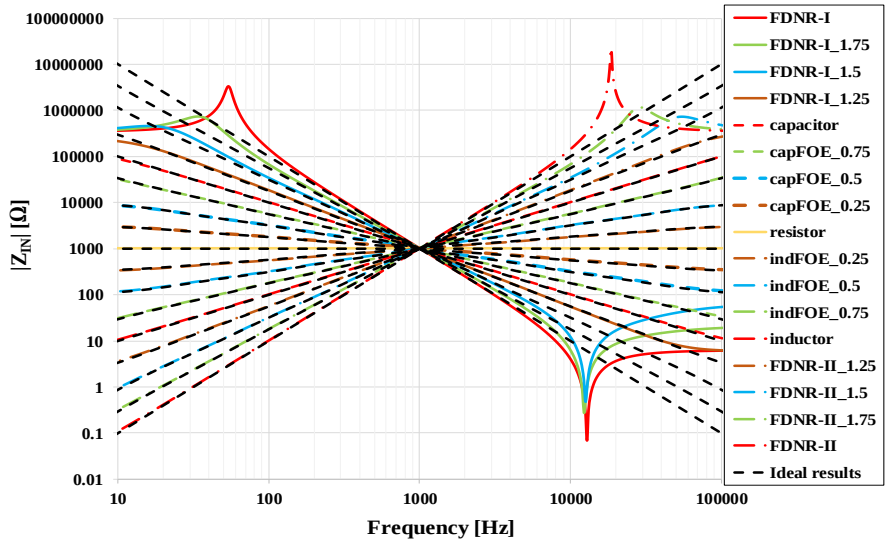


Fig. 8 Absolute error in magnitude (red line) and phase (blue line) of the approximated "seed" FOE

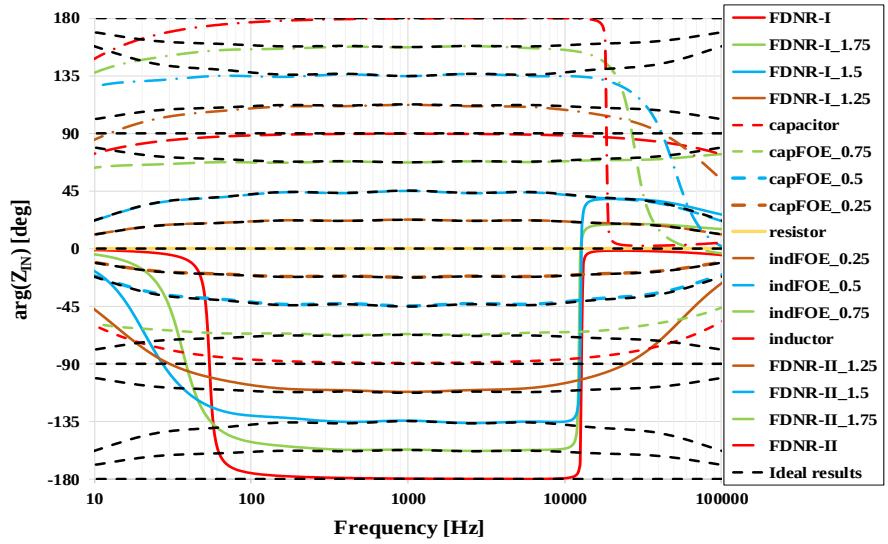
Fig. 6. The deviations of the simulated characteristics (color curves) in Fig. 9 from the ideal results are most apparent outside the frequency range 100 Hz 10 kHz. These errors in phase are shown in Fig. 10. It can be observed that the error is higher for the cases with higher absolute values of the resulting α. The impedance deviations are caused by non-ideal behavior of OTA elements whereas the internal output impedance of OTAs most significantly effects the overall performance of the immittance inverter/converter. The utilized OTA element adopted from [21] exhibits real part of the output impedance approximately 360 kΩ which also limits the maximum value of the impedance magnitude of the nodes at the OTA outputs. Consequently also the dynamic range of the overall input impedance magnitude is limited as apparent in Fig. 9 (a).

Additionally, the resonance in Fig. 9 being observed for the FDNR-I and FDNR-II cases with higher absolute value of α is caused by non-zero parasitic conductances of OTA terminals in the GIC structure (note that an ideal OTA shows zero input and output admittance). The resonances of FDNR-I at low frequency and of FDNR-II at high frequency arise due to the parasitic conductance of the overall input of the GIC where the main contribution has the internal conductance of OTA_7 output. On the other hand, the resonance of FDNR-I at high frequency is caused by the parasitic conductance of the GIC internal node where the outputs of OTA_1 and OTA_6 are connected and their parasitic conductances are present. All these resonances are damped by the inherent parasitic capacitances of the respective nodes which prevent the GIC from unstable behavior. To ensure higher damping, the node capacitances can be intentionally increased which results also in soft GIC input impedance phase transition around the resonant frequency and reduction of frequency range.

In Fig. 10 the absolute error in phase is shown. It is evident that the final accuracy of the FOE at the input of the GIC is primarily determined by



(a)



(b)

Fig. 9 (a) magnitude and (b) phase shift of the proposed immittance inverter/converter from Fig. 3

the accuracy of the "seed" FOE and count of "seed" FOEs to implement the required α. The error increases primary for solutions, where two "seed" FOEs

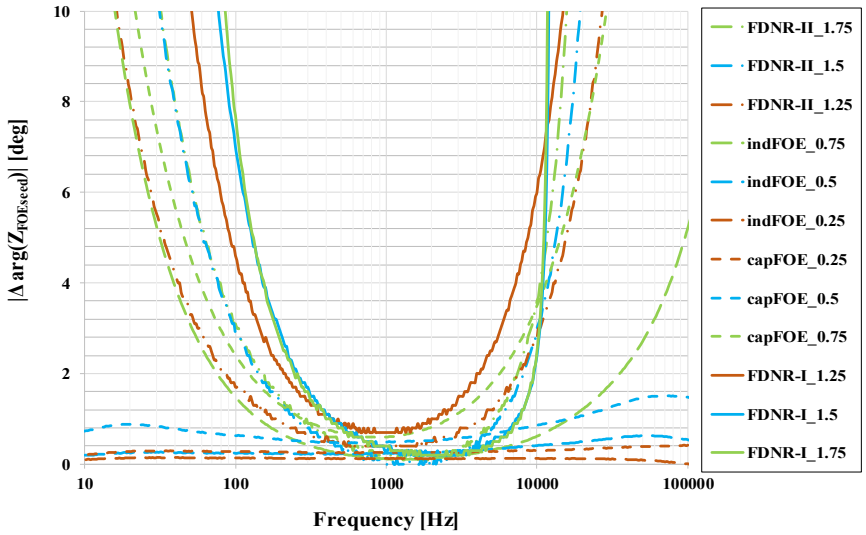


Fig. 10 Absolute error in phase of the proposed immittance inverter/converter with "seed" FOEs.

are used to replace the general admittances Y_1, Y_2, Y_3, and/or Y_4. Hence, if higher accuracy is required, the accuracy of the "seed" FOE must be increased, primarily increasing the order of the RC network (Fig. 6).

5.3 Utilization of synthesized FOEs in filter design

Here, as an example we show the practical utilization of a new FOE obtained at the input of the proposed GIC on fractional-order low-pass filter from Fig. 11.

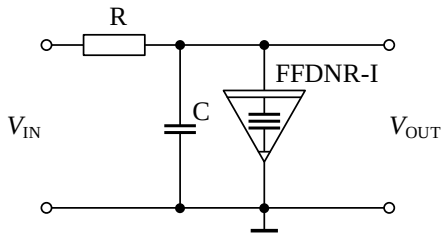


Fig. 11 Passive low-pass filter using fractional FDNR-I (FFDNR-I).

Assuming that for fractional FDNR-I (FFDNR-I) the fractional order α is in the range of $[1, 2]$, the transfer function of the filter from Fig. 11 can be

determined as:

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{a}{s^{\alpha} + s^{\alpha-1}b + a}, \tag{12}$$

where $a = 1/(RF)$ and $b = C/F$, whereas F is the fractance of the fractional FDNR-I.

Selecting the FFDNR-I with its fractional order $\alpha = 1.75$ as it was obtained in sec. 5.2, its fractance is $F = 225.5$ pFs$^{0.75}$. From Fig. 9, proper operation frequency band is approx. 100 Hz to 10 kHz. Hence, following the fractional frequency filter design recommendations as they were presented in [15], the cut-off frequency of the filter is set to 100 Hz to maintain the fractional slope in the stop-band of the filter in wider frequency range.

Coefficients a and b of the transfer function (12) are found for Butterworth response by the method as decribed in [7] for fractional order 1.75 and frequency-scaled to obtain the filter cut-off frequency ω_0:

$$a = \omega_0^{\alpha}\left[-0.0992(\alpha-1)^2 + 0.0989(\alpha-1) + 1.004\right], \tag{13}$$

$$b = \omega_0^{\alpha-1}\left[-0.4838(\alpha-1)^2 + 2.023(\alpha-1) + 0.0104\right]. \tag{14}$$

Assuming $f_0 = 100$ Hz, according to (13) and (14) the transfer function coefficients are $a = 80616.7$ and $b = 157.564$, and the transfer function (12) turns to:

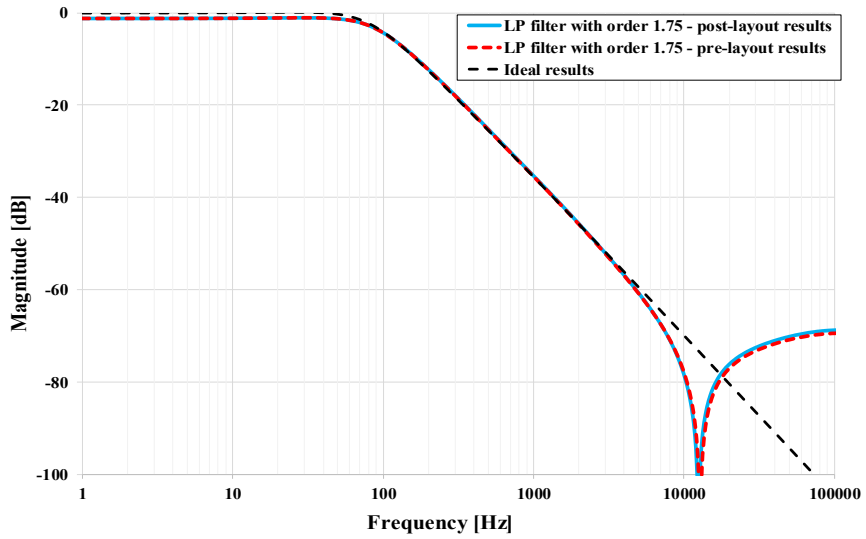
$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{80616.7}{s^{1.75} + 157.564s^{0.75} + 80616.7}, \tag{15}$$

whereas, the values of the resistor and capacitor from Fig. 11 are then determined to be $R = 55$ kΩ and $C = 35.5$ nF, respectively.

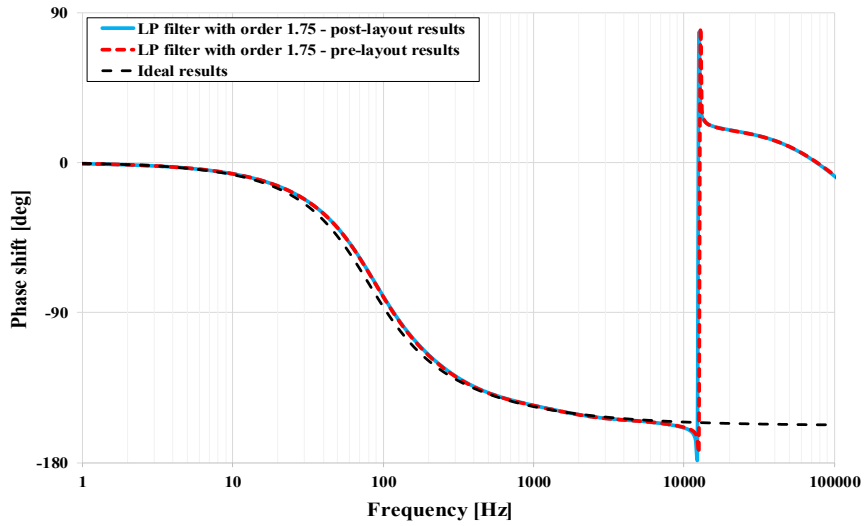
The magnitude and phase frequency responses of the low-pass filter reached by simulations are presented in Fig. 12. Here, both the pre- and post-layout simulations of the designed filter are shown by dashed red and solid blue curves, and compared to ideal magnitude and phase response determined by (15), shown as dashed black. Both from magnitude and phase response of the filter only a slight difference between the pre- and post-layout simulations is observed, which basically proves proper design not only of the proposed GIC, but also of the initial OTA cell as it was described in [21]. From the simulations results follow the ideal plot up to frequency approx. 12 kHz, where a parasitic zero is present and is caused by the parasitics of the GIC as deviation at the same frequency could already be observed in simulation results in Fig. 9 showing the magnitude and phase shift of the input impedance of the GIC.

6 Conclusion

In this paper, we proposed a concept of efficient design of a series in fractional order α of fractional-order elements (FOEs) utilizing a limited number of initial FOEs, here referred to as "seed" FOEs. The proposed concept is further verified by designing an immittance inverter/converter suitable for obtaining a series of α spanning the range $[-2, 2]$. It was shown that using a



(a)



(b)

Fig. 12 Simulation results of fractional low-pass filter from Fig. 11: (a) magnitude and (b) phase response.

tuned "seed" capacitive FOE with the fractional order $\alpha_{\text{seed}} = 0.25$, a series of 17 FOEs that differ in their final fractional order α can be obtained. Next

to obtaining different values of fractional orders, another advantage of using immittance inverter/converter is the possibility to adjust the absolute value of the impedance at specific frequency, that is the pseudo-capacitance C_α once speaking about capacitive FOE. The presented post-layout simulations further prove the operability of the proposed concept in efficient design of fractional-order elements. Additionally, as practical example, selecting the implemented fractional FDNR-I it was used to design a fractional low-pass filter.

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Conflict of interest

The authors declare that they have no conflict of interest.

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