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COMPARISON AND OPTIMIZATION OF DC/DC POWER CONVERSION TOPOLOGIES USING GAN FET TECHNOLOGY FOR HIGH EFFICIENCY AND POWER DENSITY POWER CONVERTERS

SROVNÁNÍ A OPTIMALIZACE TOPOLOGIÍ PRO DC/DC KONVERZI ENERGIE S POUŽITÍM TECHNOLOGIE GAN FET PRO MĚNIČE S VYSOKOU ÚČINNOSTÍ A OBJEMOVOU HUSTOTOU VÝKONU

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Abstract

Focus of this thesis is the analysis of the current state of GaN semiconductor technology in power electronics and its application on DC/DC converter, optimized for high efficiency and high power density with the intention to use it in server and telecom applications.

The theoretical part analyzes problems and challenges related to novel GaN technology, such as gate driving for various internal structures, layout optimization for cooling of minimized surface mount packages without constraining parasitic elements affecting switching performance. Precise losses calculation for totem-pole power factor correction converter using novel GaN technology is included. Results and ideas resulting from theoretical analysis of various problems are applied in the design of prototype and verified by series of measurements, proving the benefits of novel technology and its potential to impact power electronics applications around us. Deep description of current measurement technique with high bandwidth, control loop operation and its implementation in digital signal processor is included.

Keywords

Gallium Nitride semiconductors, Cooling of minimized surface mount devices, Novel R_{DSon} Measurement method, Dynamic R_{DSon}, High Efficiency GaN half bridge, GaN Totem Pole converter

CONTENT

1 INTRODUCTION

After years of evolution and domination on the power electronics market, the Silicon semiconductors are reaching their physical limit, which opens space for the new technologies. In the last few years, amount of available GaN switching devices for power electronic applications has significantly increased. The number of emerging devices with a different internal structure has a growing tendency. Devices are offered not only by small/startup companies but also by well-known manufacturers of semiconductors (Infineon, Panasonic). The higher bandgap of Gallium Nitride (3.4eV) material offers potentially higher operating temperatures, fast switching capability and therefore generates less power loss than widely used Silicon or SiC devices.

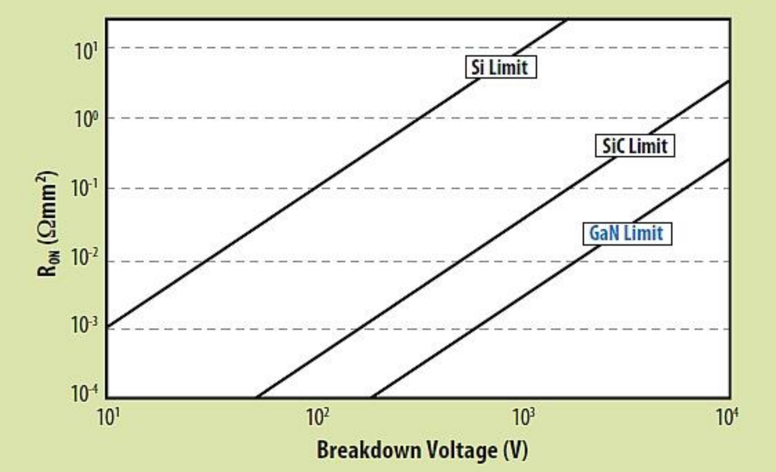

Fig. 1: Theoretical limits of Si, SiC and GaN material, [7]

GaN Transistors are well-known from low voltage, high frequency (MHz, GHz Range) applications (RF amplifiers in cell phones, consumer electronics, and many more). Improved manufacturing technology allows to use GaN in power electronics, which sets a brand-new benchmark in power converters´ parameters. Nowadays markets provide relatively narrow portfolio of GaN devices with 600V rating focused on power supply applications (consumer electronics, server and telecom applications…). First transistors with 1200V rating exist too, which makes them usable in electric drives and automotive applications. General requirements on power conversion systems are moving to smaller, higher dense solutions (60-100W/inch^3) to reduce the overall size of the system and cost of the power supply.

In following chapters the structure and parameters of currently available GaN transistor part numbers will be described. As the manufacturers are choosing different way how to proceed in the development of new devices in terms of internal semiconductor structure, closer look will be taken onto analysis of those structures with intention to compare.

MOSFET Gate driving principles are well known in power electronics. With new absolute maximum ratings for Gallium Nitride semiconductors, new challenges and possibilities are being introduced into design. This thesis aims to analyze and name these problems, with intention to propose solutions applicable to power converters design for various applications with GaN.

Roadmap in packages development is leading into size minimized packages, designed for surface mount technology. This style of packaging fixes problem with gate driving and improves switching performance of the device, on the other hand makes cooling design of the power chip challenging. Finite element method simulations together with measurement on prototypes of printed circuit boards designed for high performance cooling of small packages, which give a reference for industrial designs, are included.

Introduction of innovative devices, with brand new production technology and semiconductor structure should have different qualification process, comparing to settled Silicon MOSFETs used nowadays. The reason is simple, new phenomena might be present and might affect device performance in different operating conditions, which are not included in qualification process for semiconductors nowadays. This might affect long term reliability, which poses a high risk for pioneers introducing new technology into their commercial products. One of these phenomena is dynamic on-channel resistance, varying with time and various conditions. Analysis of this particular problem and collection of results measured on existing, commercially available samples, is one of base topics of this thesis.

Main result of this thesis is supposed to be the application of gained knowledge into prototype of DC/DC converter using Gallium Nitride devices, optimized for high efficiency and high-power density. This converter is operated as power factor correction in totem pole configuration with output power 3kW at output voltage 400V. Results show real benefits of this new technology, with immediate introduction into industrial application possible.

Study and analysis of certain topics related to GaN in this thesis, resulted in potential application of integrated circuit used primarily for this technology in different field. Penultimate chapter shows example of recuperative gate driver for silicon MOSFETs in synchronous rectifier for high efficiency resonant converter. This shows, that using novel/high-speed integrated circuit originally designed for GaN transistors, might bring significant improvements in various electronic problem categories.

1 PRESENT GAN TECHNOLOGY OVERVIEW

Nearly every manufacturer on the market is presenting his own GaN technology, with a different internal structure on a semiconductor level and with different performance. Internal structures of the transistors promoted for a usage in power electronics are - Cascode (Transphorm, VisIC), Enhanced mode (GaN systems, EPC) and Gate insulated transistors (Panasonic, Infineon). Different internal structures have different levels of complexity of the chip and different driving requirements. As per documentation of the aforementioned manufacturers, it is clear, that current common production technology is creating GaN structures on a silicon wafer. This technology is borrowed from manufacturers of optoelectronic components (LED, low wavelength lasers), where it has a long tradition and provides a good start point for GaN development. In this sector, two major companies (Veeco U.S., Aixtron Germany) are well known, providing automated solutions for manufacturing of GaN on Si structures.

1.1 D-MODE GAN

The basic GaN HFET (Heterostructure Field Effect Transistors) functional structure is grown on the silicon substrate with thin layer of Aluminum Nitride (Fig. 2), in some sources this type of transistor is also called depletion or d-mode transistor. As in every power Field Effect Transistor, there are Gate, Source and Drain contacts. Due the Gate electrode placed on the top of the AlGaN, we need to apply negative voltage bias on Gate-Source to turn the device OFF. This is caused by Schottky contact on the top of the surface, which becomes reverse biased by negative voltage and the electrons underneath are depleted. This device is “normally ON”.

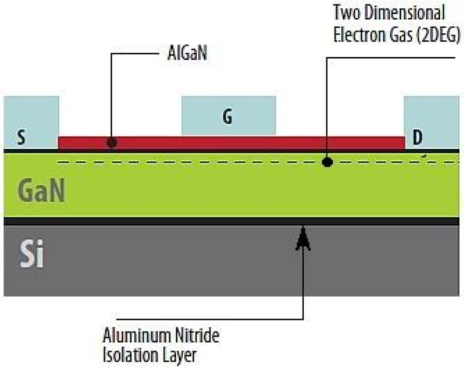

Fig. 2: Depletion mode GaN transistor structure, [7]

In power conversion applications this device obviously could not be used. The negative bias voltage on Gate-Source contact must be present before the power bus voltage. This may be hard to achieve in many applications and can result in driver circuit complexity, which affects the system reliability. To make GaN transistor useful in real application, manufacturers were forced to deal with the mentioned problem by developing new structures while maintaining the performance.

1.2 E-MODE GAN

GaN Systems, EPC works with enhancement mode field effect transistor (FET) structure. Basic enhanced mode manufacturing process starts with silicon wafers with thin aluminum layer (AlN) growth on it. This thin layer allows the growth of gallium nitride heterostructures (AlGaN) and creation of the whole transistor structure. The result is the structure shown on picture below, which is similar to silicon metal oxide semiconductor FET (MOSFET) with some exceptions. To enhance this FET, positive voltage must be applied between Gate and Source contact, same as in standard power MOSFET transistor.

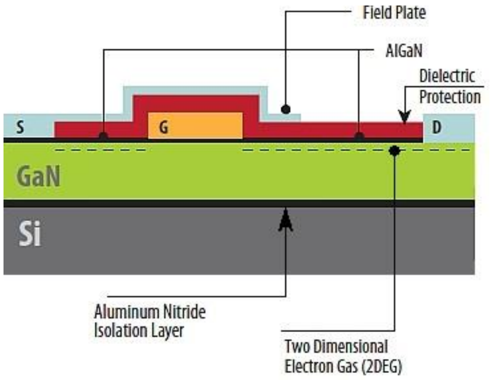

Fig. 3: Enhanced mode GaN transistor structure, [7]

With voltage present on the gate electrode, device can operate in two quadrants (forward and reverse current), with voltage drop equivalent to product of channel resistance in open state and drain-source current. Important difference between Si MOSFET and the GaN is the absence of natural body diode, which was causing serious problem with its reverse recovery charge in hard-switched topologies and increasing switching losses.

1.3 GAN CASCODE

Transphorm, ON Semi, VisIC are developing the cascode GaN transistors. Cascode is combination of low voltage fast silicon transistor (typically N-MOSFET) with “normally ON” GaN transistor (d-mode) connected as in picture below.

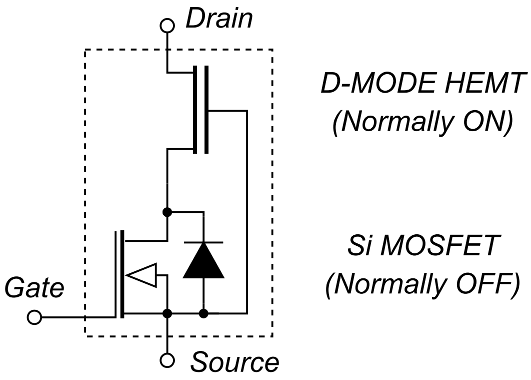

Fig. 4: GaN Cascode power transistor

Main benefit of the GaN cascode is the higher Gate-Source threshold voltage (3-4.5 V) – as the gate drive parameters are defined by silicon MOSFET in “bottom” part. Israel manufacturer VisIC is promoting GaN cascode with the best parameters at the time in terms of on-state resistance (22 mΩ), outstanding peak forward (180A) and reverse current capability in 650V class of transistors. This manufacturer also provides first GaN 1200V 40mΩ cascode transistor. Disadvantage of cascode devices is a need of two chips in one device (d-mode GaN and Silicon MOSFET), which can influence reliability and have negative price impact.

1.4 GATE INJECTION TRANSISTOR

GIT transistor promoted by Panasonic, Infineon is normally off transistor based on high electron mobility principle, similar as d-mode using two-dimensional electron gas forming at an AlGaN-GaN layer. The transistor is being produced in the same way as the other structures on silicon substrate, with a buffer layer to allow reliable creation of GaN structures.

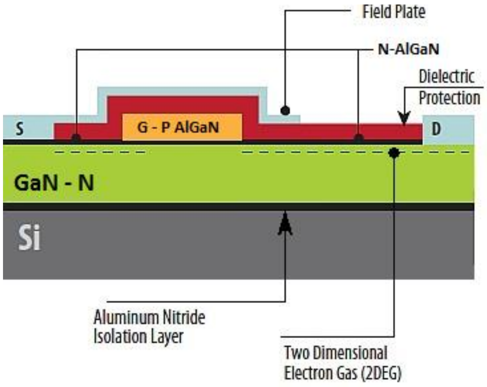

Fig. 5: Gate injection transistor structure, [7]

Same as e-mode transistor, GIT is forced to conducting state by increasing gate-source voltage above threshold voltage, typically around 1-1.3V. Major difference between e-mode and GIT is the on state behavior of Gate – while e-mode acts similarly to unipolar MOSFET transistor, GIT is above threshold voltage acting as a diode (P type Gate), therefore requires on state current (typically dozens of mA) which is defining the on state channel resistance of the Drain-Source. Thanks to the diode behavior in the on-state is gate electrode rugged (up to the current rating) against high dv/dt transients on drain-source. As transistor does not have a parasitic body diode, the current is flowing in reverse conduction mode through the channel – reverse drain-source voltage is dependent on gate-source voltage, minimum corresponding with the threshold voltage and increasing with a negative gate bias. The transistor therefore acts as a combination of bipolar transistor (in forward mode) and e-mode unipolar transistor (in reverse mode).

2 THESIS GOALS

1.) **Study of Gate driver requirements analysis of nowadays available GaN semiconductors**

With rise of novel technology, several different structures of Gallium Nitride power chip exist. While some of the parts are manufacturers developing based on combination of two independent chips in one package, others are investing effort into advanced single chip solutions, with different layout and production technologies. Different principle of operation means different parameters and requirements for driving and its application in power converter, which is a target of the analysis.

2.) **Design and optimization of innovative cooling solutions for minimized surface mount packages, used for novel GaN devices**

Voltage driving levels and fast switching performance of the GaN high electron mobility transistor are a motion for packaging style change, as large lead packages are no longer suitable and are limiting the performance of a chip. Goal of this chapter is to develop innovative solutions for cooling of minimized surface mount packages without constraints related to increased inductance of input terminals.

3.) **Characterization of dynamic R_{dson} problem related to certain production technologies**

Based on published articles of different authors, electron trapping under Gate contact of high electron mobility transistor exists. As this misbehavior might significantly affect performance of switch in final application, further analysis and characterization of this problem is crucial. Special experimental test setup is being built, and test results will be compared.

4.) **Application of gained sub-results in practical case of innovative DC/DC power converter and its optimization for high efficiency while maintaining high power density**

Multiple of partial improvements gained within this thesis are being verified in totem pole power factor correction converter. Detailed steps of optimization for high efficiency at certain operating conditions are explained, to comply with 80plus certification required by the European Union regulations for computer and server appliances. Goal of this section is to present gained results with all the improvements applied.

5.) **Application of novel GaN integrated circuits in various applications**

Evolution in production of Gallium Nitride based semiconductors results in development of novel integrated circuit, capable of parameters never seen before. This chapter shows application of integrated driving circuit in special application of recuperative Gate driver of high Current synchronous rectifier in resonant converter, resulting in US patent.

3 COOLING OF MINIMIZED SURFACE MOUNT PACKAGES

Reducing parasitic elements is leading to size minimized, surface mount packages. On the one hand improved switching performance helps to reduce power loss of the device, on the other hand it makes cooling of the device much more challenging. Comparing to standard lead packages (TO-220, TO-247), which were in most of the cases directly attached to the heatsink over insulating thermal interface. With minimized surface mount packages it is necessary to design more sophisticated structure, in special case as a part of the printed circuit board itself. If we take a look at the current portfolio of GaN devices available on the market, we can split it into two groups - TOP and BOTTOM cooled surface mount packages.

3.1 TOP SIDE COOLING

For a package where a cooling plate is located on the top side (opposite to soldering pads), the heatsink is a part of the PCB assembly, or the opposite way, the PCB is mounted to the heatsink. Problem seems too obvious and easy to resolve. But, for long term reliability in certain pollution degree (2-3) it must be taken into account, that for high voltage (typical bus voltage 400V DC) the creepage and clearance distance defined by IPC9595 are relatively high (>3mm), comparing to device size itself. This distance must be maintained between all electrical poles, mechanical fixings of the heatsink to the PCB tracks and connectors.

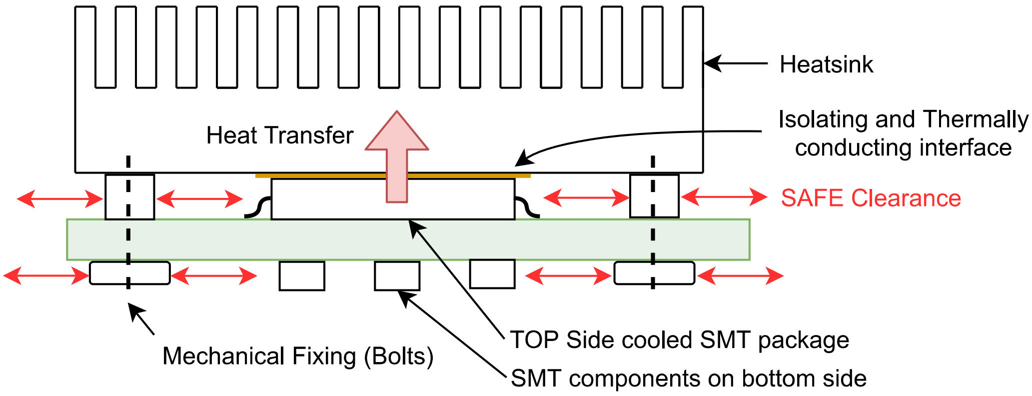

Fig. 6: Top side cooling mechanical construction

VisIC company producing GaN Cascodes is promoting very special hybrid package, most probably with military background, which has insulated cooling pad from other contacts of the device (part number V22TC65S1A). Manufacturer claims that part provides basic isolation up to 2.5kV which might bring significant benefits for Top cooling approach. Disadvantage is a package height (approx. 3mm), which is not compliant with IPC9592 recommended distances for advertised isolation voltage level.

3.2 BOTTOM SIDE COOLING

Second group of devices is manufactured with bottom side cooling pad, on the same side as electrical connection. Heat transfer is performed over PCB to the heatsink attached over thermal interface/foil on opposite side of the device. Mechanical interface is in this case not needed, PCB is assembled in simple single sided SMT assembly process and afterwards assembled over sticky/insulating interface to the heatsink. Bottom side solution is possible, in case the thermal resistance over the PCB thickness is minimized to acceptable value – power loss of the cooled device will create temperature rise, which together with temperature of the heatsink (ambient temperature) have to stay below maximum ratings of the chip.

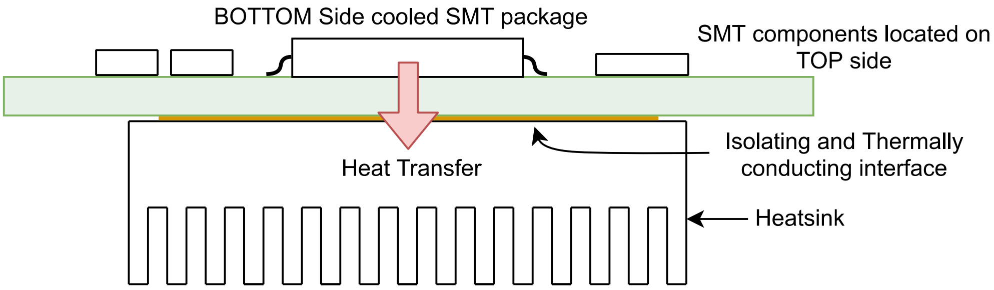

Fig. 7: Bottom side cooling mechanical construction

Heat transfer over PCB can be done over base/core material and over tracks and vias – copper part. In case of standard printed circuit board made from FR4 the core contribution to cooling is very low (0,35Wm^{-1}K^{-1}). On the opposite side is the ceramic material base - Aluminium Nitride ceramic (140Wm^{-1}K^{-1}), which has other disadvantages as brittleness, cost and only single layer PCB is supported by manufacturers. In following lines, several bottom side cooling solutions will be presented, using different printed circuit board manufacturing techniques with their performance evaluation.

3.3 PCB WITH COPPER INLAYS

Using standard core material FR4 should be the target for all designs, as the technology of PCB manufacturing on fiberglass is well developed and cost effective. Therefore, we are looking for a way how to create area of higher thermal conductivity from top side of the PCB to the bottom, to the isolating thermal interface/heatsink. These requirements are well fulfilled by Copper inlay technology - which is a copper element protruded over pre-milled opening in standard, several layer PCB. This design style is ideal for carrying high currents over PCB, seen in automotive applications nowadays, but ideally fits for this case, as the copper is a good heat conductor (400Wm^{-1}K^{-1}).

Before proceeding to prototype phase and testing, solution is to be verified by Finite Element Method simulation in ANSYS ICEPAK. In simulated case the cooled surface mount device is directly soldered to the copper inlay and the heat is transferred through the foil (Arlon Secure 1500KT2) to the heatsink over copper block. Power losses assigned to the four devices are 20W, assuming two transistors in parallel in a half bridge application (5W for every transistor chip). Ambient temperature is 25 °C, overall temperature increase is 23 °C – including isolation between heatsink and device thermal resistance between chip and case.

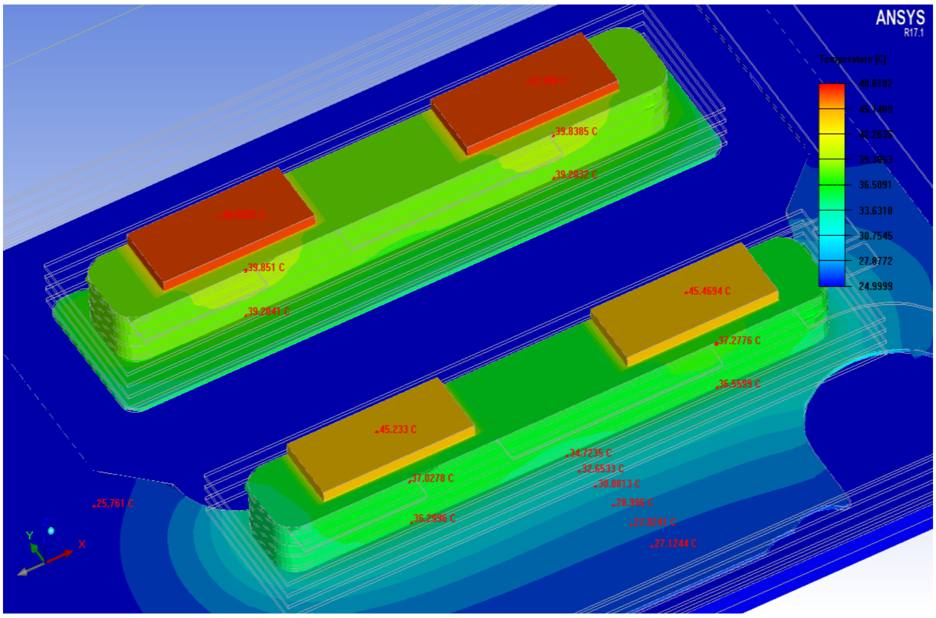

Fig. 8: Copper inlay thermal simulation

Overall Δϑ from surface of printed circuit board to the heatsink temperature is 12.3°C – thermal resistance is calculated with power 10W is $R_\vartheta = 1.23\ KW^{-1}$. Majority of the temperature increase is on the thermal insulating foil, while PCB is bridged with temperature difference 5.4°C ($R_{\vartheta PCB} = 0.54\ KW^{-1}$). This result shows major disadvantage - high tech PCB technology used, but overall performance is lost on high voltage insulating layer. Prototype using copper inlay technology was produced, and results were evaluated (Fig. 11). Simulated case and tested prototype are representing primary power stage of 3kW resonant converter (LLC).

3.4 PCB WITH THERMAL VIAS

Alternate solution to copper inlays is the PCB with high amount of vias, with an intention to transfer heat efficiently to the heatsink. Design and effectivity of this solutions are hardly dependent on printed circuit board manufacturer capabilities – especially maximum hole/via plating thickness (Fig. 9 - c), distance between drilled holes (Fig. 9 - k) and the hole diameter itself (Fig. 9 - D). Considering dimensions displayed in the drawing below (Fig. 9) - for lowest thermal resistance of the PCB in Z direction, highest area of copper should be achieved. Triangular organization of vias is using manufacturing capabilities in the most effective way.

Comparing to frequently seen square pattern [18][26], brings triangular pattern 15.5% more copper vs. area ratio, which is directly reflected in performance. By comparing area of the "useful" copper transferring heat to the total PCB area, following formula can be constructed (1). Derivation (=0) of this equation shows the optimum for a defined via plating thickness and drilled hole distance, which is feasible by standard manufacturing process.

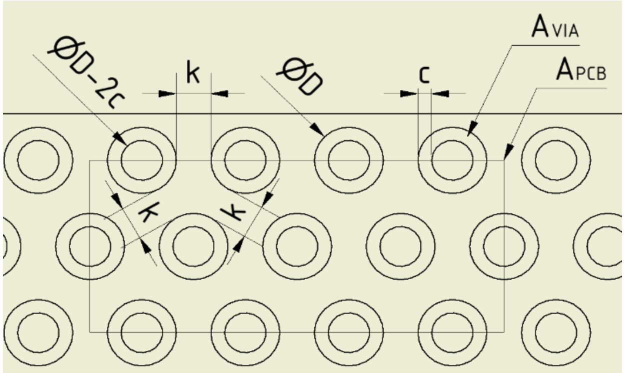

Fig. 9: Copper fill factor

Ratio between the area of thermal conducting copper versus total PCB area:

$$\frac{A_{Cu}}{A_{PCB}} = \frac{8\ x\ A_{VIA}}{A_{PCB}} = \frac{2.\pi.(D.c - c^2)}{\sqrt{3}.(D + k)^2} \tag{1}$$

If the thickness of the top layer is sufficient (>50µm) and parameter k is in optimal range, the thermal resistance of across PCB can be calculated using following formula:

$$R_{\vartheta} = \frac{1}{\lambda_{Cu}}.\frac{l_Z}{N.\pi.(D.c - c^2)} \tag{2}$$

Where N is the total amount of vias in cooled area, l_z is the overall PCB thickness. Same as for copper inlays, development started with thermal simulation of solution in ICEPAK. Simulation of model requires significant amount of mesh elements and computation power. Certain simplification had to be taken to make simulation possible – vias as a "barrel shape" were replaced by simple hexagons.

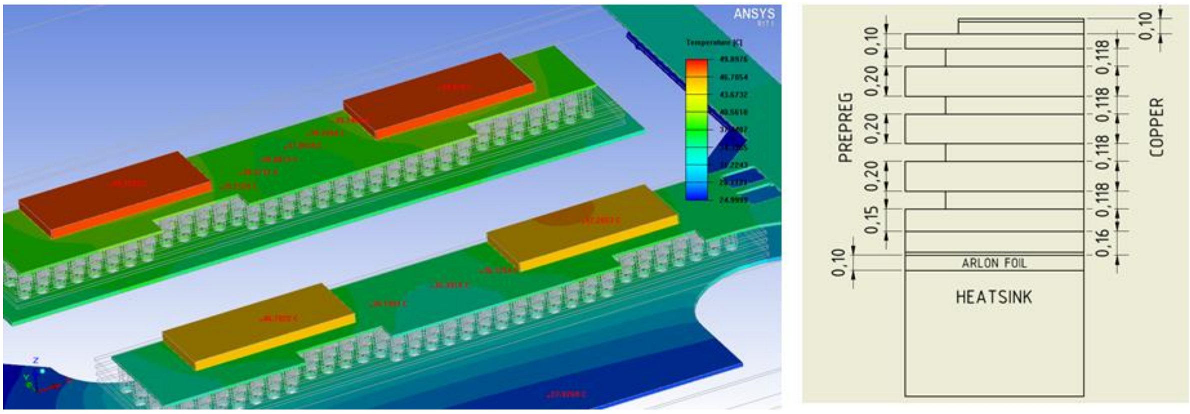

Fig. 10: Thermal Simulation of PCB variant B, k=0.25mm, D=0.5mm, c=100µm, PCB thickness= 1.5mm

Simulation of model B shows better results, and is preferred by the PCB manufacturers, heatsink temperature is 25.0°C and PCB surface temperature is 39.9 °C, resulting in thermal resistance from PCB surface to the heatsink side $R_{\vartheta FR4\text{-}VIASB} = 1.49\ KW^{-1}$. Temperature resistance on the PCB itself is based on cursors under chip and on opposite side is $R_{\vartheta PCB} = 0.87\ KW^{-1}$. Further improvement of thermal vias might be achieved by filling of the vias by thermal conductive material, but this a non-standard process which is not offered by many PCB production houses.

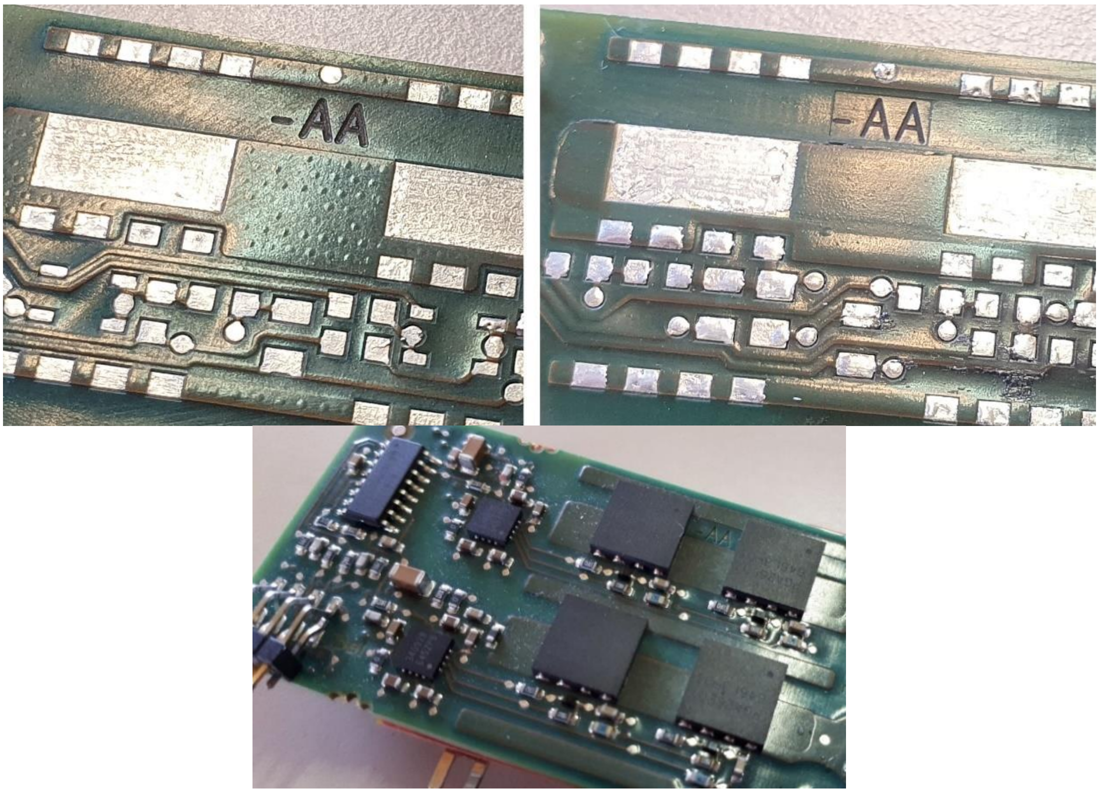

Fig. 11: Pictures of prototypes – printed circuit board with thermal vias technology (left), PCB with copper inlay (right) and assembled prototype

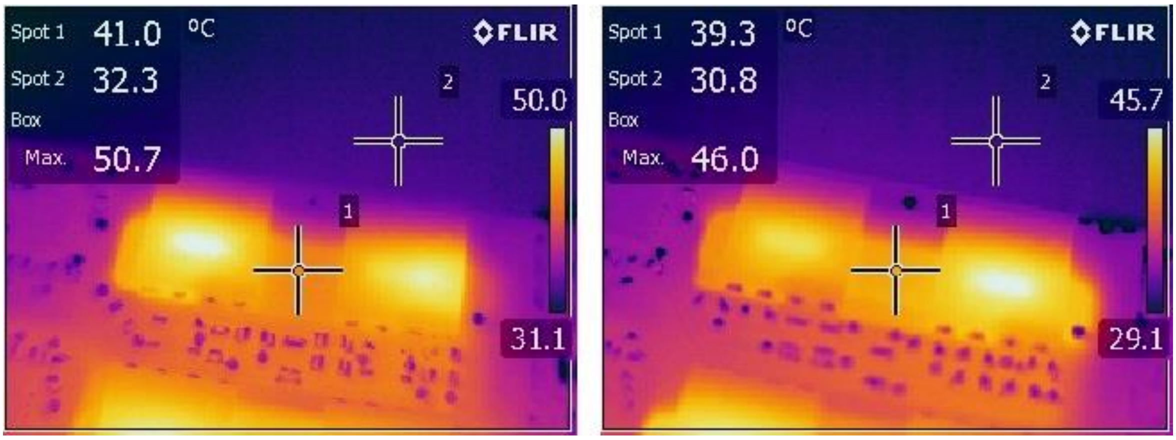

Fig. 12: Thermal camera picture of FR4 based PCB – copper inlay (right), optimized thermal vias (left). Power loss 5W/device, spot no.2 represents the heatsink temperature

3.5 IDEA OF PCB ON INSULATED METAL SUBSTRATE FOR POWER ELECTRONICS

For further performance improvement, temperature increase over electrically insulating interface between PCB and the heatsink needs to be reduced – by technology of printed circuit board on insulated metal substrate (IMS). Insulated metal substrate printed circuit board is produced the same way as board with FR4, by process of vacuum lamination, high voltage insulation is integrated “inside” the PCB and done by insulating layers. This technology is well adopted in automotive lighting application for the same purpose – cooling of surface mount devices.

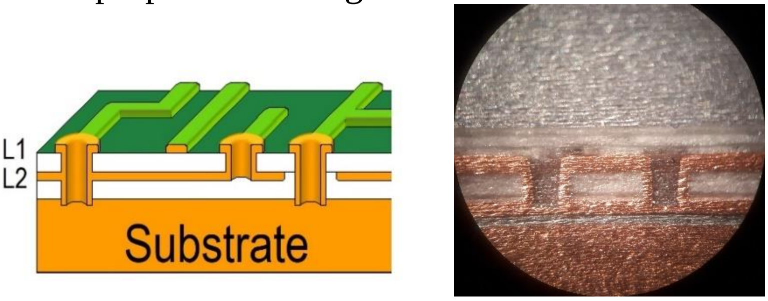

Fig. 13: Cross section of dual layer IMS board, suitable for power electronics application

From cooling point of view it is optimal to place driver and power semiconductor in surface mount package on a single layer IMS board. In such a case the heat travels only through one layer of high voltage insulating material, which can be thanks to novel ceramic-filled epoxy materials and production processes very thin, considering 400V operational voltage (typ. from 70-150µm). One of the suitable materials is named 92ML (ceramic-filled epoxy) and can provide thermal conductivity 1.6 WmK^{-1} in Z direction, which is ten times more than FR4. Routing proper low inductive layout for GaN gate driver and for power path is without doubts not possible on a single layer. Therefore, at least two-layer board should be used to achieve switching performance with minimized parasitic elements in the circuit.

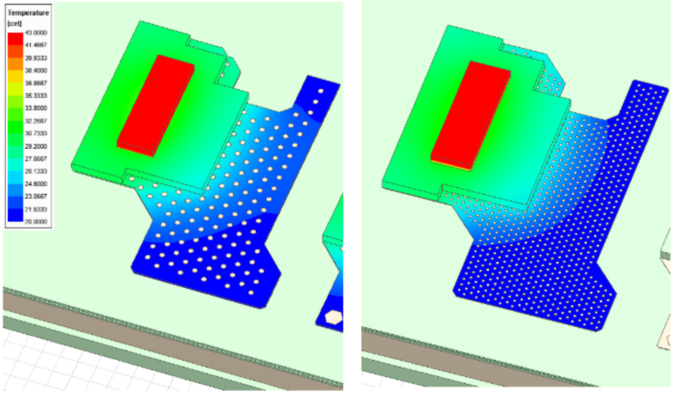

Fig. 14: Thermal simulation of Insulated Metal Substrate PCB

This solution has significant disadvantage, as the heat needs to travel through two layers, while layers in between need to provide high voltage insulation, the initial benefit of IMS is lost. By using thermal vias described in previous chapter is possible to “gain back” part of the performance of single layer solution, by bridging the intermediate insulating layer. Two different variants were simulated and tested.

Variant A – drilled vias with diameter D = 0.5mm with industrial standard plating c = 40um, distance between holes k = 0.25mm. Thickness of layers 150µm/150 µm (fill factor k_{vias} = 11.87%)

Variant B – high dense laser drilled D = 0.15mm copper filled micro-vias, distance between holes k = 0.2mm (k_{vias} = 16.66%). As the laser drill technology was used, the middle layer thickness needs to be reduced to avoid any defects in micro-vias plating. Therefore, the layer thickness is 100µm/150µm.

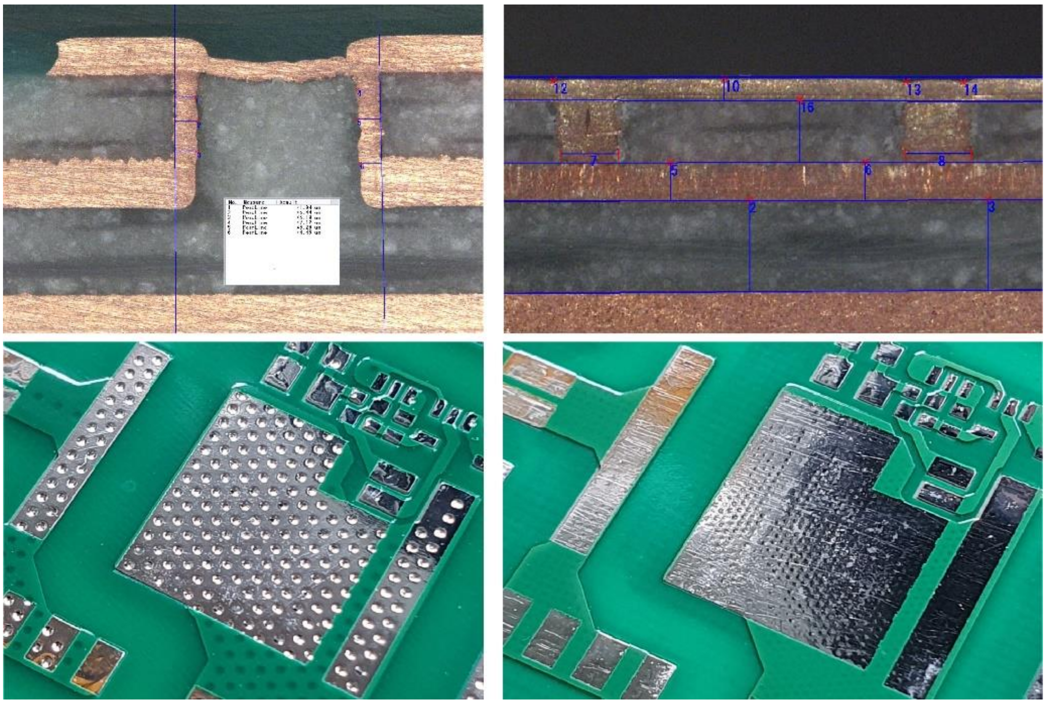

Fig. 15: Micro-section analysis and surface photos of tested prototypes - variant A (left), variant B (right)

Thermal camera pictures of variant A and B are shown in Fig. 16. MOSFETs are carrying current in reverse conduction mode – current and voltage drop on device is measured by calibrated multimeters - power loss is precisely set to 10W for both devices. Note that power assigned is the same as for thermal simulation created again in Ansys ICEPAK 2020 R1, with results visible in Fig. 14.

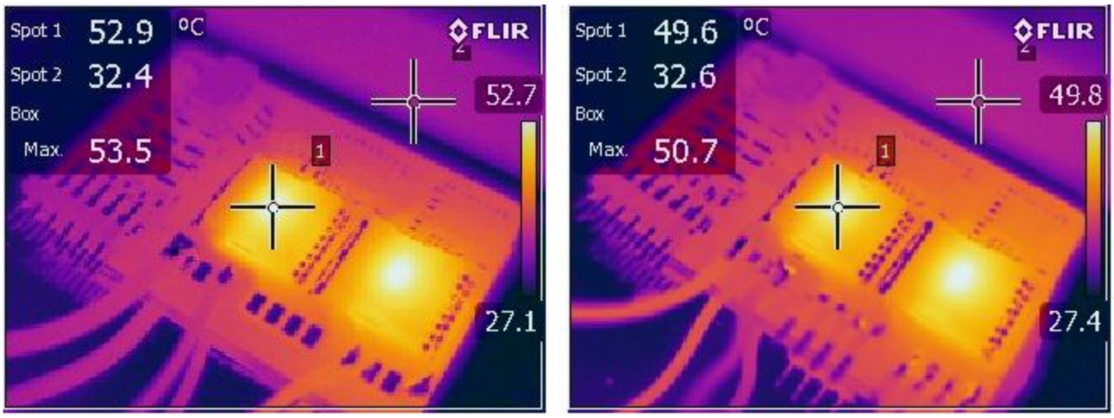

Fig. 16: Thermal camera picture of IMS PCB - variant A (left), variant B (right). Spot no.2 represents the heatsink temperature.

3.6 SUMMARY

Several configurations of printed circuit board for cooling of minimized surface mount packages in power electronics application were presented. Result of the development is presented by thermal simulation results and measurement on physical prototypes with various constructions.

The best results in terms of thermal resistance from PCB surface to the heatsink can be achieved by using insulated copper metal substrate technology. In addition, performance might be improved by using optimized thermal vias matrix down to outstanding $0{,}81KW^{-1}$. Presented examples contain insulated GaN gate driver, routed on two layers without any design constraints. Solutions based on multilayer FR4 PCB are suitable mainly for applications, where cost saving is the main decision factor.

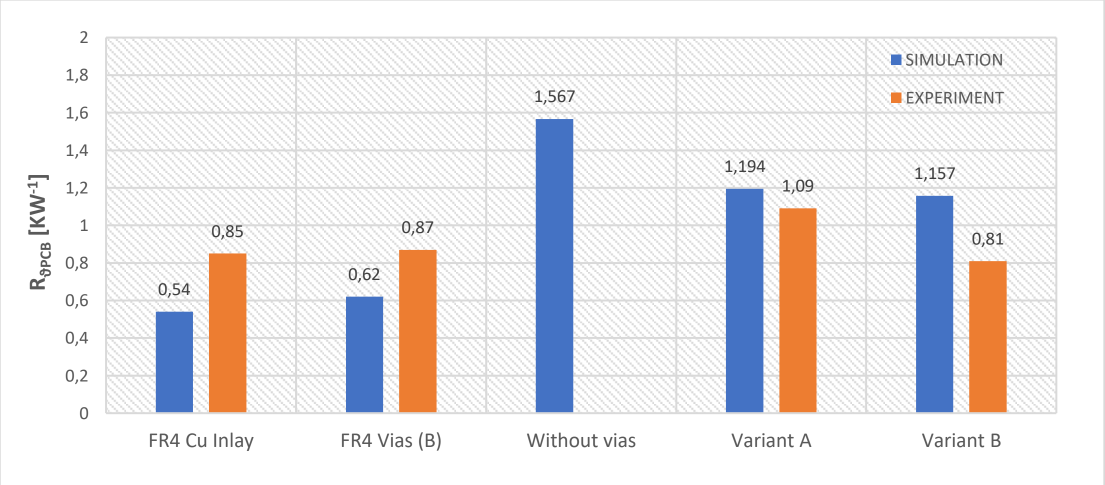

Fig. 17: Summary of the temperature rise on the PCB (w/o insulating foil) for all simulated and tested solutions

Chapter presents innovative solutions for cooling of minimized surface mount packages, used nowadays mainly for novel wide bandgap devices for power electronics using GaN and SiC material. Author believes that cooling is one of the major design constraints affecting lifetime of devices in the application and its resolution requires step to more advanced technology of printed circuit board comparing to what the industrial standard is nowadays.

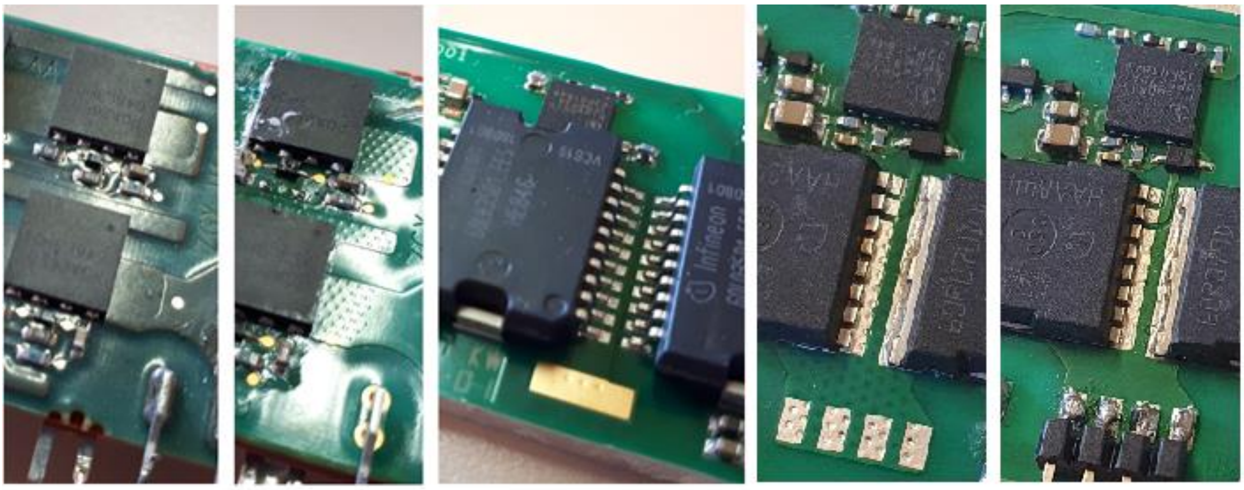

Fig. 18: Physical construction of simulated samples (Copper Inlay, Thermal Vias B, IMS)

4 DYNAMIC R_{DS-ON} OF GAN DEVICES

The power loss in a semiconductor switch can generally be divided in two parts - switching and conduction power loss:

$$\Delta P = \Delta P_{Sw.} + \Delta P_{Cond.} \tag{3}$$

The switching power loss $\Delta P_{Sw.}$ is defined by energy dissipated during switching event multiplied by switching frequency. The conduction loss $\Delta P_{cond.}$ is defined as a product of squared rms current and resistance in conductive state of semiconductor device. It is assumed that the switching loss is linearly increased with switching frequency and conduction loss is in many cases considered to stay constant – as the on-state resistance and the device rms current remains the same over the frequency. As shown further in this chapter, due to defects in the semiconductor structure, the on-state resistance of a device is not constant and should be considered nonlinear at higher switching frequencies.

4.1 THEORY OF MEASUREMENT

In order to obtain a plot of the on-state resistance during a device operation cycle in a power electronic circuit, the Ohm law is applied:

$$v_{DS(t)} / i_{DS(t)} = r_{DSon(t)} \tag{4}$$

The current through the device $i_{DS(t)}$ and the voltage over the drain source terminals $v_{DS(t)}$ are measured during the device switching operation. Let's consider following conditions for further analysis:

- a typical continuous conduction mode (CCM) operation
- the $v_{DS(t)}$ high voltage transition has settled before the $r_{DSon(t)}$ is measured
- inductor with a low inter-winding capacitance is used to connect the device switching node with the rest of the circuit

In this case we can consider the current through the device constant in a short time scale and the bandwidth of the current probe not critical. Therefore, a 50MHz BW current probe used in the inductor path is sufficient to emulate the device current. This allows to avoid the current sensor in the switching loop what is essential for a representative emulation of the normal device operation.

Sensing of the $v_{DS(t)}$ voltage is however a critical point. During device off time, the $v_{DS(t)}$ voltage reach a level of hundreds of volts while after a switch-on transient the $v_{DS(t)}$ quickly drops to few millivolts. Therefore, it is essential to use a $v_{DS(t)}$ sensing with a high dynamic range. When taking the speed requirements into account, the task is getting quite challenging.

An alternative option is to use a clamping circuit which protects the $v_{DS(t)}$ sensing device to saturate in off-state and enables the transfer of a signal in mV range to the sensing device in on-state conditions. Typically, a HV signal diode is used to clamp the $v_{DS(t)}$ voltage as shown in [3][4][16]. The common issue of this solution is the diode drop voltage which is not easy to characterize / calibrate when taking the very fast transient conditions the diode is exposed to into account.

To avoid issues mentioned above a novel clamping circuit was developed. The circuit features following advantages:

- Very low impedance clamping capability to block the high voltage propagation into the sensing device
- Effectively zero-voltage drop between the DUT and the $v_{DS(t)}$ sensor resulting in precise R_{DSon} evaluation
- A capability to measure $r_{DSon(t)}$ down to 70-100ns after the DUT switch on
- A high $r_{DSon(t)}$ sensing BW

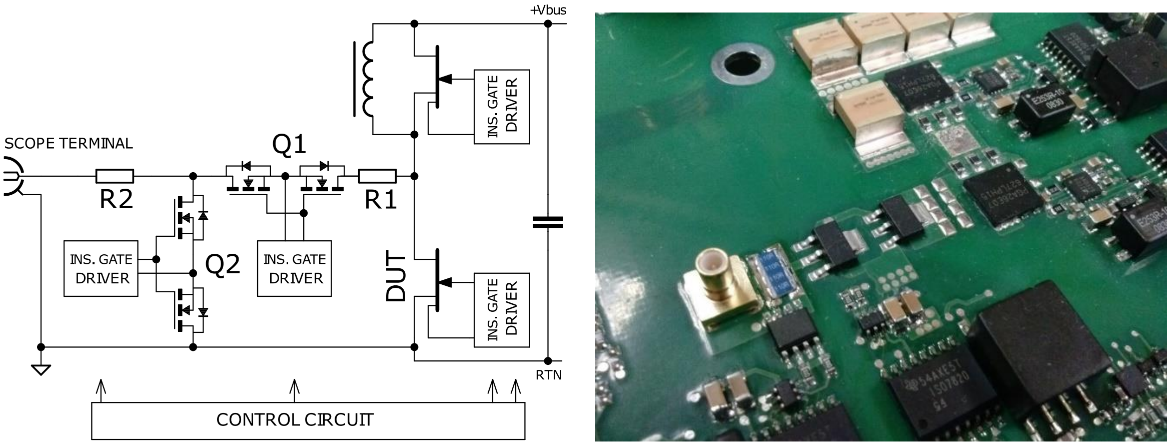

Fig. 19: Block diagram of dynamic R_{DSon} measurement setup

4.2 TEST RESULTS

Three samples of GaN transistors from three different manufacturers were tested. The test was conducted at 2 different bulk voltage levels. The test sequence consists of three switching cycles to increase the current through the choke to the test level.

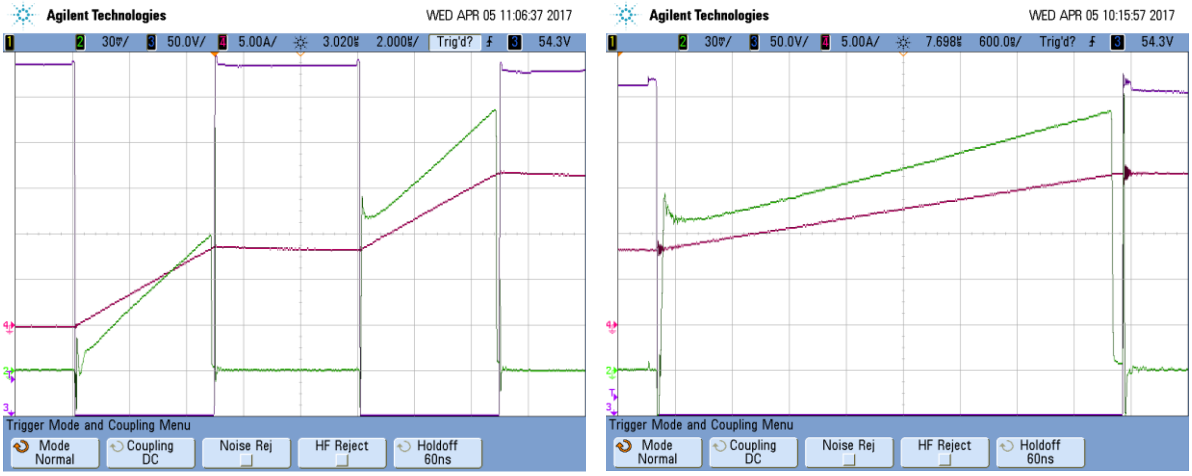

Fig. 20: Scope snapshot of GaN R_{DSon} tester operation

The voltage and current data acquisition is conducted during the last pulse sequence. The length of the pulse sequence, the peak current and the test voltage is for all samples the same. Consequently the $r_{DSon(t)}$ plot is constructed starting shortly (70-100ns) after DUT turn-on transient. Based on test results the following findings can be formulated.

Short transient increase

A short transient/dynamic on state resistance was detected for samples #1 and #3. This behavior is affected by the test voltage (e.g. voltage present on a DUT before the turn-on transient). The effect is more pronounced at high test voltage. Sample #2 however does not exhibit the short transient increase.

Long transient increase

A long transient increase is detected on sample #1 and #2, where the on-state resistance drops down to the static value over a long time (time range couple of *ms*). The only sample with no long transient increase is the sample #3.

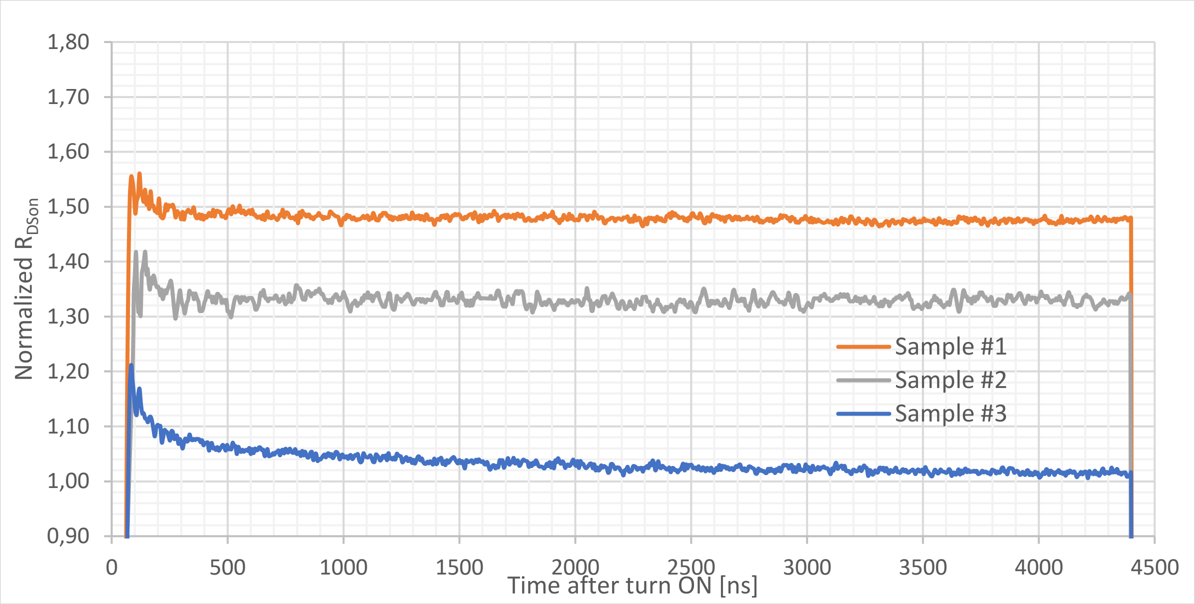

Fig. 21: Plot of normalized R_{DSon} vs. time after turn-on of three tested samples, bulk voltage 200V

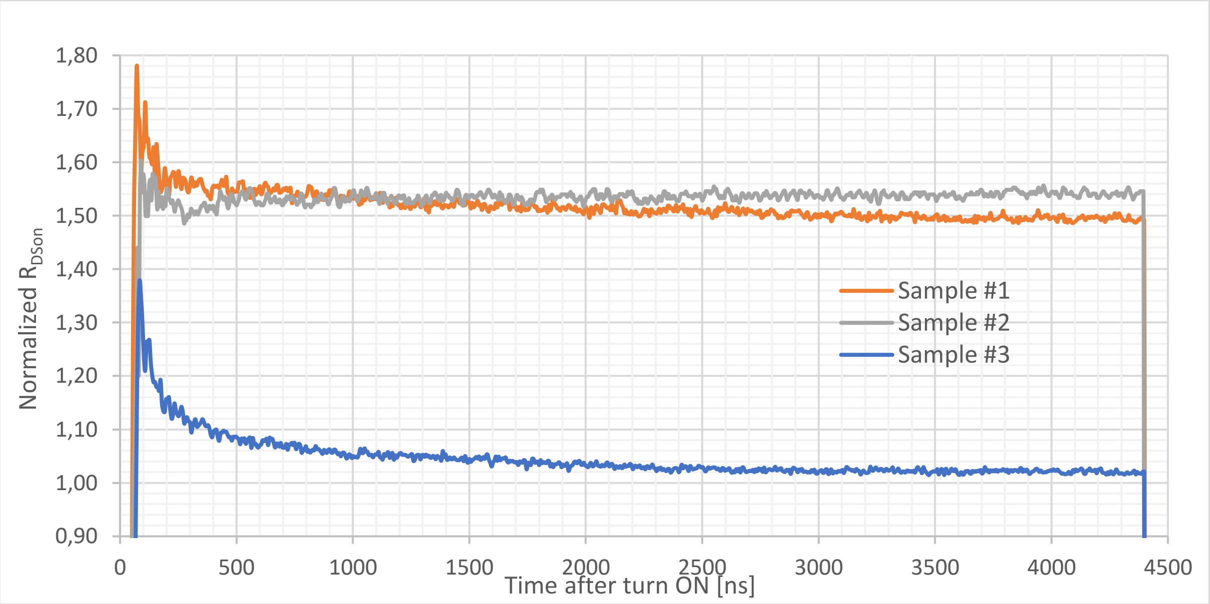

Fig. 22: Plot of normalized R_{DSon} vs. time after turn-on of three tested samples, bulk voltage 400V

Because all tested samples have a different internal structure, the mechanism of dynamic R_{DSon} is likely different. Root cause for the dynamic R_{DSon} is the electron trapping in crystal defects [14], however the test results indicate that each provider of the sample handles the electron trapping in a different way.

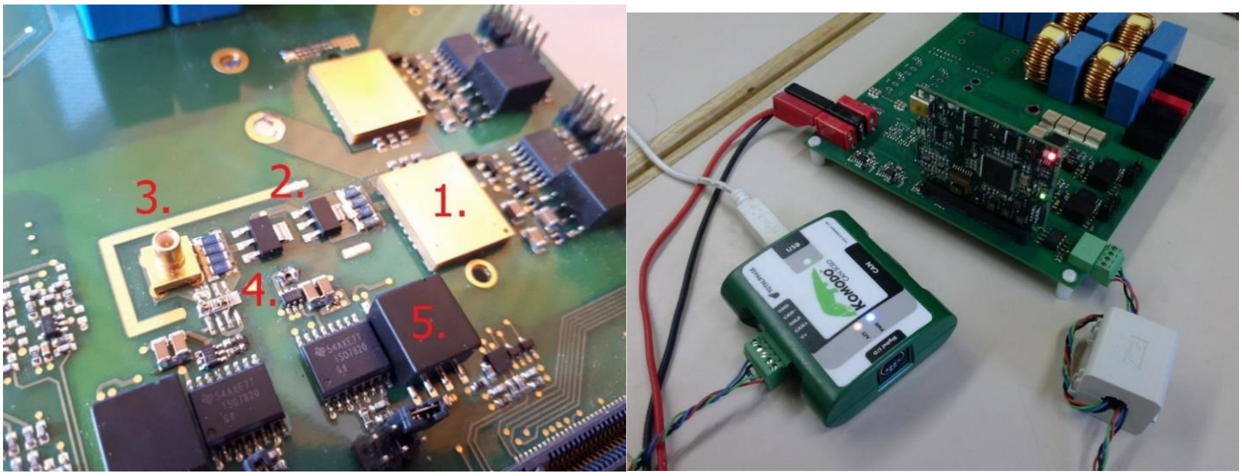

Fig. 23: Detail of the proposed tester (during sample #2 test)
1. - Device under test, 2. - Q1, 3. - Scope terminal, 4. - Q2, 5. Gate Drivers

The conclusion is that all the samples will exhibit an increased conduction loss in the application and the effect cannot be predicted from the manufacturer's datasheet. On the other hand, the relative increase will be more significant at higher operating frequencies (>1MHz) in case of sample #3. In case of sample #1 and #2 the increase is permanent during the on state.

Table 1: Part numbers and catalogue R_{DSon} of tested samples

Sample	***Part Number***	***Datasheet R_{DSon}***	***Normalized/DC R_{DSon}***
#1	GaN Systems GS66506T	67mΩ	61mΩ
#2	VisIC V22N65A	22mΩ	22mΩ
#3	Panasonic PGA26E07	56mΩ	55mΩ

Measurement of dynamic R_{DSon} is the part of JEDEC standard for qualification of wide bandgap devices. As can be seen from currently defined standard JC-70 available online [9], the exact definition of measurement setup is missing. Proposed method does not require special equipment for operation, therefore design and implementation to qualification process should be straightforward.

Design data of GaN R_{DSon} Tester (Schematic + PCB and BOM), created in student version of PCB design software Eagle (Autodesk), is available in electronic appendices to this thesis.

5 OPTIMIZATION OF DC/DC CONVERTER USING GAN SEMICONDUCTORS FOR HARD SWITCHING APPLICATIONS

Gained knowledge by investigating parameters of Gallium Nitride semiconductors and implementing of novel cooling methods in previous chapters, will be applied in a design of a power converter in this chapter. Based on parameters of available GaN power MOSFETs and a possible improvement of switching losses mainly, high voltage (400VDC) DC/DC converter is a scope of focus.

As the majority of nowadays produced electronic devices have to contain power factor correction, is for analysis chosen totem pole topology (Fig. 24) suitable for middle range power (3kW). Converter is designed for operating voltage range meeting one phase European mains voltage with tolerance. With certain power derating, operation starting from 90VAC input voltage (USA, JAPAN) is possible.

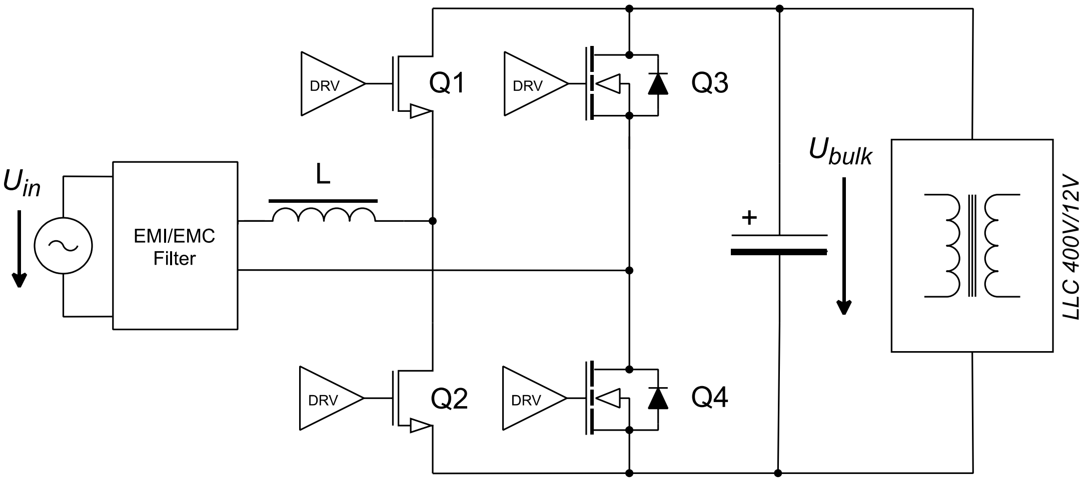

Fig. 24: Simplified block diagram of totem pole power factor correction converter with a DC/DC converter on the output

Input power factor correction with this input and power requirements can be found nowadays mainly in power supplies for Server, Data center and Telecom applications. Quantity of power supplies produced for the aforementioned markets is rising significantly, as the demand for data storage is enormous due to rise of various social media and streaming services. To make this growth in energy demand sustainable, innovative technology steps are needed. On one hand, development of carbon-dioxide free/environmentally friendly energy sources to cover the rising demand for electricity, on the other hand pushing for improvement of existing solutions to make them more effective, therefore less energy demanding. In applications where high volume of power supplies is used, every watt of power loss is multiplied by quantity of installed systems – by improving single unit overall saving is significant.

This simple fact is recognized by European Union Commission, which is pushing for efficiency of power supplies used for computer applications. Those requirements are evolving over time, which works partially as a booster for the economy. Nowadays, all power supplies sold on European market need to be compliant with 80plus Platinum certification. From year 2026, new regulations are applicable, requesting for 80plus Titanium certification, which might be challenging and expensive to meet without improvements in semiconductor technology. Table below shows required efficiency levels to fulfill the certificate – efficiency is measured input to output including all power stages inside with control circuits consumption and auxiliary converter load (standby output).

Load condition	80 PLUS BRONZE	80 PLUS SILVER	80 PLUS GOLD	80 PLUS PLATINUM	80 PLUS TITANIUM
	Efficiency limit				
10%	-	-	-	-	90%
20%	81%	85%	88%	90%	94%
50%	85%	89%	92%	94%	**96%**
100%	81%	85%	88%	91%	91%

Table 2: 80plus efficiency limits, 80plus titanium applicable from 2026

As can be seen from the table, highest efficiency limit is always at half load. This requirement has origin in server applications, where redundancy of input power is required to avoid any data loss or operation failure in case of single PS unit failure. Therefore, during significant part of the lifetime power supply is operating in parallel with 50% load, where optimization makes highest effect from the system point of view. For the mentioned reasons, the intention is to show and explain design of converter optimized for highest efficiency and power density with novel semiconductors, which might be used as a reference for future designs of power supplies.

5.1 POWER STAGE DESIGN

For power factor correction converter design in this chapter, we are looking for power GaN transistor with R_{DSon} range from 30-70mΩ, to keep conduction losses in reasonable range, especially at minimum of input voltage. At the time of writing this thesis, there are only three candidates from three different manufacturers available:

Manufacturer and Part number	**Declared R_{DSon} at 25°C**	**Package style**
VisIC V22N65A	22mΩ/650V	Top – Manuf. Specific
GaN Systems GS66516B	25mΩ/650V	Bottom – Manuf. Specific
Infineon IGO60R070D1	70mΩ/600V	Bottom – PG-DSO

Table 3: Available GaN parts suitable for 3kW PFC

As the top side cooling has higher space requirements, for high speed/switching branch the GaN Systems GS66516B enhanced mode power MOSFET is chosen.

5.2 INDUCTOR OPTIMIZATION FOR HIGH EFFICIENCY AT HALF LOAD

One of the major contributors into overall power loss is power inductor. Distribution between power losses in inductor core and winding is depended on various parameters as number of turns, switching frequency of the converter and operating point in terms of input and ambient conditions. Ripple current is changing over operating conditions and affecting rms value of the current, which flows through power semiconductors. Therefore, it is varying conduction/switching losses in different parts of the circuits, especially at light load conditions. From this thought it is clear, that there exists certain optimum for power losses and parameters chosen.

As one of the design inputs we assume powder core material for its cost effectivity and easy of manufacturing. With knowledge of magnetic permeability and core dimensions, inductance can be calculated based on formula:

$$L(I,N) = \frac{N^2 . \mu_{eff}\big(H_{DC}(I,N)\big). A_e}{l_m} \tag{5}$$

To determine power loss in inductor winding, rms current at input of the converter needs to be calculated:

$$\Delta I_{L,RMS}(U_{RMS}, P_{OUT}, N) = \sqrt{\frac{1}{T}\int_0^T \left(I_L(U_{RMS}, P_{OUT}, N, t).\sqrt{1+\frac{\delta^2}{3}} \right)^2 .dt} \tag{6}$$

Manufacturer of powder core provides results of empiric measurements of volume power losses (W/m^3) based on operating frequency and magnetic flux density:

$$\Delta P_{HF}(B,f) = \left(\frac{B}{1000G}\right).(3{,}4.f + 0.0006.f^{2{,}736}) \tag{7}$$

Optimal wire turns for lowest total inductor power losses can be found by derivation of equation for variable N equal to zero:

$$\Delta P_L(U_{RMS}, P_{OUT}, N)' = 0 \tag{8}$$

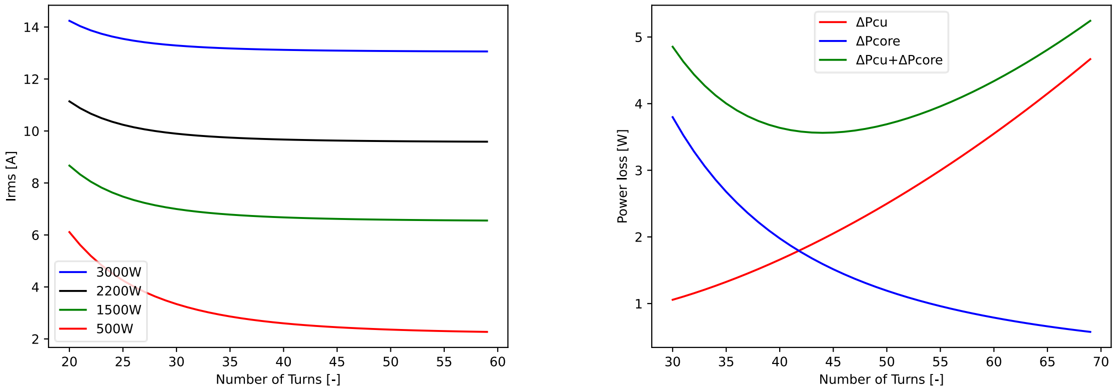

Fig. 25: Plot of input RMS current versus number of turns and various output operating conditions (left), Plot of inductor total power losses versus number of turns at nominal operating condition (right)

1.1 GAN POWER STAGE LOSSES EVALUATION

Power loss of GaN power MOSFETs can be divided into parts:

$$\mathit{\Delta} P_T = \mathit{\Delta} P_{T,R_{DSon}} + \mathit{\Delta} P_{T,Sw} + \mathit{\Delta} P_{T,RevC} \tag{9}$$

Where $\mathit{\Delta} P_{T,R_{DSon}}$ is representing conduction losses depended on the square root of the current flowing through the device, $\mathit{\Delta} P_{T,Sw}$ are switching losses and $\mathit{\Delta} P_{T,RevC}$ are losses caused by reverse conduction of the current. To calculate conduction losses, precise value of RMS current needs to be calculated first - cycle by cycle calculation method using scripting language Python is used. This method simply integrates square root of current over every switching cycle during period of the line voltage with consideration of ripple current:

$$I_{RMS,Cycle}(U_{RMS}, P_{OUT}, N, t) = \sqrt{\frac{1}{T_{SW}} \int_0^{T_{SW}} i_{Switch}(U_{RMS}, P_{OUT}, N, t)^2 . dt_{SW}} \tag{10}$$

In second step the period RMS is calculated by summing all switching cycles in line voltage period (T/T_{SW}):

$$I_{T,RMS}\big(U_{RMS}, P_{OUT,} N\big) = \sqrt{\frac{1}{T} \int_0^{T} I_{RMS,Cycle}(U_{RMS}, P_{OUT}, N, t)^2 . dt} \tag{11}$$

Switching losses can be calculated by analyzing separately turn-on and turn-off event:

$$\mathit{\Delta} P_{T,Sw}(U_{RMS}, P_{OUT}, N) = \frac{\mathit{\Delta} E_{OnSwitch}(U_{RMS}, P_{OUT}, N) + \mathit{\Delta} E_{OffSwitch}(U_{RMS}, P_{OUT}, N)}{\frac{T_{in}}{2}} \tag{12}$$

Energy lost at turn-on event can be calculated by formula:

$$\mathit{\Delta} E_{On}(U_{RMS}, P_{OUT}, t) = \frac{1}{4} U_{BULK}. I_{SW}(U_{RMS}, P_{OUT}, t). t_{sw}(U_{RMS}, P_{OUT}, t) + E_{oss} + E_{qoss} \tag{13}$$

Where first part of the equation assumes, that drain-source voltage starts to drop after current reaches inductor value, energy pulse has triangular shape for certain time t_{sw}. Second part defines energy lost by charge of nonlinear intrinsic capacitance (C_{OSS}):

$$E_{oss} = \int_0^{U_{BULK}} u_d . C_{OSS}(u_d)^2 . du_d \tag{14}$$

And third part represents charge of nonlinear capacitance of opposite device in half bridge configuration [33]:

$$E_{qoss} = \int_0^{U_{BULK}} (U_{BULK} - u_d). C_{OSS}(u_d)^2 . du_d \tag{15}$$

For purpose of calculation, nonlinear drain-source capacitance stated in manufacturers datasheet was converted into array of values using free web tool (WebPlotDigitizer by Ankit Rohatgi). Therefore, calculation of integrals stated above can be performed by python script (see Attachment no.7). Calculating E_{oss} by formula state above gives same value (17μJ) as stated in the datasheet (using same conditions), which is correct.

Energy lost at turn-off event can be calculated according to:

$$\Delta E_{Off}(U_{RMS},P_{OUT},t)=\frac{1}{4}U_{BULK}.I_{SW}(U_{RMS},P_{OUT},t).t_{sw,off}(U_{RMS},P_{OUT},t) \tag{16}$$

Total energy lost during turn-on and off events over half period of line voltage can be calculated as sum of energy lost in every switching cycle:

$$\Delta E_{OnSwitch}(U_{RMS},P_{OUT})=\sum_{X=0}^{\frac{f_{sw}}{2.f_{in}}}\Delta E_{On}\left(U_{RMS},P_{OUT},\frac{f_{in}.x}{2.f_{sw}}.T_{in}\right) \tag{17}$$

$$\Delta E_{OffSwitch}(U_{RMS},P_{OUT})=\sum_{X=0}^{\frac{f_{sw}}{2.f_{in}}}\Delta E_{Off}\left(U_{RMS},P_{OUT},\frac{f_{in}.x}{2.f_{sw}}.T_{in}\right) \tag{18}$$

During transition between high and low side switch, is for certain time one of the switches conducting current in reverse mode. For e-mode and GIT transistor structure is the source-drain voltage in reverse conduction mode directly depended on the Gate-Source bias, voltage drop in reverse mode can be approximated by nonlinear curve:

$$V_{S\rightarrow D}(I_{S\rightarrow D})=4{,}3V+I_{S\rightarrow D}.0{,}095\Omega \tag{19}$$

Therefore, energy dissipated by reverse conduction can be calculated as:

$$\Delta E_{RevC}(U_{RMS},P_{OUT},t)=V_{S\rightarrow D}\big(I_{SW}(U_{RMS},P_{OUT},t)\big).I_{SW}(U_{RMS},P_{OUT},t).t_{deadtime} \tag{20}$$

where $t_{deadtime}$ is fixed and its value is 50ns for both edges. Power loss assigned to reverse conduction of current can be calculated as sum of all events divided by half period of line voltage

$$\Delta P_{T,RevC}(U_{RMS},P_{OUT},N)=\frac{\sum_{X=0}^{\frac{f_{sw}}{2.f_{in}}}\Delta E_{RevC}(U_{RMS},P_{OUT},t)}{\frac{T_{in}}{2}} \tag{21}$$

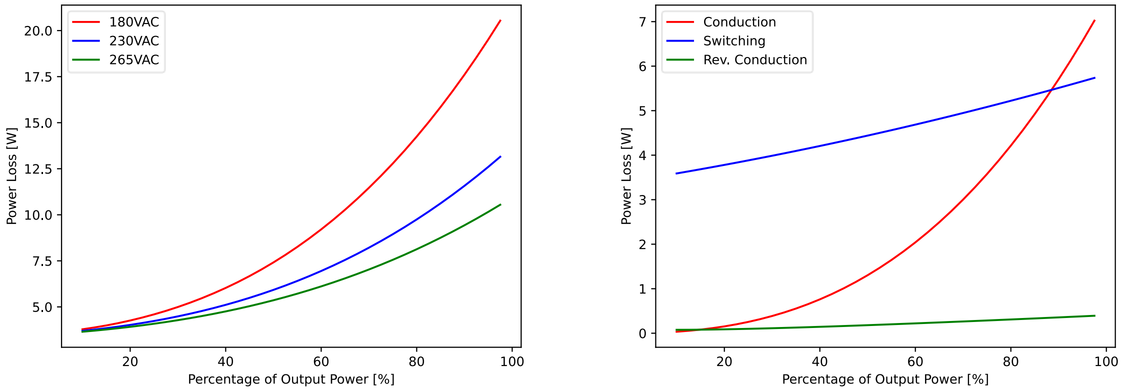

Fig. 26: Results of power losses calculation of GaN MOSFETs in 3kW totem-pole converter, dependency on output power and input voltage (left), overview of power losses at nominal operating conditions (right)

5.1 CONTROL LOOP DESIGN

Nowadays trend in the power converters, starting from few kilowatts, is a digital control – calculating control loop in the software programmed typically into Digital Signal Processor (DSP) or Field Programmable gate array (FPGA) in connection with system control microcontroller.

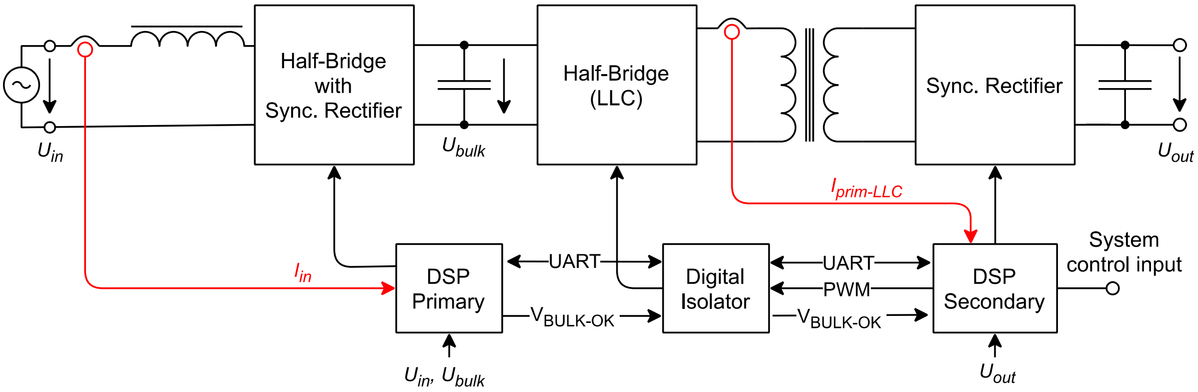

Fig. 27: Block diagram of digitally controlled power converter with galvanic isolation

For designed power converter, the newest (at this time) and cost optimized 32-bit floating point DSP from Texas Instruments TMS320F280041 is selected. Though, similar DSP can be found in portfolio of NXP (Freescale) or ST Micro. Block diagram describing control loop operation with explanation is part of the thesis.

5.2 DEBUG TOOL FOR DIGITALLY CONTROLLED SYSTEMS

Verification of sampled value, tuning the control loop or simply detecting the root cause of the issue might be the daily business for electrical engineer. As digital control design is a base of this thesis, tool to display “variables” on the oscilloscope screen was designed by author in free PCB design tool KiCad - design files together with STL file for 3D printed box are public and available in the appendices.

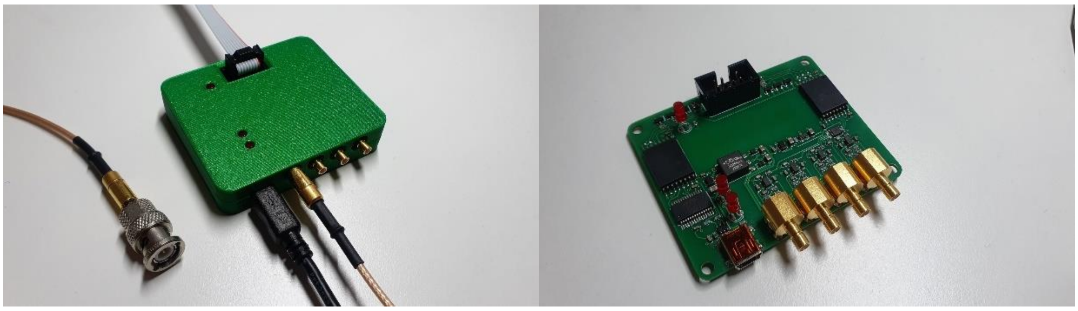

Fig. 28: *Picture of debug tool prototype*

Heart of the debug tool is four channel buffered analogue to digital converter AD5324ARMZ from Analog Devices, controlled over isolated serial peripheral interface with clock rate up to 30MHz.

5.3 DESIGN VERIFICATION

After characterization of all power losses, verification of voltage and current rating of all components, verification of cooling concept by FEM simulation and finalization of schematic for control circuits and main board, design can proceed to phase of printed circuit board design and assembling of the prototype. Before powering up of the assembled unit, all supply voltages and signals are verified.

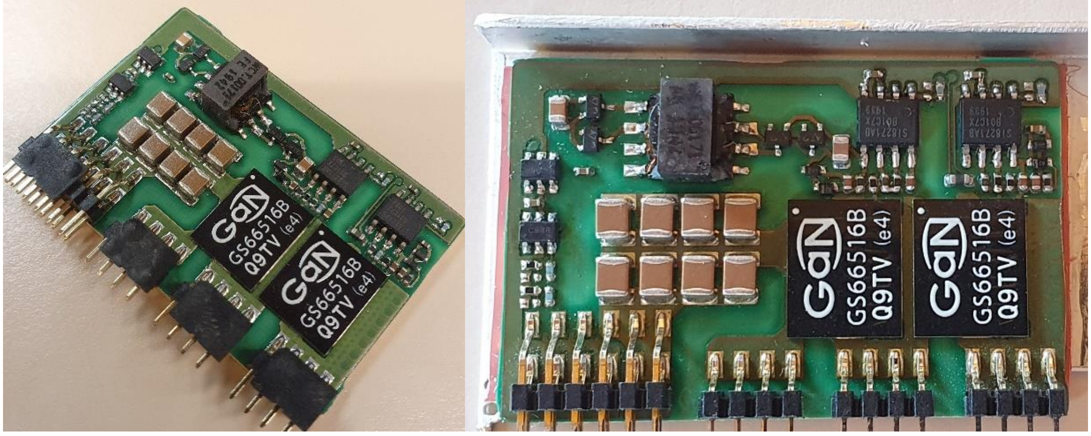

Fig. 29: Tested prototype – Insulated metal substrate board with GaN (GS66516B) half-bridge and insulated gate drivers after SMT assembly (left), assembled to the aluminum heatsink (right)

Single side insulated metal substrate board assembled with GaN Half Bridge and isolated gate driver is assembled on aluminium heatsink. Finished sub-board is therefore assembled into “mainboard”, which is 6-layer PCB providing connection between rest of the power components, such as inductor, bulk capacitor, EMC filter and the second power stage of the power supply – resonant converter (known also as LLC) providing 12VDC output voltage.

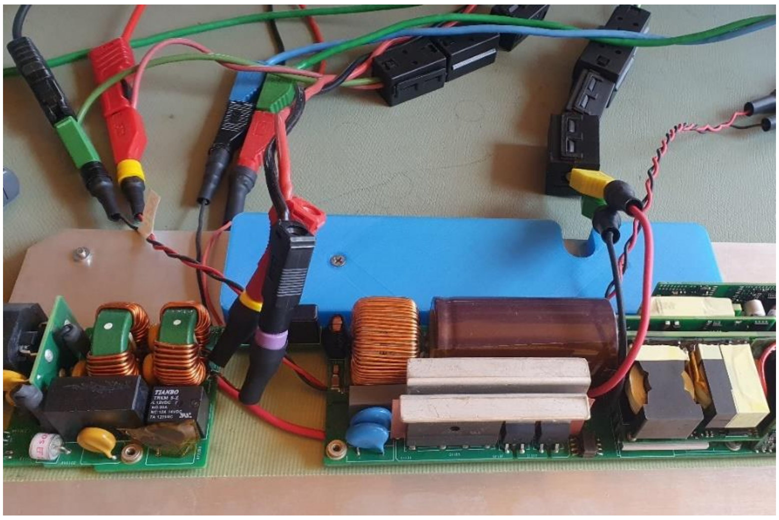

Fig. 30: Tested prototype – Efficiency measurement test setup

Synchronous rectifier is attached on the same heatsink profile as GaN board and is visible in Fig. 30. Aluminium heatsink is simple L shape, which might look insufficient for calculated power losses – as the power density is high priority in case of this power supply form factor, cooling is managed by high power FAN.

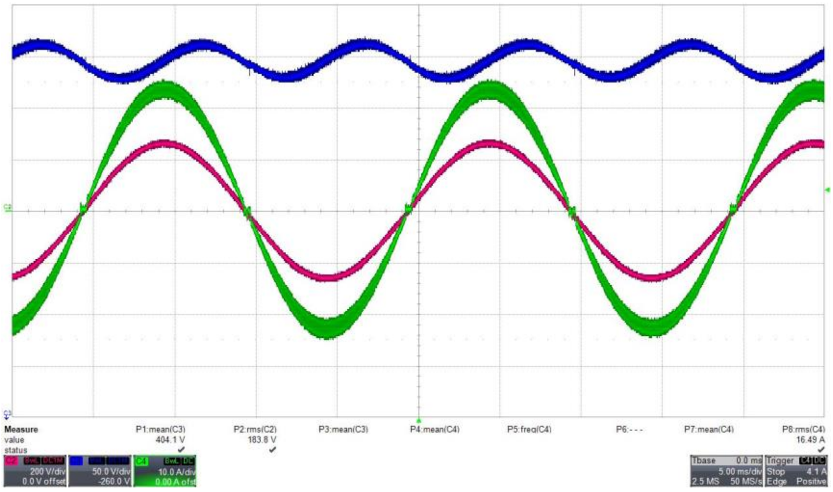

Fig. 31: Input voltage, bulk voltage and current waveform at 180VAC input voltage and 3kW output power (90kHz switching frequency), timebase 5ms/div

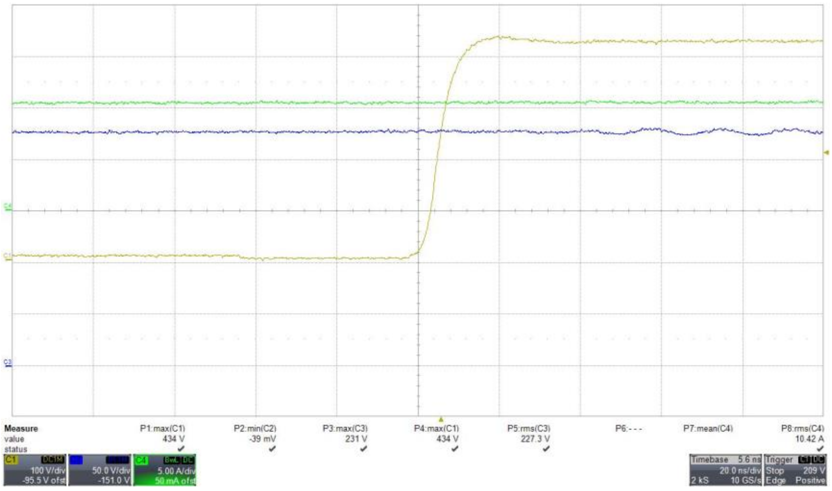

Fig. 32: Drain-Source voltage (Yellow) of GaN Half-Bridge at DC input voltage with detail on rising edge, green waveform is power stage current, timebase 20ns/div

Thermal camera snapshot below shows converter operation at minimum input voltage and full load 3kW, with improvised FAN cooling on the test bench. As the heatsinks are designed for high airflow in its surroundings, the measured temperatures are higher than one in the enclosure.

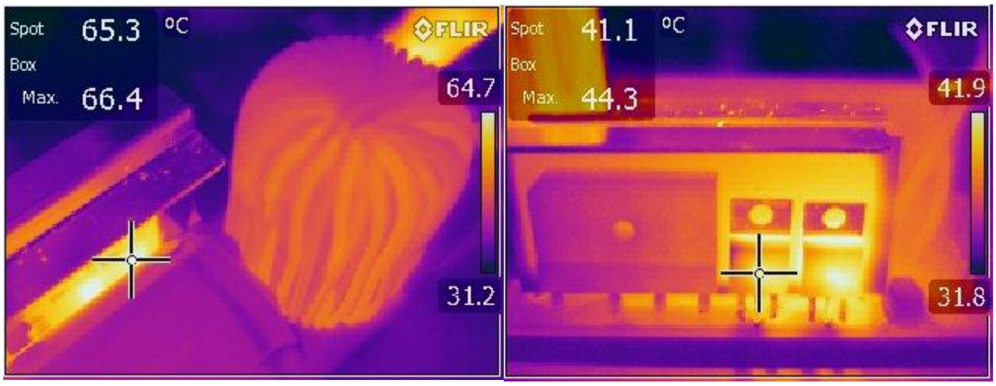

Fig. 33: Thermal camera picture of power stage during operation at full power 3kW – GaN half bridge on insulated metal substrate board (left), synchronous rectifiers (right)

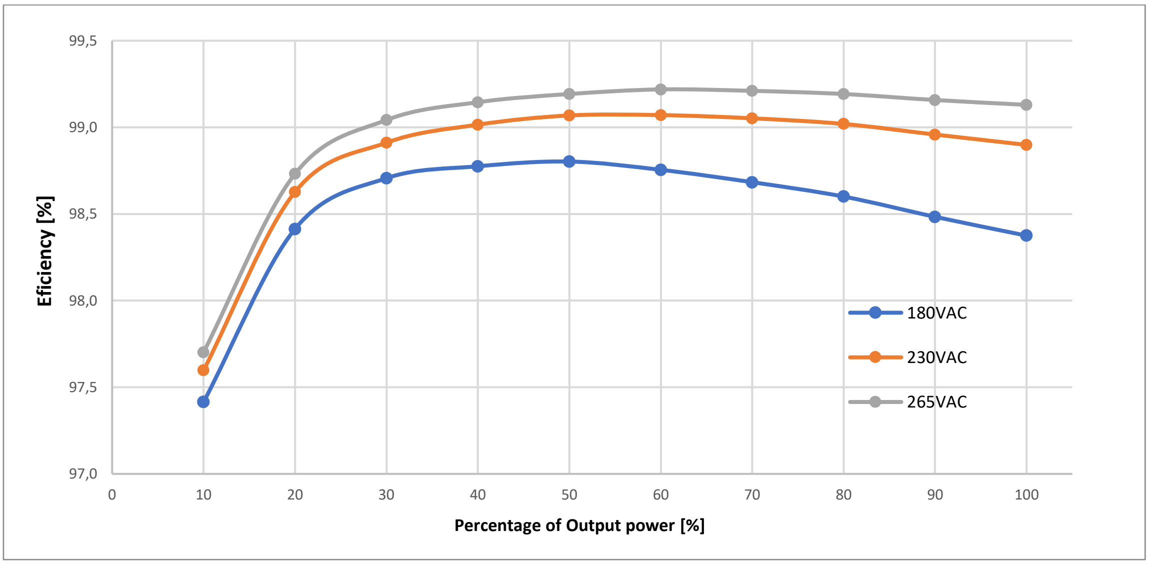

Fig. 34: Measured efficiency curves of tested prototype for various input voltage and output power conditions (at 60kHz)

Using scripting language and equations for power losses of all components, efficiency curve can be calculated for various input voltages and output power. As can be seen from both graphs, calculated curve is matching measured with +/-2W tolerance in power loss over the whole range of loads. Converter is reaching peak efficiency between 50-60% of load at the nominal conditions, optimization target is achieved. Maximum point of efficiency moved above half load of power factor corrector might be useful, as converter efficiency in 80Plus certification is qualified based on power present on the output terminals, therefore some margin for power losses of second DC/DC power stage is present.

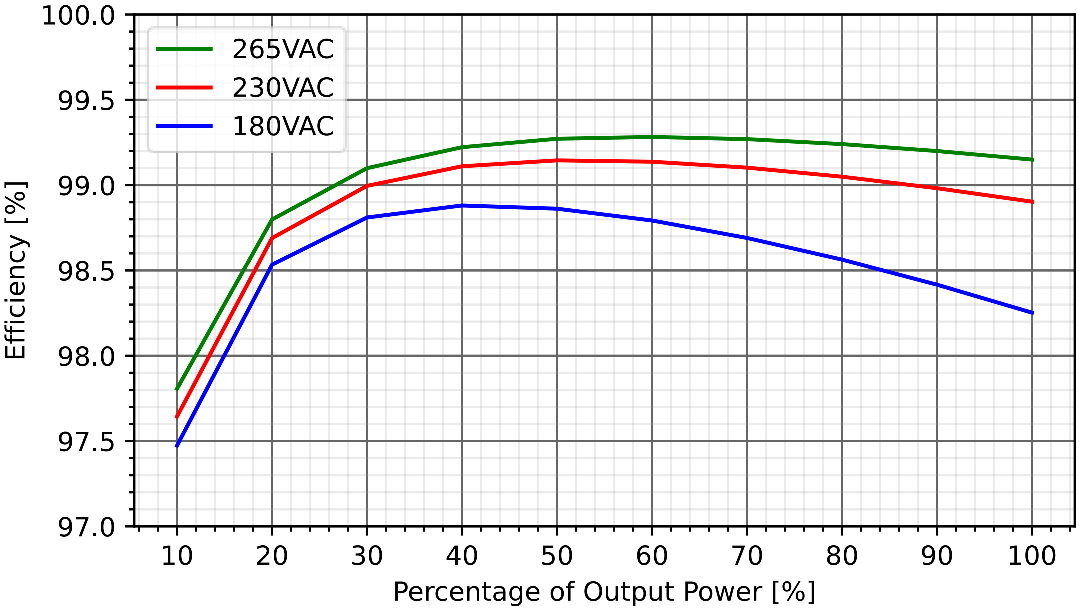

Fig. 35: Calculated efficiency curves of tested prototype for various input voltage and output power conditions (at 60kHz)

6 RECUPERATING GATE DRIVE SOLUTION

Following lines shows example of improvement of synchronous rectifier of high output current resonant converter, by using special recuperative Gate driver circuit for Silicon MOSFET. Circuit is using very fast Gate driver (LMG1020) specifically designed for GaN devices.

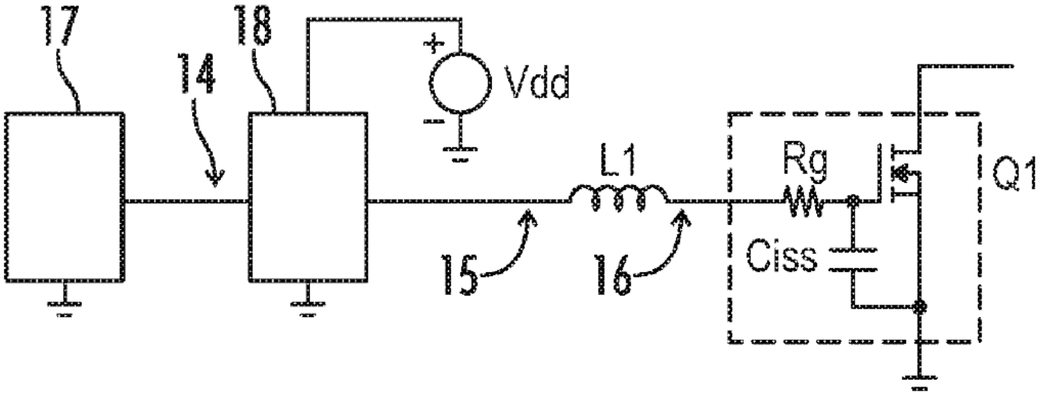

Fig. 36: Recuperative Gate driver for high current synchronous rectifier

Principle of operation can be explained as one cycle buck-boost converter, inductor L1 is used for energy accumulation during switching cycles. By proper sequence of driving pulses for GaN driver can be achieved, that resonant waveform between inductor and Ciss of MOSFETs, damped by Rg, ends exactly at desired point – at maximum of Vdd during turn on cycle, at minimum voltage during turn off – “big” silicon MOSFET Gate discharge.

Fig. 37: Scope snapshot of recuperative gate driver during operation (left), Detuning effect of Miller capacitance (right)

To create driving pulse sequence displayed on picture above, DSP operating at 100MHz with minimal resolution 10ns per bit is required to be able to precisely tune resonant cycle, therefore achieve the best efficiency of recuperation.
This solution of Recuperative Gate Drive Circuit and Method is registered by United States Patent US10250249B1, owned by Bel Power Solutions Inc. Santa Clara US.

CONCLUSION

Aim of this thesis is to explore and analyze advantages of Novel Gallium Nitrite wide bandgap transistors technology in switch mode power supply applications. Special focus is high power density and high efficiency power supplies used for server and telecom applications, as optimization in this field of power consumption brings significant power savings worldwide, reduction of carbon dioxide production is possible. Due to Author´s tight cooperation with industry, given goals and investigated topics are related to major problems related to successful implementation of novel technology into commercial products.

Partial goals of this thesis are fulfilled and have following conclusions:

1. Portfolio of currently available GaN devices is limited, but growing constantly and attacking higher ratings with every newly released device. Nearly all nowadays available transistors are produced as GaN structures on standard Silicon wafers – which gives advantage for ease of implementation into production for chip manufacturers, on the other hands limits the possibilities of price reduction, therefore attractiveness of GaN for commercial products. Conducted analysis shows, that one of the most promising structures is enhanced mode transistor, although also the most challenging for gate driver performance. Future of GaN switching devices might lead to on chip integrated drivers aiming to maximize the device performance in custom designs.

2. Gate driving requirements are minimizing package sizes dramatically. Third Chapter shows novel methods and design principles to achieve high performance cooling of minimized surface mount packages, widely used for recently released GaN devices. Special insulated metal substrate printed circuit board stack-up, developed in cooperation with PCB manufacturing company, optimized for cooling and switching performance is presented and proposed as reference for industrial designs. For cost sensitive applications, lower performance methods of cooling are presented and optimized using FEM simulations. Extensive research is proven by measurement on various physical prototypes.

3. One chapter of this thesis is related to deep analysis of the problem related to early samples of GaN devices from all manufacturers - electron trapping under the gate electrode of high electron mobility transistors. As a result of this phenomena is on state channel resistance variation over the time shortly after the switch event present, resulting in possible higher conduction losses in high switching frequency operating converters. To characterize this problem, special tester able to operate with standard equipment was developed and measurement on three different samples from three different manufacturers

was conducted. Gained results show, that certain increase in on state channel resistance is present and might impact the end application. Test setup was published and proposed to JEDEC committee, as one of the points stated in standard JC-70 required for successful qualification of wide bandgap devices is dynamic R_{DSon} measurement.

4. Results of research from previous chapters are now applied in design of totem pole converter for power factor correction with 3kW output power. Application of fast switching GaN transistors gives biggest advantage in hard switching applications, where the efficiency and power density improvements are significant. Choice of power and input voltage range is not random - 80Plus Titanium mark in server/computer applications is requested by upcoming European Union regulations, therefore optimization of PFC stage together with isolated DC/DC converter is needed for all newly designed power supplies entering mentioned sectors. Peak efficiency of designed converter is after optimization of all components achieved at half load and exceeding 99% at nominal input conditions, which gives good margin and it is fulfilling defined target.

   High power density of the converter is achieved by integrating gate driving circuit together with power stage on insulated metal substrate board. Optimized control technique performed by digital signal processor reduces the needs for hardware complexity and size of the components used. Complete design verification measurements - including oscilloscope snapshots, thermal measurement and emission analysis of totem pole converter using novel Gallium Nitride technology are included.

5. Outstanding parameters of components developed specifically for GaN transistors, might give advantages in different fields of electronics – example can be seen in eight chapter of this thesis. Further efficiency optimization of resonant converters might be particularly difficult, if ultra-high efficiency needs to be achieved. For this purpose, innovative recuperative gate driving method for secondary side silicon rectifier of resonant converter was developed, resulting in successful US patent application.

One of the major drivers for success of GaN technology in commercial applications is optimization of its cost, which is comparing to its robust SiC counterparts still questionable. Author’s research will continue by exploring transition mode of operation, which together with Gallium Nitride semiconductors and advanced control algorithm might give various advantages in specific converter topologies. Analysis of the reliability data related to converters based on GaN semiconductors operating in the field might be interesting topic for future research.

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Author´s Publications related to topic of this Thesis

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Patents

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Employment History

September 2020 – now	Electrical Design Engineer at Green Cubes Technology GmbH, Uster - Switzerland
August 2017 – August 2020	Electrical Design Engineer at Bel Power Solutions GmbH, Uster - Switzerland
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Education

2016 – 2021	Doctor of Philosophy (PhD.), Brno University of Technology, Brno, Czech Republic
2014 – 2016	Master´s degree, Brno University of Technology, Brno, Czech Republic
2011 – 2014	Bachelor's Degree, Brno University of Technology, Brno, Czech Republic
2007 – 2011	Stredná priemyselná škola, Dubnica nad Váhom, Slovakia

Internships

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Scope of Focus:

Power electronics – switch mode power converters, control loop design and implementation in DSP (C & ASM), battery management systems