

On-Chip Energy Harvesting for Implantable Medical Devices

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Abstract. *The paper brings an overview of main challenges in implantable medical devices (IMD) research area, where the main objective of discussion covers wireless power transferring (WPT) systems as the hot topic dedicated to energy harvesting that is still gaining in popularity. The paper is focused on electromagnetic-transfer principle, where full integration of the WPT systems on a chip is taken as the primary goal covering passive transducer and rectifier implementations. The presented research reveals many issues raised from the state of the art solutions. These solutions can or should be detailed investigated in the future research. Therefore, this paper discusses about so far hidden potential of fully integrated WPT systems, where both near-field and far-field approaches are included. Additionally, the discussion is also extended to a principle of power transfer efficiency (PTE) maximization through approaches such as matching and finding the optimal source/load together with rectifying and regulating issues.*

Keywords

Wireless power transferring systems, energy harvesting, fully on-chip WPT implementation, electromagnetic-transfer principle, on-chip antennas

1. Introduction

Advanced modern technologies of integrated circuit (IC) fabrication are characterized by not only high density of circuit elements but also the support of heterogeneous systems such as systems-on-chip (SoC) including radio frequency (RF) structures and compatibility of micro-electro-mechanical systems (MEMS) in the post-processing steps. In other words, IC research area has a promising potential to deal with selected issues of energy harvesting (EH) and contribute to the entire system miniaturization. Just miniaturization (in addition to the energy consumption) belongs to one of the most critical task in medical applications such as IMDs or grown in popularity active implanted medical devices (AIMDs). AIMDs according European Union direc-

tive 90/385/EHS extend definition of active medical device (AMDs) that originally says: "AMD is any medical device relying for its functioning on a source of electrical energy or any source of power other than that directly generated by the human body or gravity." This part of the definition is important in terms of necessity for a permanent battery power source, which is partially in conflict with the recent trend of full energy autonomy by replacing them with internal EH systems. Such devices recycle renewable energy from environment and are usually, but not necessarily, implemented as MEMS in order to ensure their compactness [1–5].

Nowadays, many internal EH systems are still not capable to completely fulfill power requirements of energy-hungry electronic systems under the full operation conditions. Unfortunately, tens (rarely slightly above hundreds) of $\mu\text{W}/\text{cm}^2$ (cm^3) of available non-time-deteriorated power per area (volume) densities can be expected in the most optimistic case for medium and deeply implanted IMDs not based on strong kinetic movement such as waving of limbs [6–9]. In the case of internal energy harvesting, researchers are looking for solutions especially in fuel-cell based harvesters with encouraging results of thousand of $\mu\text{W}/\text{cm}^2$ in peak but at the cost of significant gradual degradation over time [8]. However, to compare the power available from internal energy harvesters with specifications of selected medical devices and applications (Tab. 1), one can conclude that the current solutions only recline in mutual intervention of internal harvesters and a battery like the power source. Such approach inevitably negatively impacts the lifetime of IMDs. Perhaps, the only potential exception includes heart-function stimulus and monitoring system, and low-duty cycled operating devices.

From IMD trends point of view, the alternative could be implementation of external energy harvesters (known as wireless power transfer - WPT EHs), and especially those based on acoustic and conduction (for medium and deep implantation depths), then optic, electric and electromagnetic principle (for shallow or subcutaneous implantations) [3, 9, 12–20]. All of them can be realized as relatively planar structures and selected ones directly benefit of their semiconductor nature. Therefore, there is a huge

Application	Power	Communication	Energy Source
Pacemaker, Cardioverter-defibrillator	$\leq 10 \mu\text{W}$ $\leq 100 \mu\text{W}$ $1 - 10 \mu\text{W}$	inductive link	primary battery, 10-year lifetime
Hearing aid	$100 - 2000 \mu\text{W}$	telecoil	rechargeable battery, 1-week lifetime
Analog cochlear processor, Cochlear implants	$200 \mu\text{W}$ $1 - 10 \text{mW}$	inductive link	rechargeable battery, 1-week lifetime
Neural implants	$1 - 10 \text{mW}$ $1 - 100 \text{mW}$ $10 - 200 \text{mW}$	high-rate inductive link	external battery, inductive power
Retinal implants	200mW $40 - 250 \text{mW}$ $1 - 100 \text{mW}$	high-rate inductive link	external battery, inductive power
Insulin pump	$10 - 50 \mu\text{W}$	-	-
WBAN monitoring	$140 \mu\text{W}$ $\leq 100 \mu\text{W}$	far-field wireless link	primary battery
Artificial heart	$10 - 100 \text{W}$	-	external source, inductive power

Tab. 1. Specifications of selected medical devices and applications [7, 8, 10, 11].

potential in direct full implementation in a standard CMOS process (omitting acoustic harvesters as primarily MEMS based ones), which turns out to be greatly attractive in terms of many benefits such as miniaturization, increase of system and packaging reliability, low-cost solution, omitting post-processing steps, etc. All these advantages become the driving force towards integration of the entire EH into a chip, where the choosing of an adequate WPT approach for the final application depends directly on specific requirements of the system itself such as energy density, depth of IMDs implantation, necessity for out-of-body energy-transport, and so on.

2. EM-Based WPT Systems

From the global perspective of WPT systems, the electromagnetic (EM) transfer energy systems based on near reactive and radiative field (reactive near field means magnetic-based coupling) belongs to the most popular ones. Here, one can expect typically tens of mW with $\eta > 50\%$ and from tens of μW to ones of mW with $\eta < 10\%$ in a case of fully discrete system (size $\geq 10 \times 10 \text{mm}$) and more compact version (size $\leq 10 \times 10 \text{mm}$), respectively [17], [18]. Such an approach enjoys tremendous popularity also in powering of many market products such as Activa RC Neurostimulator, Eon Mini Rechargeable IPG or others. These results were achieved through a long history and with an extensive research accompanied by the relatively simple design and implementation. This simplicity is anchored mainly in:

- The straightforward implementation chain of WPT individual circuit blocks (Fig. 1).
- Neglecting (without introducing significant error) of parasitic effects of the transfer media itself in operation with the frequency range well below 100 MHz. Such parasitic effects contribute to the attenuation of EM wave (material loss) and multiple reflection at individual tissues interfaces (reflection loss), which start to be already notable above 100 MHz [21].

However, while the full-integration effort of energy harvesters remains relatively untouched, the second item mentioned above must go through serious investigation due to inevitable pushing the operation frequency to the considerably higher values (if compared to commonly used discrete solutions). Generally, from far-field point of view, higher frequency value improves not only radiation efficiency but also impedance matching capability. On the other hand, in the near-field case, increasing rate of magnetic intensity change also often contributes to the improvement of the PTE in terms of getting a passive rectifier into better working conditions. But one has to keep in mind that increasing the frequency also increase losses in tissues. Therefore, amount of the transferred power required for correct IMDs operation strongly depends on PTE under the supervision of health hazard limits such as specific absorption rate (SAR), local maximum induced electric field strength E , and current density J [21], [22]. It is obvious that the only way how to bring power hungry IMDs to life without violation life-threatening limits lies in the PTE enhancement. Being aware of this, the paper brings analysis of selected issues (associated with on-chip energy harvesters) divided into the following three sections: Sec. 2.1: On-chip EM Transducer, Sec. 2.2: Rectifiers and PTE, and Sec. 3: WPT Design Example. It should be noted that attention will be primarily focused on-chip EM transducer and everytime when talking about on-chip antenna (OCA) we will refer to a passive structure designed and implemented together with the active part of the system in a single chip (known as SoC).

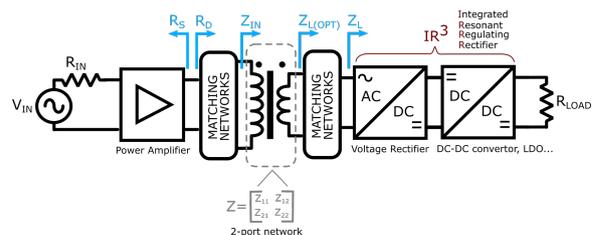


Fig. 1. Block diagram of the power transfer in a point-to-point WPT system with control management on the receiving side.

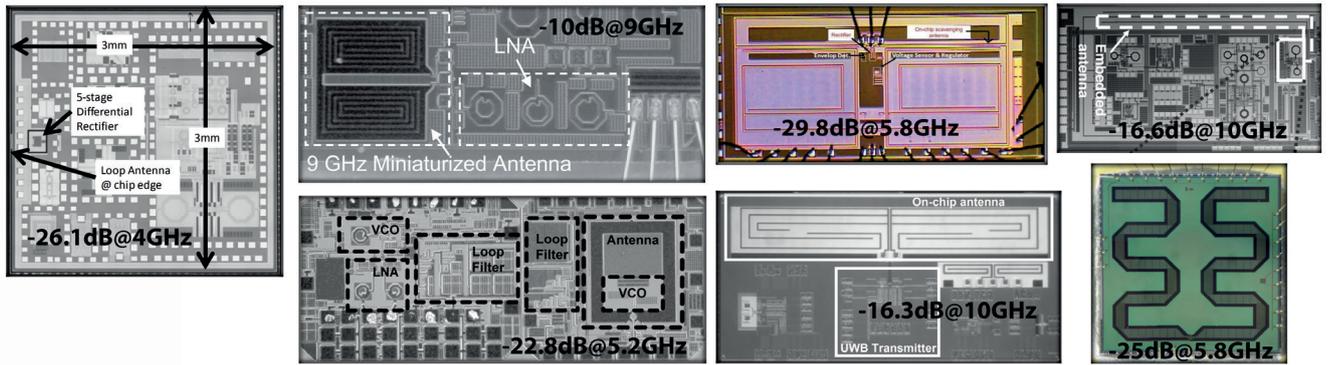


Fig. 2. Example of OCAs realized in standard CMOS process [23–30].

2.1 On–Chip EM Transducer

2.1.1 Far-Field OCA

As indicated above, for on-chip antenna realization, the standard operational frequency is shifted up to tens of GHz and more to preserve the antenna performance features (e.g. convenient handling of matching condition, reasonable radiation gain, etc.) which originated from physical requirements. However, in the case of IMDs, using frequency values above GHz boundary can be impractical since the attenuation constant of lossy tissue increases rapidly with frequency [31]. The different challenges of a discrete version of the implanted antenna ([32]) and the OCA ([33], [34] or Fig. 2.) in IMDs research are obvious. For example, while in the discrete form in the case of MISC (402 – 405 MHz) and ISM (2.45 GHz) antennas, relatively reasonable gain (≈ -30 dBi) can be achieved for 2 – 3 cm implantation depth, the OCA solution suffers from radically poor performance, where in lower limit of 5 GHz, not more than -20 dBi antenna radiation gain (that drops sharply towards lower frequencies) is usually reached by common way. Moreover, if a path loss will be contemplated, additional decrease about 8 dB @ $f = 2.4$ GHz and 25 dB @ $f = 5$ GHz should be expected [35]. Such an observation about the total gain of -45 dBi seen from outside environment makes the OCA highly impractical for middle-depth IMDs applications, where PTE at least around 1% is recommended. The more perspective situation is in the case of subcutaneous implant devices, where the same discrete antennas are capable to deliver power with the PTE greater than 1%.

From this brief discussion, it is obvious that only modification of OCA structures based on techniques for electrically small antennas [36] or implementation of only elementary, physically design-based feasible techniques to reduce the impact of high-loss substrate (e.g. incorporation of a shielding layer [26], [37]) are insufficient for such desired frequencies (< 5 GHz) in a standard CMOS process. In addition, significant nuisance is caused by the following:

1. Absence of progressive techniques (lens forming, dielectric or cavity based resonator, waveguide technique, HIS/AMC or superstrate structures, micro-machining,

etc. [33, 37–43]) because of physical requirements or additional post-processing steps.

2. Limiting physical space for the OCA realization.
3. Presence of low resistivity substrate ($5 - 20 \Omega$), which is critical because electrically small antennas are characterized by high quality factor, and therefore, intensive reactive near field.

Therefore, it can be stated that for the intention to integrate the OCA antennas into IMDs applications, it is essential to find an alternative solutions or techniques to existing ones that would offer promising results.

One of the unconventional ways that we have investigated for OCA design, draws on idea of packaging the IC chip together with the OCA by so-called matching insulation layer (MIL) that can reborn the GHz frequency spirit by significant improvement of the radiation efficiency (Fig. 3). MIL concept was built on the following two main observations:

- observation based on application of a specific material with high relative permittivity (dielectric resonator or superstrate structure) and assessing its impact on OCA properties,
- observation based on close native analogy between packaging material of IMDs and a matching layer.

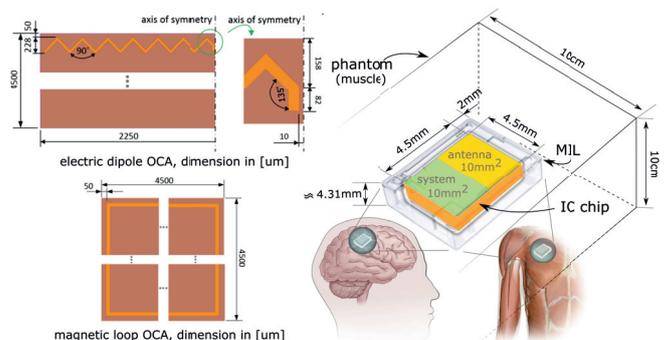


Fig. 3. Proposed concept based on MIL for IMDs.

For example, in the case of a dielectric resonator, it has been shown that ϵ_r in the range of values 40 – 60 at frequency ≈ 28 GHz contributes to reducing the influence of a low-resistance substrate leading to increased radiation efficiency and gain, which is caused by the "trapping" of the electromagnetic field primarily in electrically denser environment (dielectric resonator) rather than in individual modes of surface/substrate waves [42], [43]. In the case of superstrate structure application with a high ϵ_r , a positive effect on the radiation efficiency of the microstrip antenna (and also its vertical compaction) has been observed [44]. Horizontal compaction can be observed from the theory of conduction in multi-layer structures, where the incorporation of a material with a relative $\epsilon_r > 1$ increases the effective permittivity of the waveguide and thus, shortens the wavelength of electromagnetic waves travelling through them. The second point is aimed at especially to work of Mr. Merli and Dissanayake that prove that the incorporating material with suitable properties between a lossy tissue and antenna leads to negotiability improvement of the antenna performance. Including the previous discussion and all the findings [32, 45, 46], the gained knowledge essential for OCA and IMDs negotiability can be summarized into the following points:

1. Reduction of direct contact between the radiating element and the lossy environment contributes to an overall system improvement.
2. In the low-resistance substrate, the implementation of the super-stratified layer or dielectric with high ϵ_r positively affects the radiation properties of on-chip antennas and contributes to their overall compactness.
3. Inclusion of a dielectric insulating layer in the design leads to a reduction of insertion losses from the IMD perspective.
4. ϵ_r of both interfaces (tissue-MIL) should be the same or at least approximately the same (high ϵ_r of the soft tissue and hence the MIL results in a shifting of the reflection coefficient Γ to lower values and lower frequencies).
5. The MIL thickness should be maximized, but in reasonable manner not to endanger human health,
6. as a source of excitation of electromagnetic radiation it is better to use magnetic source rather than electrical one.
7. Negligible variability of Γ depending on the change in the conductivity of the tissue (the conductivity of the insulator was considered zero) in contrast to the considerable variability associated with a lack of consistency in ϵ_r of individual interfaces.

The powerful and great potential of the above-mentioned observations can be clearly observed in Fig. 4 that originated from idea presented in Fig. 3 with incorporation of a lossless MIL with $\epsilon_r = 50$. This graph shows results obtained from numerical simulations without the presence of lossy tissue, where properties of TSMC CMN90 fabrication process is considered and both OCAs are designed at AL-RDL (top) layer. It can be observed that the radiation efficiency of simple electric and magnetic dipoles quite

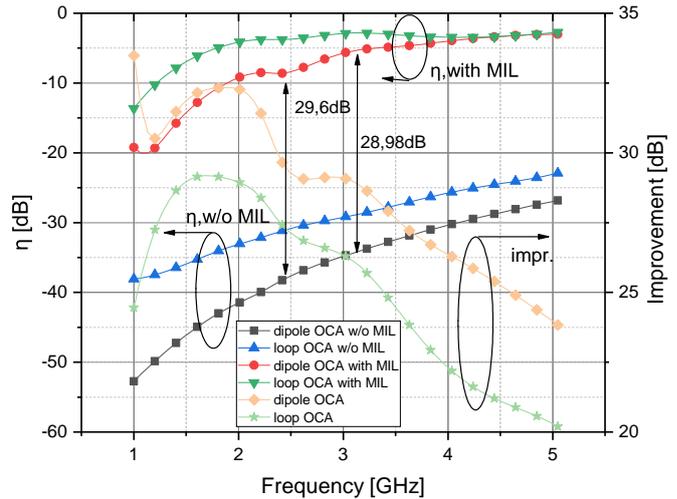


Fig. 4. The demonstration of promising OCA concept based on MIL for IMD application.

copies the performance of the published solutions from Fig. 2 (air as surrounding environment). It is obvious that a poor performance that drastically decreases with lowering frequency. However, if the MIL concept is considered, the situation significantly changes in favor of promising results. For example, roughly about 30 dB @ $f = 2.4$ GHz (1000-times) improvement with $\eta > -10$ dB was observed and so in conjunction with knowledge about 8 dB @ $f = 2.4$ GHz path loss, the proposed concept (in issue of EHs based on far-field OCA) potentially can open the door for low-depth implantation devices with theoretical efficiency close to 1%. Moreover, theoretically the concept does not need extra post-processing steps (in comparison to [47]) except for the packaging process itself.

2.1.2 Near-Field OCA

From the above discussion, one could conclude that GHz radiative far field is impractical for IMDs in terms of high attenuation of electromagnetic wave in a soft tissue and moreover, OCAs suffer for significant performance degradation under GHz boundary (seen as slope changes in Fig. 4). To deal with this issue, another solution has been carried out to get reasonable PTE while still being compatible with a CMOS process, and to fully retain the idea of miniaturization. The new trend has gained momentum especially in the last decade and is based on near field and magnetic coupling fundamentals (Tab. 2). Similar to the far-field research area, the main motivation is to achieve compactness, affordable price and reliability at the best possible performance of the WPT systems including OCA (in this case, OCA refers to strictly passive-inductive based structure with the ability to couple an external magnetic field, simply coil). Besides a pure MEMS implementations [48], there exist attempts to implement an antenna in the form of a coil directly on a silicon chip but this requires additional steps in a manufacturing process such as micro-machining [49]. It is also possible to use the process of contacting itself in the implementation of bonding coil with $L = 103.7$ nH, $Q = 24.25$ at 147 MHz [49], [50]. In general, such approaches lead to

the better system performance, however for the prize of increasing reliability risk that belongs to the most important requirements when speaking about IMDs. Therefore, implementation effort in the recent years aims at OCA realization especially.

Nowadays, there are two leading trends in near-field applications with integrated OCA, marked according to [58] as resonant inductive coupling: a) long-fledged high-frequency (≥ 850 MHz) [51, 52, 56, 57] based on radiative near field; and b) raising up lower-frequency (≤ 500 MHz) [22, 53, 55, 59–61] alternative that dominantly draws from benefits of reactive near field. The lower-frequency approach grows in interest especially due to success of Zargham’s two-port theory of the PTE maximization [62]. Table 2 shows selected works that reflect the state-of-the-art EHs implemented directly on a chip, where the attention was aimed at biomedical applications. One can observe that the systems with an integrated OCA (usually called rectennas to emphasize direct purpose of conversion to the output DC level) realized in a standard CMOS process are in general characterized by PTE not exceeding 1% for distance about 1 cm in practice, where weak coupling mostly determine the final performance of WPT systems. Traditionally, a coupling is increased by additional intermediate coil or multiple coils where for instance, so called booster antenna seen to be relatively perspective [63]. However, their implementation in IMDs is quite restrictive. Additionally, from Tab. 2 it can be stated that the use of lower frequencies (about hundreds of MHz) contributes to the effective design of WPT in case of EHs realized directly on the lossy chip, where huge loss in power efficiency through losses of the silicon substrate plays the main role [62]. The formula (1) reflects this phenomenon, where σ_{SUB} is substrate conductivity, A represents inner area of coil, B_C is magnetic field at center of coil, t_{SUB} is the

substrate thickness and ω^2 means angular velocity that contributes to losses with factor of power of 2 [64]. The equation also reflect direct relationship between substrate conductivity and thickness. Taking this into account, the superior performance of SOI (Silicon-On-Insulator) realized WPTs has a logical reason. Additionally, using the lower band of a frequency range also contributes to SAR reduction as a complement to other techniques like including metamaterial, segmentation of an external antenna, etc. [22].

$$R_{SUB,ED} = \frac{\sigma_{SUB} A^2 B_C^2 t_{SUB}}{16} \omega^2. \quad (1)$$

Investigation of the WPT system itself in terms of high-level mathematical description (e.g. effect of basic matching configuration to PTE) to improve the power transfer performance is well extended. However, detailed insight into individual phenomena (eddy current, proximity effect, coupling capacities, density of metal filling, etc.), which affect properties of an OCA-coil working under 500 MHz together with the implementation of suitable layout techniques suffer from a lack of results, where only very few works are aimed at OCA-coil design strategies [22, 59, 62]. All of them agree with the statement that the optimal design of integrated WPT systems depends not only on its structure but also on the external conditions and load, where the initial interest should focused primarily on the transducer design under knowing of $Z_{L(OPT)}$ (see Fig. 1). The known design strategies include:

- Mr. Park et al. [59] suggest to start the process of maximization quality factor Q thought the optimum turn width/space ratio after selection of right number of turns in the horizontal plane that is usually in the range of 1-3 [59], [62].

	[51]	[52]	[53]	[54]	[22], [55]	[56]	[57]
Year	2013	2016	2018	2013	2013, 2015	2017	2016
Application	EH, RFID tag	EH	EH	EH	EH	EH	RFID tag
Frequency [GHz]	1.5	0.95	0.434	5.2	0.16	2.75	0.986
CMOS process	65 nm	45 nm SOI	180 nm SOI	180 nm	130 nm	180 nm SOI	180 nm
EH chip dimension [μm]	500 \times 250	550 \times 700	2000 \times 2000	3200 \times 1500	2000 \times 2180	1600 \times 1600	1500 \times 1500
Distance [mm]	1 (air)	40 (air) + 10 (chicken)	10 (air)	30 (air) + 5 (saline)	2.5 (air) + 7.5 (muscle)	10 (air) + 10 (chicken)	15 (air)
Quality factor	8	NA	14.18	NA	11.05@101 MHz 8.5@160 MHz	NA	20.8
Inductance [nH]	18	NA	7.3	NA	65@101 MHz 90@160 MHz	NA	NA
Output power/ max. efficiency	10.5 μ W@ P_{in} =17 dBm/ -34.5 dB	50 μ W@ EIRP=36 dBm/ NA	138 μ W@ P_{in} =17 dBm/ -21.7 dB*, -25.6 dB	NA@ EIRP=37 dBm/ NA	56 μ W@ NA/ -20.96 dB	1.21 mW@ NA/ -26.46 dB	\approx 1 mW@ NA/ -25.4 dB
Output voltage [V]	0.7	1	1.08	1.15	3.1	1.1	NA

* only link efficiency; RFID - Radio Frequency Identification; SOI - Silicon On Insulator; NA - Not Available

Tab. 2. Selected energy harvesters with on-chip antennas.

- Mr. Zargham et al. [59] implement various methods for Q and L investigation through techniques such as vertical parallelization of metal layers or applying a multi-layer structure depending on specific conditions on the principle of the optimum load. In doing so, Zargham proceeded from the requirement of eliminating a possible additional matching coil (e.g. a part of PI, L matching block, etc.) and targets matching realization (to fulfil the optimum load condition $Z_{L(OPT)}$) only by an on-chip resonant capacitor.
- When the optimum load condition is met, the aim of WPT design is to maximize the mutual inductance of the primary and a secondary coil (maximizing L and Q) while reducing their resistance (maximizing Q but only if the optimum load condition persist inviolate) [22], [62].

As already mentioned, the missing detailed investigation of various OCA-coil designs in sub-500 MHz frequency band can open a new space in the issue of fully-integrated energy harvesters for IMDs. For instance, in the case of GHz frequency and classic approach to coil design (designed for a specific inductor value), the effect of changes into the coil structure are well described and characterized. However, without doubt, one of the main goals of OCA-coil design for energy harvesting is to maximize the inductance, i.e. mutual coupling (or better maximize QL product under the optimum load condition). Besides that, if the MHz frequencies are in interest, the other parasitic effects can become dominant. It has been proven that different techniques (e.g. horizontal and vertical traces tapering, multi-layering, multi-stacking, cutting a wide conductor into slices, techniques for proximity effect reduction and many others) affect the quality, inductance and self-resonance frequencies, and can be used to tune the PTE to its maximum for desired load conditions. Nevertheless, the main question remains: "How much benefits can bring these techniques in EH applications with an OCA-coil and few hundreds of MHz operation frequencies?"

Good early insight into situation can bring these three examples:

1. If we look little bit closer at the issue of OCA-coil structure, the interesting observation has been carried out by Park et al. where careful design of an OCA-coil (e.g. tapering technique) and layout manipulation (H-tree signal distribution) bring very promising experimental results of the PTE about 4% (1 mm air + 10 mm tissue) with possible improvement up to nearly 9% in the case of air as the transfer medium [59].
2. Multilayered turns technique is in general characterized by a high resistance value caused by proximity affect and extremely small distance of stacked (vertically parallel) conductors ($< 1 \mu\text{m}$). In the case of 3-layer conductor configuration, 1 GHz frequency and 20/1 width/space ratio increasing the resistance per length about 50%

has been recorded in comparison to an individual wire and is much significant than the side-by-side configuration [65]. This phenomenon together with the skin effect are even more dominant when a wider conductors are used [66]. Just method of using a wide conductor can be found in many recent publications [22,56,59,62].

3. Most of investigated OCA-coils are based on a simple spiral coil structure. However, it is well known that the symmetrical structure in general can be more beneficial [67], [68]. This observation was proved also for sub-500 MHz frequency band where improvement of Q by about 24%, and L value improvement by 34% were reported [69]. Figure 5 brings additional information about the investigated coil structure in the form of experimental verification, where significant performance degradation is observable compared to simulation results. This is mainly caused by high density of metal coverage (with loop-based nature) and semiconductor active devices in the core of coils that is not the case in the conventional design of specific inductor value in GHz frequency band.

As can be seen from the previous examples, some of the rules copied from the RF inductor GHz design can be valid also for sub-500 MHz frequency band and some of them may raise some doubts requiring a deeper investigation. It is also important to note that using the lower operational frequency and challenging with related issues can bring promising results directly in two individual research branches at the same time. The first one is already discussed OCA-coil-based utilization (power/energy harvesting), while the second one is related to inductor-based utilization in DC-DC on-chip converters (power/energy distribution) [71–74]. Frankly speaking, the targeted research can kill two flies by a single stone.

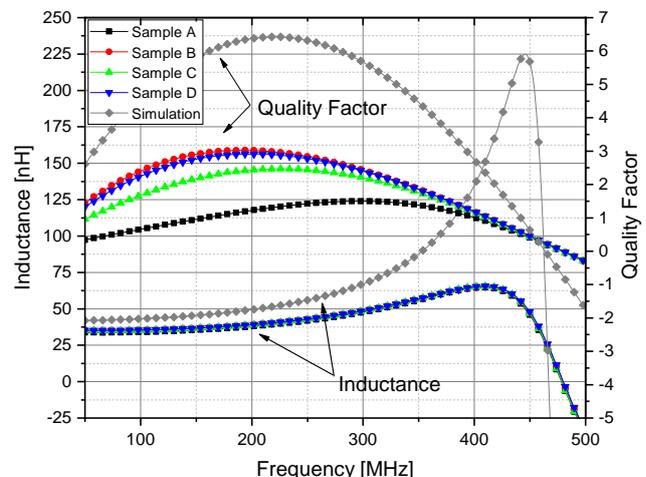


Fig. 5. Performance of a symmetrical OCA-coil for sub-500 MHz frequency band. The layout of the proposed OCA-coil can be found in [70]-Fig. 24.

2.2 Rectifier and PTE

2.2.1 Rectifier

The primary objective of a WPT system (as a part of RFID or energy harvester in general) is the maximization of PTE across physical dimensions of antennas, impedance matching (or an alternative related approach) that varies with load impedance, the distance (or implant depth) between device and external source, and also with environment material [53, 57, 62, 75]. In other words, the PTE is translated into link, matching, driver and rectifier efficiencies covering entire power flow chain (according to Fig. 1):

$$\eta_{TOT} = \eta_{AMP} \eta_{MC,T} \eta_{LINK} \overbrace{\eta_{MC,R} \eta_{REC}}^{\text{regulating rectifier}} \eta_{DC-DC}. \quad (2)$$

On the receiving side directly behind the OCA, the alternative (AC) signal in nature is harvested. Such a signal must be then rectified and modified to suitable voltage value necessary for ensuring reliable operation of the targeted IMD. In general, we have few options how to deal with it, and those can be categorized into three main groups according to functional realization of the rectifier:

1. active, so called synchronous rectification,
2. passive,
 - conventional design without a suppression mechanism of the MOS device threshold voltage V_{TH}
 - design based on suppression mechanism of the threshold voltage V_{TH}
 - implementations using a transformer with a central terminal
 - class-driven design (e.g. E-class rectifier)
3. special, known as a regulating rectifier.

Relatively widespread are active synchronous rectifiers, which use fast comparators and control loops to manage the pass transistors. To our best knowledge, their application for higher frequencies > 100 MHz (expected hunting for ISM 433 MHz realizations failed) and low voltages (in terms of requirements for comparator) WPT systems with high voltage η_{REC-V} and power η_{REC} efficiency seem to be yet unprofitable. Special high-speed comparators are typically characterized by high power consumption (up to hundreds of μ W at frequencies in ones of MHz), relatively high AC input voltage (usually at least 1 V if step-up voltage conversion not included), compensation mechanism for the input offset voltage and loop delay and so on [76–78]. Despite of these unfriendly facts, very promising results of $\eta_{REC-V} = 83\%$ and $\eta_{REC} = 84\%$ at 200 MHz that benefit from using a high-speed comparator with simple mechanism of loop delay and input offset compensation were presented in [79]. Reported self-consumption of 80μ A@200 MHz exhibits acceptable level.

On the other hand, employing the conventional passive rectifiers belongs to the most popular approaches, which

are also feasible for GHz frequencies (all realizations introduced in Tab. 2 employ a passive rectifier) and low voltage conditions. From low voltage point of view, mainly solutions that suppress the effect of the V_{TH} and thus reduce the voltage drop across the rectifier are attractive. The V_{TH} suppression (or precisely said the reducing its effect in MOS transistor control) may be either static or differential (also presented in Sec. 3), and comprehensive overview of the individual principles and their impact can be found in [80]. We only note that one of the most popular principles is the technique using “bootstrap” capacitors. Thanks to this technique, the promising performance even for high frequency applications such as RFID could be possibly achieved [81–85]. For example, in [82], it has been reported 73% @ $f = 950$ MHz of η_{REC} for 0.29 V (1.25 V) input (output) voltage and the load of 50 k Ω . A special technique is floating gate approach that is however incompatible with a standard CMOS process [86], [87]. An alternative may be a quasi-floating gate design technique that exhibits excellent properties ($\eta_{REC} > 66.7\%$ @ $V_{in} = 0.45$ V under 30 k Ω load) and can also be used for high-frequency applications (2.4 GHz in this case) [88]. However, despite of the wide use of passive rectifiers, they suffer from the voltage drop across the rectified diode and also from significant reverse-leakage current (this is not the issue in active rectifiers). This two phenomenons effect the PTE, depending on the input voltage/power on both sides of characteristic. In a lower band, the significant voltage drop is dominant, while in opposite, the leakage issue causes serious problem in the case of increasing the input voltage/power and surprisingly, for decreased frequency (increased time window in which reverse current can flow back into the source) [89]. Therefore, we often see the significant decreasing of PTE on both sides with the cramped optimum point. To achieve a flat PTE curve, the gate-boosting scheme (V_{TH} suppression) has to fulfil the following requirements [88]:

- For input levels smaller than the optimum point, positively boost the effective gate-source voltage of the switches (i.e. decrease the effective V_{TH} of the switches and thus, increase the forward current).
- In the optimum point, preserve the already generated gate voltages, i.e. provide a zero boost in the maximum efficiency point.
- For the input voltages larger than the optimum value, decrease (or negatively boost) the effective gate-source voltage of the switches, i.e. increase the effective V_{TH} and accordingly reduce the reverse leakage current.

We have to also be aware of the voltage amplitude at rectifier input during design phase that can be estimated for RF far-field application under lossless matching circuits [59], [87] as follows:

$$V_{IN} = \sqrt{\frac{(1 - |\Gamma|^2) G_R P_{RAD} \lambda^2}{4\pi} \left(\frac{\eta_{REC}}{\eta_{REC-V}^2} \right) R_{IN,DC-DC}} \quad (3)$$

where individual quantities mean: Γ - reflection coefficient from the antenna terminals, G_R - transmitter antenna gain, λ - medium wavelength, P_{RAF} - radiation density around the receiving antenna, $R_{IN,DC-DC}$ - input impedance of the DC-DC converter or a low dropout voltage regulator. The partial solution to flattening PTE curve can be in using the multi-path rectifier [90] or other mechanism that can adaptively manage above mentioned issues.

Very promising performance in low-voltage applications seems to be rectifiers based on a OCA-coil with central terminal, where implementation in the form of a symmetrical structure is not a serious problem (see Sec. 2.1.2). Such a realization can attacks 80% @ $f = 1$ GHz level of PTE under the input voltage comparable to the V_{TH} of rectifying transistors. However, similarly to the previous designs, after achieving the peaks, there is a significant decrease reported [91]. The last group include all class-driven designs which covers large amount of solutions with own issues that go far beyond the content of this paper. As for the maximization of the integration and inductive near-field power transfer in sub-GHz band, we can mention for example Class-E half-wave zero dv/dt rectifier (labeled as series-L VDR) that can benefit from a weak-coupled inductor and parasitics capacities of rectifier components [92], [93]. Simultaneously, it should be noted that current research of individual class-based solution is primarily focused on high-power applications and therefore, it is too early to discuss their feasibility for low-power μW applications, where many of IMDs belong. Class-E rectifier can be also readily find in many UHF applications.

In general, when the rectifier is implemented as a separate block, WPT system usually needs an auxiliary circuit (DC-DC converter or LDO) that performs two additional functions: 1. modifies the voltage value and its time-domain response behaviour, and 2. can engage in assistance with fulfillment of the optimum load (see Sec. 2.2.2) condition. However, how can be observed from (2), with using the two-stage cascading conversion approach, the total efficiency is degraded much more because of multiplying relationship $\eta_{REC}\eta_{DC-DC}$. For example, if we take quite optimistic values of $\eta_{REC} = 70\%$, $\eta_{DC-DC} = 80\%$ for a rectifier and a DC-DC converter respectively, we get only 56% efficiency. Moreover, bulky energy storage components in DC-DC converters play against the effort of full integration of the harvesting system. To deal with this issue, the work by Kim brings interesting results [61, 94, 95], where the rectifier and regulation process are combined into one block called Integrated Resonant Rectifier-IR³ (Fig. 6). Usage of active rectification in bridge and hybrid pulse modulation control has positive impact not only on the efficiency but also on fast regulation response. The IR³ design reports $\eta_{REC}\eta_{DC-DC}$ up to 60% at 144 MHz that is immediately reflected to the total prodigiously high WPT efficiency reaching up to 5% across 10 mm distance that is, according to our knowledge, probably the best confirmed result so far for low-power application with highly integration requirements, This work demonstrates a great potential of R³ structure that is already wide-spread in many

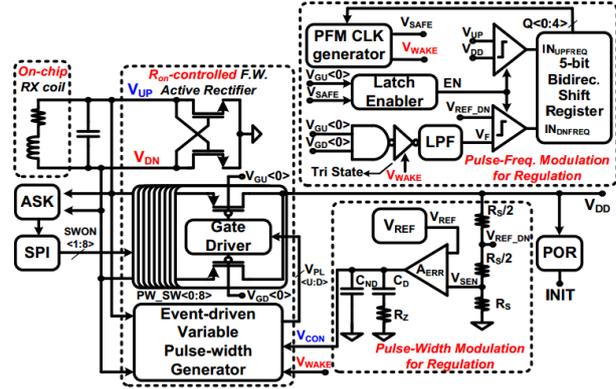


Fig. 6. Hybrid pulse modulation (HPM) with combined pulse-width modulation (PWM) and pulse-frequency modulation (PFM) for integrated resonant rectification and regulation (IR³) [61].

WPT applications [95]. Implementation of energy recycle technique and seamless-voltage/current-mode structures are other unexplored techniques where improvement in the efficiency and low-voltage behaviour can be found without affecting the design compactness or using off-the-shelf external components [96].

2.2.2 PTE Issue

The previous sections were dedicated to particular building blocks of a fully integrated WPT system. Nevertheless, the most significant factor, influencing the total efficiency i.e system level design, has been omitted so far. Since the most preferred approach in the current state of IMD research is near-field technique at the expense of significant deficiencies in far-field power transfer (see Sec. 2.1.1), this section is focused primarily on near-field resonant inductive coupling. However, all the knowledge presented here may be used with some caution for both. Despite the fact that there are some publications dealing with the design of IMDs using near-field resonant inductive coupling, the majority of works are based on system-independent analysis. In other words, only in the last few years, there is a starting trend to distinguish between the efficiency of four basic topologies for a dual-coil system (Fig. 7) with respect to the maximum power transport and maximum power transport efficiency-PTE. Those topologies are: SS topology, PS topology, SP topology, and PP topology, where the first (second) letter indicates the circuit arrangement on the source (load) side: S-series, P-parallel.

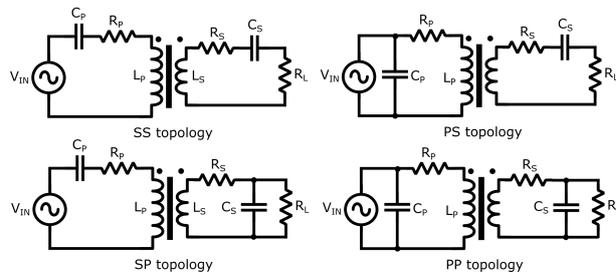


Fig. 7. The most widely used topologies for realization of an on-chip integrated WPT system (inductor-less-capacitor-only matching solution).

It has been shown that for the SP configuration with a high coupling coefficient, the intended maximization of power transport based on the standard resonant condition of the secondary coil can lead to its local minimum [97].

As well a general misconception is that the applying of maximum energy transport theorem, which is based on the mutual matching of input/output impedance (known as impedance matching theorem), also leads to an increase in the efficiency, which is of course not true. The maximum efficiency, in this case, is limited to 50%. Thus, it is clear that system-level optimization is as important as the optimization of individual elements within the transport chain (link, OCA-coil, rectifier, etc.). System-level optimization itself can be realized on the basis of the following requirements:

- maximum power transport efficiency,
- maximum transferred (delivered to load) power,
- targeted compromise between the previous two requirements.

It is important to be aware of these requirements because in many works, only the PTE maximization is taken as the main goal.

In [98], Mr. Guo et al. report analytical expressions of the energy transport efficiency for individual WPT system configurations from Fig. 7. The authors also state that if the standard resonance condition on the secondary side of the WPT system is met, the efficiency expression does not depend on the topology choice on its primary side. However, as been mentioned before, applying a standard resonance condition on the secondary side does not necessarily lead to the optimum solution. Moreover, existence of so-called boundary frequency, above which the SS topology shows higher efficiency than the SP configuration and vice versa, was observed. A comprehensive analysis of SS and SP topologies in terms of the PTE and power transport is given in [97]. This work deals with finding suitable values of C_S and C_P capacitors. An important finding is that the SP topology is limited compared to the SS topology in terms of the maximum power transport to one optimum point (see Fig. 5 and Fig. 9 in [97]). At the same time, the authors provide an optimization-selection tool (figure of merit) for a trade-off between PTE and power transport, which is based on maximizing the weighted amount of the required PTE and the power transferred to load. Finding an optimization-selection tool for the SP topology is also the goal addressed in [99], where the authors utilize the maximized weighted multiplication of the efficiency and the transferred power using standard resonance conditions. The results include an improvement of the PTE from 44% (design for power transfer) to 72.5% (design for a compromise) at the original 90.2% (design for PTE). Similarly, it is also valid in terms of the power delivered to load from 8.8 mW (design for PTE) to 177 mW (design for a compromise) at original 220 mW (design for power transfer). The same team later extended the proposed optimization-selection tool to three-coil and four-coil systems [100].

The great job in the context of making a certain order into quite messy and laborious approaches was done by Mr. Zargham, who introduces consistent theorem of the optimum load/source for maximizing the PTE in a two-coil WPT system that represents very powerful analysis and optimization mechanism [62]. He analyzed inductive-based WPT system as a general 2-port model using scattering (S parameters), admittance (Y parameters), impedance (Z parameters), and hybrid (ABCD parameters) in the presence of two degrees of freedom created by two separated matching circuits (see Fig. 1). This can also be obtained by a multi-coil configuration [101]. The strength is hidden behind the versatility (independence on a chosen WPT topology) and straightforward application where the delivered power under the maximized PTE can be carefully tuned by the two matching circuits. In this way, the four topologies from Fig. 7 can be readily transformed and optimized.

The capacitor-only approach is gaining weight because quality factor of on-chip capacitors such as MIM (Metal-Insulator-Metal) is several times greater than the quality of an on-chip inductor optimized for sub-GHz frequencies. Moreover, the inductor design is also more area-intensive that leads to highly inefficient design. In [102], a capacitor-only L-match approach for simultaneous power transferring to multiple devices was reported. Interested observations were reported in terms of the delivered power, sensitivity to load variation, responsiveness to the cross coupling, etc. In [62], Zargham brings very useful analysis by the investigation of parasitic effect of an additional matching component in L-match topologies that are preferred to be used in situations, where the quality factor of the matching network is not enforced and efficiency is of the primary concern. He derived generally valid formulas but his attention was focused mainly on SP-based topology i.e stepping-up impedance conversion at the source side and stepping-down at the load side (looking from load to source) as the most often scenario. This work also brings meaningful observation about the maximum ratio between $\text{Re}\{Z_L\}$ and $\text{Re}\{Z_{L(\text{OPT})}\}$ to $\approx 21\times$ (Fig. 1). This ratio is dedicated to a situation about increasing requirements on the matching capability of the rectifier input impedance $\text{Re}\{Z_L\}$ in the case of not to significantly breach the condition of 1-stage implementation under the optimum load condition. In terms of restriction on single capacitor-only matching, fully on-chip integration of a WPT system and the optimum load condition, approximate equality between the parasitic series resistance of coils R_s on the receiving side and load $\text{Re}\{Z_L\}$ should be respected. It is very important to note that this equality is valid only under conditions of a weak-coupled WPT system when losses in the transfer medium can be neglected and high Q capacitor is expected to be used. If this is not ensured, detailed information published in [62] should be taken into consideration.

In addition to what has been said so far, the finding and adaptively mapping Z_L impedance to $Z_{L(\text{OPT})}$, introduced also challenging area with a deeply anchored method in tuning the input impedance of a DC-DC converter varied by the

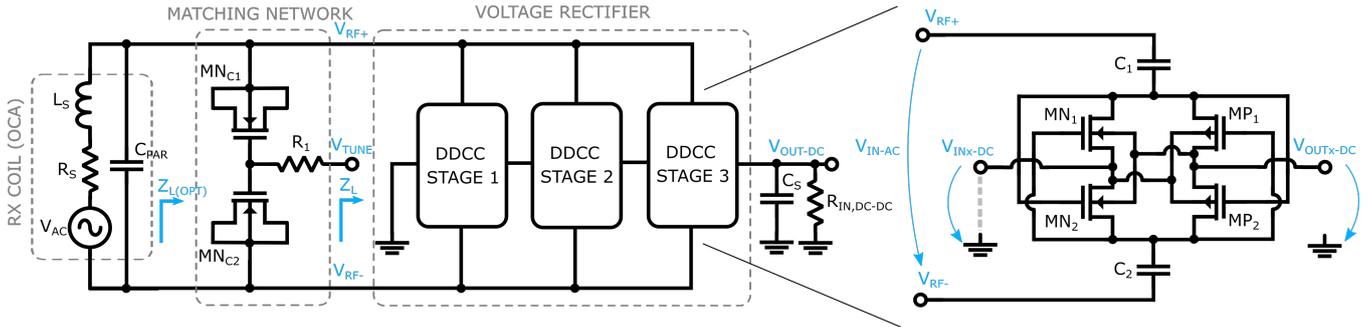


Fig. 8. Circuit diagram of the proposed WPT receiver.

maximum power point tracking (MPPT) algorithm [7]. The adaptively-varied input impedance of a DC-DC converter is then transferred across the rectifier to Z_L . As an alternative, Q-Modulation technique [103] or other techniques that directly and suitably adjust Z_L to the extracted maximum power into the load, can be employed. However, one has to be always aware of the fact that the nonlinear rectifying element also generates currents and voltages at the harmonics of the input frequency, and although in this case, the output is in DC domain, the efficiency of the rectifier can be modified by terminating the harmonics. For these reasons, the small-signal analysis used in tradition-fashion can result in false estimation. To overcome this nuisance, usually harmonic balance methods are used for this purpose under numerical investigation [104]. In some cases (e.g. an ideal rectifier), methods like harmonic linearization in conjunction with Fourier analysis can be also employed to derive an analytical formula reflecting frequency behaviour of the input impedance [105]. In [59], a formula based on η_{REC} and η_{REC-V} parameters was used for investigation of effect of Z_L on the WPT performance. One can also find useful conclusions in [106] saying that "to maximize the power transfer and the amount of harvested power, the matching network must be designed to convert the small-signal input impedance calculated when input port is biased at the peak of input signal".

3. WPT Design Example

This section presents an example of WPT design with the fully integrated receiving part (rectenna – rectifying antenna) consisting of an OCA-coil (introduced in Sec. 2.1.2), where a weak coupling is expected and therefore, the low-voltage operational capability of the rectifier was taken as priority. Through performed research, a differential drive cross-coupled (DDCC) CMOS bridge rectifier was found to be effective topology to deal with the low input voltage/power issues [89, 107–110].

The aim of the proposed rectifier was to further improve the performance of the DDCC rectifier topology for very low values of the input voltage. This was achieved by compensating the effect of threshold voltage V_{TH} of all the switching transistors. To improve the parameters of the

rectifier from [89], the body-biasing technique is applied to NMOS transistors in addition to PMOS devices, as shown in the core cell depicted in Fig. 8 [111]. This has been made possible by the use of triple-well NMOS transistors in the design. By compensating V_{TH} of NMOS transistors, utilizing the generated DC voltage as the body-bias voltage, the performance of the rectifier is expected to improve also for very low values of the input voltage. It was shown in [111] that this topology provides an increase in the output power if compared to the topologies presented in [89], [107]. The negative effect of the proposed approach is a reduced PTE at higher values of the input power that is caused by excessive bias voltages reflecting to increased leakage and reverse currents, and therefore also increased loss. This rectifier stage forms the basis of the proposed receiver presented in this paper.

3.1 Proposed Receiver Architecture

The circuit diagram of the proposed receiver is depicted in Fig. 8 [112]. The RX OCA-coil inductance, quality and self-resonance frequency were modelled based on the previously measured samples. Capacitor C_{PAR} together with two variable capacitors MN_{C1} and MN_{C2} form the parallel resonance capacitance – a part of the impedance matching circuit. These circuit elements were optimized to achieve the resonance frequency of 200 MHz with the tuning voltage of around 250 mV. The rather large total span of the tunable capacitance allows us to adjust the rectifier input voltage depending on the receiver input conditions. This is done by tuning the resonator, if the input signal is weak, and detuning it, if the input signal becomes too strong. This ensures that the rectifier operates close to the optimum conditions.

Three rectifier stages are cascaded to provide the desired value of the output voltage (multiplication effect). This is done by connecting the DC input $V_{IN(x+1)-DC}$ of the next stage to the DC output $V_{OUTx-DC}$ of the previous one. The other part of the impedance matching is realized by the series input capacitance of the rectifier stages. Capacitor C_S serves to smooth the output voltage V_{OUT-DC} . A more detailed description of the receiver including simulation results can be found in [112].

The receiver was designed and manufactured in a standard 130 nm CMOS technology, as part of an experimental prototype chip. The design of the RX OCA-coil was based on our work previously published in [69]. The final layout of the receiver, with its main parts highlighted, is depicted in Fig. 9. The total RX OCA-coil area is $1.16 \text{ mm} \times 1.16 \text{ mm}$. There are other circuits included in the area of the coil, as it was manufactured as part of a shared prototyping chip. These might have adverse effects on the OCA-coil performance, most notably increasing its parasitic capacitance and losses caused by eddy currents in crammed center (refer to degradation performance in Fig. 5).

3.2 Measurement Results

To facilitate measurement of the manufactured samples, the transmitter side of the WPT system has to be implemented as well. For this purpose, four versions of transmitter TX coils were implemented, based on the methods presented in [62], [113], with two coil sizes and two matching circuit topologies. A more detailed description of the TX coil and impedance matching design can be found in [114].

To minimize the influence of parasitic properties of a IC package on the measurement, bare die samples were used for the measurements. This necessitated the chip bonding to a small PCB that serves as a carrier. We also considered the possible effect of the chip seal ring on the RX OCA-coil. The seal ring forms another conductive loop around the RX OCA-coil and therefore, it has a negative effect on its parameters. To investigate this further, we prepared two versions of the samples to be evaluated. One includes the original chip as it was manufactured. The second version uses a modified version of the chip, which has the seal ring broken. This was achieved by a careful chip cutting at a sufficient distance from RX circuitry in order to avoid the chip damage. Photographs of the two sample versions are shown in Fig. 10.

So far, only preliminary measurement data is available. The measurement setup is not yet fully developed, therefore, the reported parameters are not final. Several problems arose during the building the measurement setup, mainly related to the bonding process and the TX coil tuning. These will be investigated further in the future. Nevertheless, the basic functionality of the system has been demonstrated.

Figure 11 shows the output voltage $V_{\text{OUT-DC}}$ and the output power $P_{\text{OUT-DC}}$ of the WPT system as a function of the rectifier load $R_{\text{IN,DC-DC}}$ obtained by measurement for three different generator output power levels. Thus far, only one sample with the broken seal ring was evaluated, where the TX coil with the outer diameter of 24 mm and two-component matching network were used.

The maximum achieved $\eta_{\text{MC,T}}\eta_{\text{LINK}}\eta_{\text{MC,R}}\eta_{\text{REC}}$ efficiency in this measurement was 0.05%. This is rather poor performance if compared to previously published works, e.g Kim's work in [95] or works in Tab. 2), where the peak efficiencies of up to 5% and around 1% were reported, respectively. Even

if we factor in the different RX OCA-coil areas, the performance is below expectations. Reasons of poor performance are still under investigation but it is likely due to poor tuning of the TX coil, resulting in the operating frequency shift from 200 MHz to 165 MHz. Likely, a redesign of the various PCBs used in the measurement setup will be needed in the future.

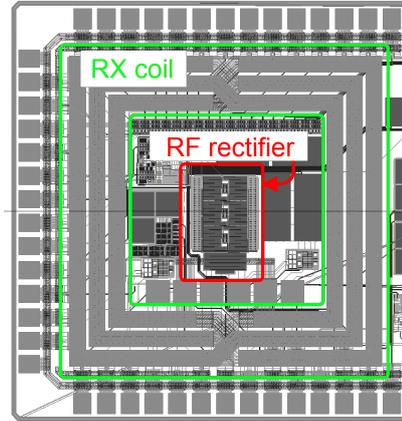


Fig. 9. Layout of the proposed RF wireless receiver. The area between the receiver coil (placed between the green rectangles) and the rectifier (placed inside the red rectangle) is filled by other circuits of the shared prototype chip.

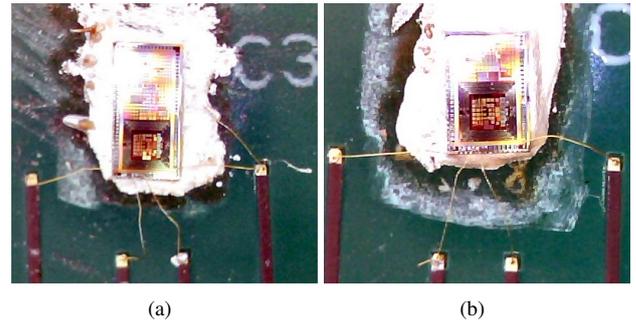


Fig. 10. Photographs of measurement samples: whole chip (a), chip with broken seal ring (b).

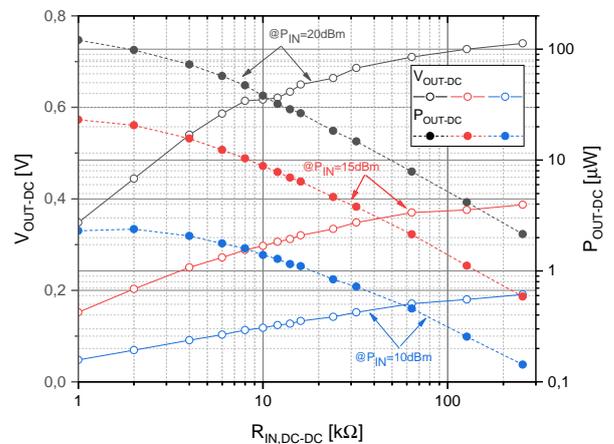


Fig. 11. Preliminary measurement results using the TX coil with 24 mm diameter and a sample with broken seal ring at TX to RX distance of 10 mm: rectified output voltage (left y-axis), output power (right y-axis) of the receiver as a function of load resistance (x-axis).

4. Conclusion

Despite of the selected restrictions in long-distance energy transferring at the presence of loss-hungry environments such soft tissue is, the electromagnetic (EM) WPT can draw benefits from ad-hoc design in IC design phase without additional postprocessing steps needed, except for still present packaging/encapsulation process. Packaging can immediately influence the reliability, safety and cost. For this highly attractive reasons, challenges and problems that have to be solved within the design of a fully-integrated WPT system suitable for IMD applications are addressed in this paper. It has been shown that energy harvesters based on EM principle and fully realized in lossy silicon suffer from many issues that strictly limits their wider use. However, at the same time, it has been shown that they are still drifting in potential to be competitive with getting more and more popular alternatives as for example, ultrasound energy transferring that is dominant in brain monitoring and stimulating IMDs. To overcome current weaknesses of an on-chip EM WPT system, particularly present in standard IC processes, the area of interest in the future research should take into account the following observations: 1. needed for biocompatible and biostable high ϵ_r materials for IC chip package/encapsulation, 2. deeper investigation of parasitic effect on OCA-coils in hundreds of MHz frequency band, 3. higher attention on the effective design of a regulated rectifier for near-field resonant inductive coupling with improved low-voltage behaviour, 4. future high efficiency EM WPT system in presence of near-field and especially, high lossy tissue should be designed for the optimum source/load theorem rather than the matching theorem (limited to 50% efficiency), 5. searching for novel and alternative solutions such as promising implementation of a booster antenna [63] or MIL implementation discussed in Sec. 2.1.1. Finally, we have to emphasize that information about individual system blocks present in this paper is strictly limited to fully on-chip WPT systems directly implemented on the IC chip in the meaning of clear SoC concept (especially for hundreds of MHz frequency band). In other words, e.g. if SiP approach is feasible or GHz frequency provide healthy conditions, the implementation of bulky active and high Q-passive components open additional amazing possibilities in the research field, which plays the major role in highly efficient design of EM WPT systems.

Acknowledgments

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