

An Automated ESD Model Characterization Method

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Abstract. *Novel automated simulator-independent ESD model characterization method based on Differential evolution and Nelder-Mead Simplex algorithms is presented in this paper. It offers an alternative for time and human-resources demanding manual characterization that is still widely used. The paper also presents stable macro-models of the four most often used snapback-based protection devices in CMOS technologies, i.e., NMOST and three variants of silicon-controlled rectifier structure. These macro-models were used for evaluation of the proposed method and the results are included and discussed.*

Keywords

ESD, automated model calibration, differential evolution, Nelder-Mead simplex, I-V characteristic

1. Introduction

Electro-static discharge (ESD) has presented serious problem for integrated circuits reliability and lifetime since the first steps on a field of high integration. Energies that may be transferred during this relatively short event can completely destroy sensitive analog or digital blocks within an integrated circuit (IC) if this phenomenon is not taken into account during every phase of the design. It was demonstrated that more than 30% of IC production is lost due to ESD damage which in total costs the electronics industry almost 6% of total revenue [1].

To increase IC robustness against ESD events, full-chip protection design has to be carefully integrated. Introduction of special models that are able to describe behavior of a protection device during ESD event may substantially decrease number of iterations necessary for full-chip ESD protection system design to be refined. Many research teams are presenting different approaches of ESD protection devices modeling based on different techniques, but all of them are using traditional manual characterization methods [2–4]. These methods require number of specific measurements to be performed, thus increasing demand on dedicated specialists and total characterization time. In most of the cases,

the measurements require all terminals of a protection device to be connected to external pads which increases systematic error of the measurements as all those pads shall be always protected by ESD protection devices that add parasitics into the measured device terminals. The characterization process is then iterative work of manual “tuning” of the calibration (or often called fitting) parameters.

Our goal is to create automated characterization method able to calibrate physical macro-models to available quasi-static transmission-line pulse (TLP) or better to exponential-edge TLP (EETLP) data that better reflect transient properties of characterized devices [5–7]. The used optimization algorithm have to be effective in non-continuous objective-function space with numerous penalty factors used. This criterion is met by differential evolution (DE) which was in past proven to be very effective and robust in global optimum search tasks [8], [9]. We also incorporated Nelder-Mead Simplex algorithm (NMSA) to the final stage of the optimization task to solve one of the shortcomings of the DE algorithm, i.e., slow convergence rate in the end of the optimization process [10]. As an automated ESD model calibration approach driven by DE algorithm was to the best knowledge of the authors never published before, special care had to be taken in terms of convergence properties of the calibrated macro-models to ensure that the calibration process is not misled by convergence difficulties.

In current state of the research, the main focus was put on improvement of macro-model calibration quality – overall optimization time is not currently important as it only consumes CPU time. Model scalability and temperature and statistical effects were omitted in this work.

Novel automated simulator-independent ESD model characterization method is presented in this paper along with four case studies: characterization of single-finger drain-extended medium-voltage ESD NMOST using standard TLP data and low-voltage-triggered silicon-controlled rectifier (LVTSCR), modified lateral silicon-controlled rectifier (MLSCR), and basic silicon-controlled rectifier (SCR) using piece-wise linear data based on HBM measurements (TLP data for those devices are not available).

This paper is organized as follows: Section 2 introduces the reader to Differential Evolution and Nelder-Mead

Simplex algorithms which are essential part of the proposed characterization method. Section 3 sheds some light on the most often used ESD protection structures characterization methods: TLP and HBM. In Sec. 4, novel automated characterization method itself is described in detail, Section 5 summarizes the characterization setup including hardware and software used for the task and presents used ESD protection macro-models along with the characterization results for several different protection structures. In Sec. 6, a conclusion is drawn along with the next direction of the research.

2. Optimization Algorithms

Very basic introduction to both DE and NMSA algorithms is presented within this section. For more information, see [11] and [12] publications from the creators of the algorithms.

2.1 Differential Evolution Algorithm

Evolutionary optimization algorithms are in general very robust and fast-to-converge algorithms. They are less susceptible to fall into local optimum as in case of standard gradient-based optimization algorithms (hill-climbing, Tabu search, etc.). Thanks to the natural selection of the most fitted member of the population of parameter vectors, the possibility of the premature convergence in a local minimum is minimized [11]. Moreover, the DE is in contrast with gradient-based optimization methods able to optimize in non-continuous objective-function-space and enables the designer to introduce for example penalty coefficients to detect optimization violations.

The functionality of DE algorithm can be described in the following way: let the vector of system parameters for specific member of the specific generation be designated as

$$\mathbf{x}_{i,G}, \quad i = 0, 1, \dots, NP - 1 \quad (1)$$

where NP is a number of D -dimensional parameters in the parameter vector (D doesn't change during optimization process) and G determines the sequence of the generation. All the parameter vectors $\mathbf{x}_{i,G}$ of the same generation are called *population*. If the initial values of parameters within the parameter vector are unknown, their values can be generated randomly using uniform probability distribution. After each generation, new parameter vector (population member) is generated and is used in next iterative step. It is derived as a weighted difference of the first and the second member and then summed with the third member. If the newly created parameter vector yields lower value of the objective function than a previous "best" population member, the new member replaces the former "best" one. In addition, the best fitted member of the population (i.e., the parameter vector with lowest objective function) is stored to keep track of the progress of the optimization process.

The detailed principle of generation and selection of the best fitted member of the population is as follows: for each parameter vector $\mathbf{x}_{i,G}$, a trial vector \mathbf{u} is calculated as

$$\begin{aligned} \mathbf{u}_i &= \mathbf{x}_{r_1,G} + F \cdot (\mathbf{x}_{r_2,G} - \mathbf{x}_{r_3,G}), \\ i &= 0, 1, \dots, NP - 1 \end{aligned} \quad (2)$$

where integers $r_1 \neq r_2 \neq r_3 \neq i \wedge r_1, r_2, r_3 \in \langle 0, NP - 1 \rangle$ are randomly chosen with uniform probability distribution, F is a real weighting constant determining the influence of the differential variation vector $(\mathbf{x}_{r_2,G} - \mathbf{x}_{r_3,G})$. The role of the trial vector can be seen in Fig. 1.

To implement the principle of a mutation and crossover, the new D -dimensional vector \mathbf{t}_i needs to be created. The elements of the \mathbf{t}_i vector are random numbers with uniform probability distribution, where $t_{i,j} \in \langle 0, 1 \rangle$, $j = 0, 1, \dots, D - 1$. Now, each element $t_{i,j}$ of the \mathbf{t}_i vector is compared against the value of CR crossover coefficient and in case the value of CR is higher than $t_{i,j}$, the $u_{i,j}$ is placed in the crossover vector \mathbf{v}_i as j -th element, else the original value $x_{i,j,G}$ is used. In addition, the dimension index j is compared against randomly generated integer $R = 0, 1, \dots, D - 1$ with uniform probability distribution and in case of match, $v_{i,j} = u_{i,j}$. This can be mathematically described as

$$v_{i,j} = \begin{cases} u_{i,j}, & t_{i,j} \geq CR \vee j = R \\ x_{i,j,G}, & \text{otherwise} \end{cases}, \quad j = 0, 1, \dots, D - 1. \quad (3)$$

The graphical representation of (3) is shown in Fig. 2.

The final step is to solve objective function for the crossover vector \mathbf{v}_i and compare its value against the value of objective function of the original vector $\mathbf{x}_{i,G}$. The vector with lower objective function becomes the new member of $(G + 1)$ -th generation, mathematically written as

$$\mathbf{x}_{i,(G+1)} = \begin{cases} \mathbf{u}_i, & f_{\text{obj}}(\mathbf{u}_i) < f_{\text{obj}}(\mathbf{x}_{i,G}) \\ \mathbf{x}_{i,G}, & \text{otherwise} \end{cases}, \quad i = 0, 1, \dots, NP - 1 \quad (4)$$

where $f_{\text{obj}}(\mathbf{y})$ represents the value of the objective function for \mathbf{y} vector in its argument. After each generation, the best member (the one with the lowest value of the objective function) is selected and stored for the next generation. This ensures the progress of determination of the best set of parameters. The algorithm can be repeated indefinitely, until the ideal solution is found, or the maximum number of generations can be specified to limit the number of iterations of the optimization.

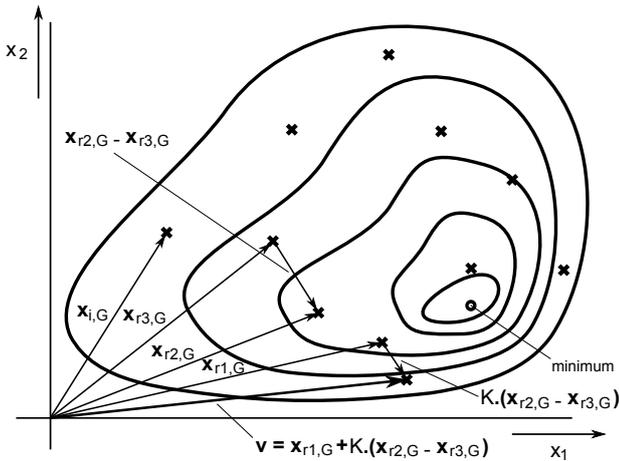


Fig. 1. Representation of the differential evolutionary algorithm.

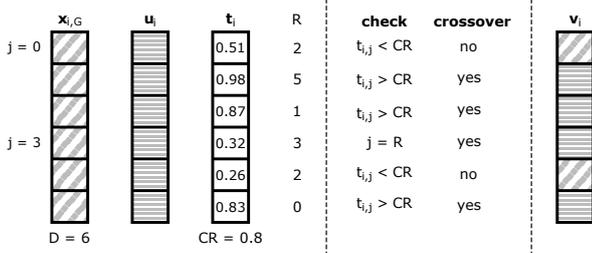


Fig. 2. Example of the crossover process.

2.2 Nelder–Mead Simplex Algorithm

The NMSA, developed in early 60s, was designed to be effective in solving standard unconstrained optimization problems. Like DE, the NMSA is not gradient-based optimization algorithm. The optimization method is based on comparison of the functional values of endpoints (*vertices*) of a general polyhedron (*simplex*) accompanied by adaptation of the simplex to the objective function surface – or *landscape*.

Initial polyhedron is defined during random generation of $D + 1$ vertices. The $(D + 1)$ -dimensional polyhedron or simplex covers the whole parameter space. Each vertex is called by its index that also easily identifies which vertex has better value of the objective function as the indexes are sorted by their objective function value. Three transformations of the polyhedron are defined: reflection, contraction and expansion (see [12]). Each of those transformations changes position of an arbitrary vertex (usually the one with the worst value of the objective function) in such a way that all the vertices move towards the global optimum which will very probably be eventually reached.

3. Transmission-line Pulse and HBM

Transmission-line pulse (TLP) is a modern approach to characterize ESD protection designs. It was presented in 1985 in [13]. In contrast with the component-level ESD models like Human Body Model (HBM) or Charged-device Model (CDM) whose output is only an ESD withstand voltage level, the TLP can provide much more information to the designers about various properties of a specific ESD protection device. It allows measurements of the high current I-V characteristics point-by-point and thus making understanding of the processes inside the protection circuits much more easier. Illustrative scheme is shown in Fig. 3 and equivalent circuit of the TLP machine with simplified principle of I-V characteristic compilation procedure are shown in Fig. 4.

In a TLP tester, a transmission line is charged by the high-voltage generator, disconnected from it, and discharged into the device-under-test (DUT) pad while the supply or ground pads are connected to the TLP tester ground creating short current pulse forced to the DUT. Pulse width can be varied by choosing different length of the coaxial cable (approx. 10 ns per meter for a 50Ω cable). The transmission line has its impedance at the opposite end matched by a polarized load to the characteristic impedance of the transmission line to prevent reflections of the pulses. The pulse waveform has much steeper edges than for example the HBM pulse. This is caused by a distributed capacitance of the transmission line making the rise time lower than 2 ns [14]. Also, in contrast with HBM pulses whose waveforms are of RC shape, pulse of TLP is due to a distributed nature of the transmission line shaped like square wave presenting quasi-static part in the waveform. Measurements are done in this quasi-static part of the pulse. The raw output of single TLP measurement is a set of pair values – voltage across the DUT and current through the DUT. The current waveform doesn't

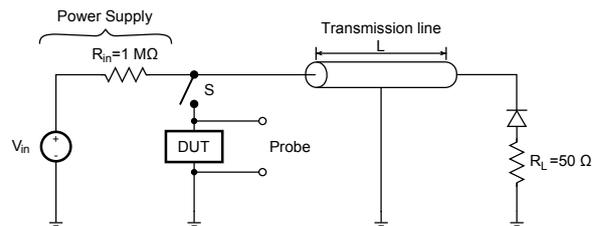


Fig. 3. Illustrative schematic of TLP machine.

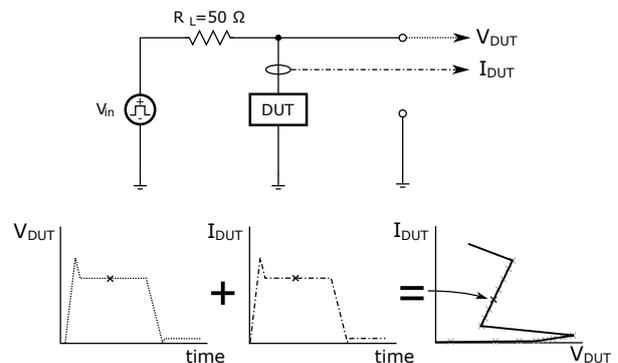


Fig. 4. Equivalent circuit and principle of I-V char. composition.

have to be captured, the current in the steady-state region can be calculated (based on the knowledge of the characteristic impedance) as

$$I_{DUT}(t) = \frac{(V_{in} - V_{DUT}(t))}{R_L} \quad (5)$$

where R_L is the characteristic impedance of the coaxial cable.

The final I-V characteristic is then simply a set of current versus voltage points derived in given number of TLP measurements.

3.1 Obtaining I-V Characteristics Using HBM

Possibility of utilizing HBM tester to obtain I-V characteristics was suggested in [15]. In principle, when both current through and voltage across the ESD protection device is being captured during an HBM stress test, it is possible to ascertain approximate values of the most important regions of the ESD protection I-V characteristics, i.e., trigger V_{t1} and snap-back (holding) V_{sb} voltages and on-state resistance R_{on} .

The major differences between TLP and HBM IV characteristic capturing methods are:

1. Necessity to measure both transient voltage and current of the protection due to undefined impedance of the IC or probe fixture and high voltage source which would otherwise link those two quantities together,
2. Absence of quasi-static portion of the TLP in HMB pulse that would allow precise capturing of transient voltage and current and also enables time averaging to further refine the final IV characteristics.

The first point can be addressed simply by using two dedicated probes, the second by performing several measurements and averaging the results before compiling the final IV characteristics.

Figure 5 shows transient voltage and current through an ESD protection DUT measured using two-pin HBM method described in [15]. After both curves are aligned accounting for different time delays between voltage and current probes, final I-V characteristic is shown in Fig. 6.

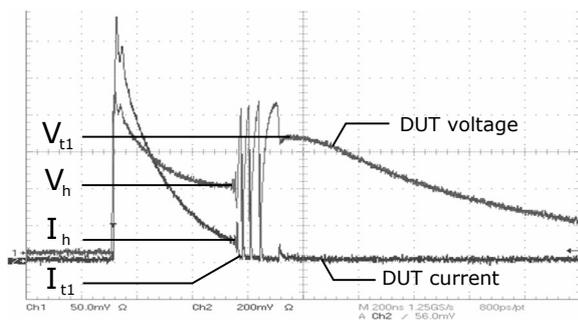


Fig. 5. Transient voltage and current through DUT obtained by HBM ([15]).

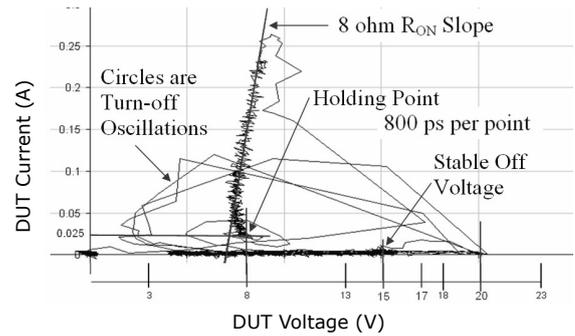


Fig. 6. Final DUT I-V characteristic measured by HBM pulse ([15]).

4. Proposed Characterization Method

As mentioned in the introduction section, proposed approach needs only the measured I-V characteristic of the protection device obtained by for example TLP or EETLP measurements, instead of a set of different manual measurements for many different conditions that needs to be performed during standard ESD model characterization method. Proposed method is basically based on curve fitting of a characterized model to a template I-V characteristics. During optimization process, so called *fitting parameters* of the characterized model are being iteratively modified by the algorithm. Quality of the fitting is then measured by so called *objective function*. Its minimization is done by differential evolutionary algorithm designated as *DE/rand/1/bin* and by Nelder-Mead Simplex algorithm in the final stages of the calibration process.

Both used optimization algorithms were implemented in Matlab programming language and executed by Octave which is GNU alternative of proprietary Matlab software. Octave was chosen because it can be easily implemented in industrial environment. The core scripts used for calibration process control and for interfacing between simulator and graphs plotting is also executed by Octave. All interfaces are modular, thus the method is not coupled with any specific simulator (even though it was primarily designed for MM-SIM simulator) and it should be possible to use it with any commercial or in-house circuit simulator provided that it can be launched and controlled via a command line.

To make optimization process more effective and robust, specific *fail-safe checks* were implemented. To prevent from infinite optimization loops, maximal acceptable value of objective function is defined which whenever is reached, the optimization process is interrupted and the best achieved set of parameters is reported as optimal. To the same purpose serves also definable maximum number of iterations which causes termination of the optimization process in case that acceptable objective function value can not be reached. Additionally, detection of simulator misconvergence was implemented to rule out parameter sets that prevents simulator from circuit evaluation.

Prior to the automated model calibration process, fitting parameters of the model have to be defined along with their upper and lower bounds. This is used to limit overall parameter space and increase speed of the process. The calibrated model must be instantiated in the simulation netlist which is then used during calibration process (see for example Fig. 8). During calibration process itself, each parameter set (i.e., specific generation member in the evolution process) calculated by DE is written into the model library that also includes the model being calibrated. The netlist simulation is performed and the objective function value is calculated and compared to the best achieved in earlier runs. This cycle continues by standard DE scheme until one of the fail-safe checks is triggered and the optimization process is successfully finished. In case that DE algorithm performed too much iterations and none of the fails-safe checks criteria has been satisfied, it is highly probable that DE algorithm is no longer effective [10] and thus Octave-embedded Nelder–Mead Simplex function is launched and tries to further improve current best result. This measure was implemented due to very low convergence rate if DE was used without NMSA. See calibration method flow diagram in Fig. 7 (action highlighted in gray are performed by external simulator).

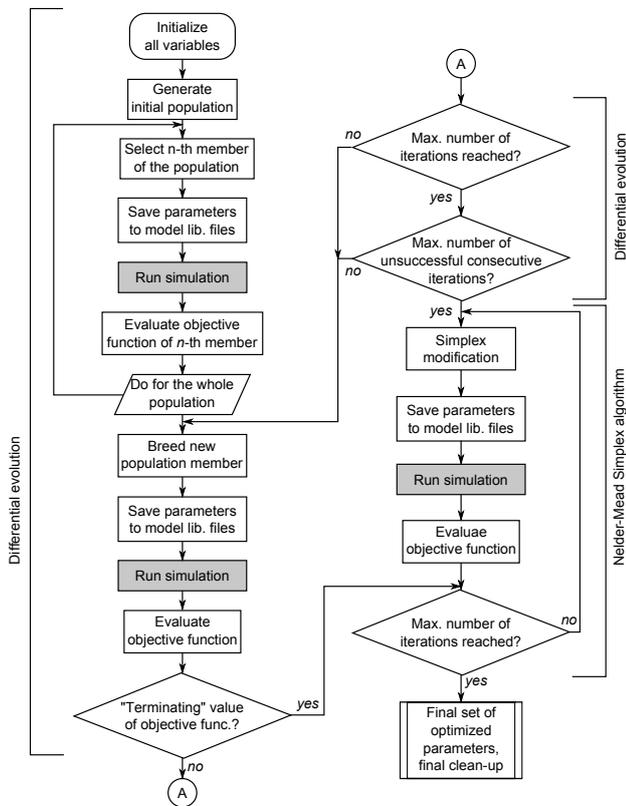


Fig. 7. Flow diagram of the presented optimization process (action highlighted in gray are performed by external simulator).

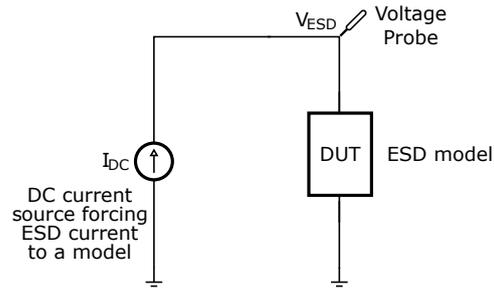


Fig. 8. Schematic of the DC simulation circuit for ESD model optimization; ESD device designated as Device under test (DUT).

5. Device Models and Results

Presented automated ESD model characterization method was tested on four basic types of bulk-silicon technology ESD protection devices: single-finger drain-extended medium-voltage ESD NMOST, low-voltage-triggered silicon-controlled rectifier (LVTSCR), modified lateral silicon-controlled rectifier (MLSCR), and basic silicon-controlled rectifier (SCR). A logic flavor of 110 nm technology was used for NMOST case study due to the fact, that it is currently the only available technology equipped with TLP measurements. SCR-based ESD protection structures were implemented using in-house 180 nm logic flavor bulk CMOS process as SCR devices are rarely available in third-party PDKs. Operation of all selected devices is based on so called *snap-back* – phenomenon that forms region with negative differential resistance in the I-V characteristic. This presents major problem due to instabilities during simulations. Great care was thus taken during selection of proper type of device models. As devices based on SCR structure are currently being introduced into the in-house technology and no TLP measurements are yet available, those macro-models were calibrated on piece-wise linear data extracted from manual measurements using HBM pulse. Only NMOST macro-model was calibrated to available TLP data.

Characterization setup was comprised of the Octave 3.0.5 executing developed tool and Cadence MMSIM 10.1.1 circuit simulator, running on quad-core based PC with 6 GB RAM using 64bit Linux OS. In all case studies, parameters of DE were set as follows: population size $NP = 1000$, crossover factor $CR = 0.9$, weighting factor $F = 0.68$. Calibrated macro-models use large number of fitting parameters, that is the reason for such a high population size – the target was sufficient optimization sub-space coverage, overall computation time is unimportant in current development state.

A new objective function was developed – *Weighted-Root-Mean Square Deviation (WRMSD)*. It is defined as

$$f_{obj} = \sqrt{\frac{\sum_{i=1}^n (f_w[i] \cdot (V_{meas}[i] - V_{sim}[i])^2)}{n}} \quad (6)$$

where V_{meas} and V_{sim} are measured and simulated voltage vectors respectively and f_w is a vector of weighting function with the same dimensions as the V_{meas} and V_{sim} vectors. This weighting vector is used to emphasize specific parts of I-V characteristic, e.g., precise fit in breakdown and trigger regions is more important than on-state resistance in on-state region or current leakage in off-state, i.e., large deviation of calibrated model in the trigger region is penalized compared to the off-state leakage. This countermeasure was implemented to prevent quantitatively better but qualitatively worse calibration results which was observed especially in case of ESD NMOST macro-model where in terms of objective function calculation relatively insignificant regions of trigger and snap-back those deviated largely from TLP measured data if no penalization was done.

All devices were netlisted in the same simulation netlist (Fig. 8) and during calibration, DC simulation was used sweeping anode/drain current to get an I-V characteristic.

Each case study ESD protection structure – drain-extended MV ESD NMOST, SCR, MLSCR, and LVTSCR – will be presented in following paragraphs along with physical structure, description of used macro-model and final characterization results. Additionally, to verify that no convergence problems occur if a device is instantiated in a larger circuit, complete digital I/O circuit equipped with both input and output signal paths was designed in both CMOS technologies used. The input signal path consists of a Schmitt trigger circuit, I/O-to-core voltage domain digital level-shifter, and digital buffers; output path of a core-to-I/O voltage domain digital level-shifter, open-drain NMOST driving circuit with selectable high-impedance state and a buffer chain feeding the open-drain NMOST. Core logic is simulated by a combinational logic of approx. 20 gates. 4 kV HBM transient pulse is used as a stimulus of the I/O circuit – which is fully powered and operational – and is applied on the I/O input (pad) of the digital I/O circuit. Transient response of each case study macro-model instantiated in such an I/O circuit to the HBM pulse will then be plotted. Scheme is shown in Fig. 9.

5.1 Drain-Extended NMOST Macro-Model

The robust, fast, reliable yet relatively simple ESD protection device is an NMOST. It can be used directly in a pad with grounded gate (GGNMOST) or as a dynamic power clamp in a pad-ring. Its drawback is large layout area consumption, especially in deep sub-micron technologies where ESD devices can't benefit from smaller geometrical features as their size is dictated by robustness required. Significant inherent parasitic capacitance thus complicate its use in radio-frequency (RF) I/Os.

Simplified structure of a single-finger ESD NMOST with extended non-salicided drain with parasitic bipolar structure and relevant resistances highlighted is shown in Fig. 10.

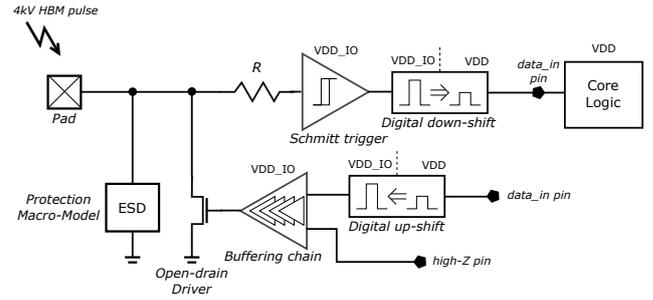


Fig. 9. Scheme of the digital I/O circuit for demonstrating correct convergence properties of calibrated macro-models.

Macro-model used for evaluation is based on macro-model presented in [16] and comprises of appropriate technological n-channel BSIM MOST core, n-type three-pin VBIC BJT model simulating parasitic NPN structure formed of drain and source n+ diffusions and p- substrate, substrate resistance and diffusion resistance on a drain side (often used improvement of ESD MOSTs having *non-salicided drain extension*). Complete macro-model is shown in Fig. 11.

The core n-channel BSIM model (version 3.24) is in fact already part of the process design kit (PDK) and majority of its parameters is already correctly characterized by model engineers or process development team. Only three parameters needs to be re-characterized to properly model substrate current. The second most important part of the model is n-type BJT modeled by VBIC model. VBIC is able to model collector-base breakdown by impact ionization and is thus used as second part of substrate current model. The MOST part of the substrate current can be described as

$$I_{\text{sub}}^{\text{MOS}} = \alpha \cdot V_{\text{DSeff}} \cdot \exp\left(\left(\frac{\beta}{V_{\text{DSeff}}}\right) I_{\text{dsa}}\right), \quad (7)$$

$$V_{\text{DSeff}} = V_{\text{DS}} - V_{\text{deff}}, \quad (8)$$

$$\alpha = \alpha_1 + \frac{\alpha_0}{L_{\text{eff}}} \quad (9)$$

where V_{deff} is the effective drain–source voltage, I_{dsa} is the drain current without considering impact ionization, L_{eff} is the effective channel length of the MOST, and α_0 , α_1 , and β_0 are the three n-channel BSIM model substrate current fitting parameters. Second part modeled by the collector-base impact-ionization breakdown model of VBIC BJT can be described as

$$I_{\text{gc}}^{\text{BJT}} = I_{\text{tot}} A_{\text{VC1}} V_{\text{bci}} \exp\left(-A_{\text{VC2}} V_{\text{bci}}^{\text{mod}}\right)^{M_C - 1} \quad (10)$$

where I_{tot} is total leakage current through the base-collector junction, $V_{\text{bci}}^{\text{mod}}$ is built-in potential of base-collector junction diminished by voltage drop across the junction, M_C is junction gradient coefficient, and A_{VC1} and A_{VC2} are fitting parameters. Total current is then just a sum of $I_{\text{sub}}^{\text{MOS}}$ and $I_{\text{gc}}^{\text{BJT}}$.

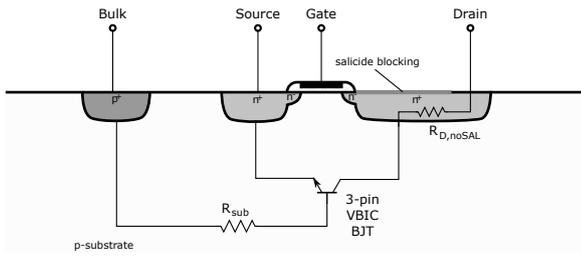


Fig. 10. Simplified structure of single-finger ESD NMOST with non-salicided drain.

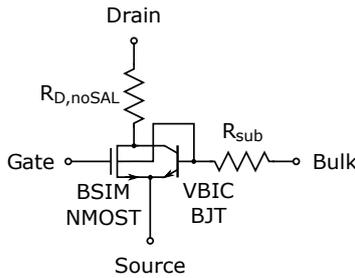


Fig. 11. Scheme of NMOST macro-model.

Parameter	TLP Measured Data	Calibrated Macro-Model
V_{t1}	8.73 V	8.12 V
V_{sb}	6.65 V	6.49 V
R_{on}	2.12 Ω	6.01 Ω

Tab. 1. ESD parameters comparison between measured characteristics and fitted macro-model of ESD NMOST.

Different approach was presented in [17] where dedicated variable current source is used to model the substrate current. On the other hand, this independent current source can very easily cause convergence difficulties during complete system simulations and is problematic for implementation due to the fact that it requires value of V_{dsat} which is not accessible model parameter and would have to be calculated externally.

Remaining parts of the macro-model are substrate resistance that is modeled as linear lumped voltage and temperature independent resistor (fitting parameter R_{sub}) and technological diffusion resistor modeling drain extension of the ESD NMOST that is defined by the dimensions of the NMOST device (length is equal to the length of the extension and width to the width of the ESD NMOST) – this resistor is also part of the standard PDK and does not have to be characterized.

The ESD NMOST macro-model is fitted against TLP measurements of I/O GGNMOST in 110 nm logic flavor CMOS process. Total number of fitting parameters is 33: three for NMOST substrate model, one for each substrate and drain diffusion resistance models and 28 for VBIC bipolar transistor model. Weighting function f_w was used to put emphasis on breakdown and trigger regions (low-current part). Total characterization time was approx 28 hours including final NMSA optimization which improved the final result by approx. 20%. Final value of the objective function is 1.18. See comparison of TLP and calibrated model I-V characteristics in Fig. 12. Table 1 summarizes the most important points on the I-V characteristics comparing measured data to calibrated. Figure 13 shows a response of the ESD NMOST macro-model instantiated inside a digital I/O circuit to 4 kV HBM pulse (both voltage and current though the protection).

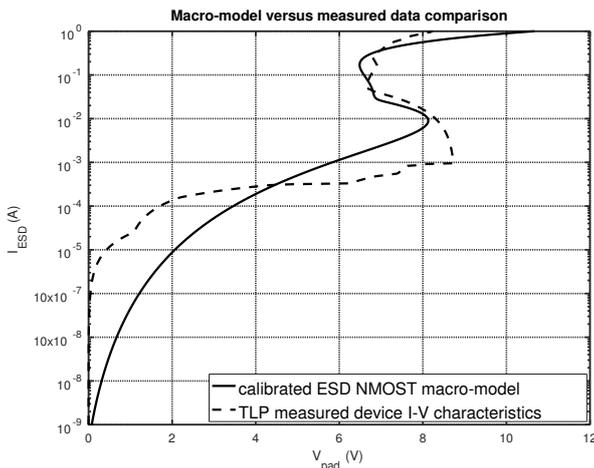


Fig. 12. Final results of ESD NMOST macro-model calibration (calibrated macro-model in solid line, calibration data in dashed).

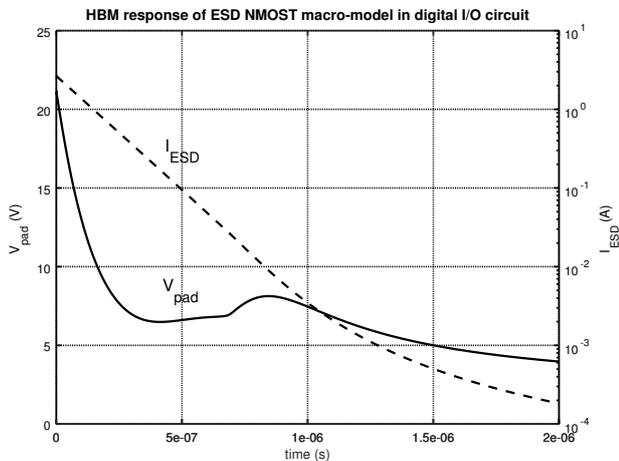


Fig. 13. 4 kV HBM pulse response of the ESD NMOST macro-model instantiated inside digital I/O circuit.

5.2 SCR Macro-Model

The Silicon-Controlled Rectifier (SCR) ESD protection devices are based on usually unwanted effect in CMOS technology – latchup. During latchup the CMOS pair consisting of NMOST and PMOST transistors placed physically close to each other begins to conduct when external current is forced to one of diffusions and continues to conduct even though the initial stimuli ended. This effect occurs due to dual parasitic bipolar structures – naturally formed in the CMOS pair – that enter active mode that is sustained by self biasing by the flowing current. In core circuits, the latchup is extremely dangerous because the current conducted through transistors of CMOS pair may fatally damage them rendering the cir-

circuit inoperative. Latchup may be prevented in several ways, most often by inserting guard rings between the transistors of the CMOS pair or by their physical separation. In contrast with internal circuits, the SCR-based protective structures are carefully designed, so they can be stressed by high currents repeatedly without fatal damage [18]. Main advantage of SCR over the MOST-based ESD protection devices is very small area it occupies thus presenting very small parasitic capacitance to protected signal path.

Enhanced macro-model presented in [19] is used as test-case model for SCR characterization. It comprises of three-pin VBIC n-type BJT model, standard SPICE Gummel-Poon (SGP) p-type BJT model, substrate and n-well resistance models. See Fig. 15.

For SCR models, correct modeling of impact ionization breakdown of NPN base-collector junction is essential. Thus, advanced VBIC model is used instead of standard SPICE Gummel-Poon (SGP) model. Equation 10 describes the impact ionization current during breakdown of collector-base junction. Parameters A_{VC1} and A_{VC2} are again used as fitting parameters. This new approach replaces external variable current source used for impact ionization substrate current modeling in many papers [17], [20]. Even though widely used in the case of NMOST model, the current source causes convergence difficulties during simulations.

Both substrate and n-well resistances are modeled as linear lumped voltage and temperature independent resistors (fitting parameters R_{sub} and R_{nw}) as in case of NMOST macro-model. Majority of static VBIC and SGP BJT parameters is used as fitting parameters.

The SCR macro-model is fitted against HBM measurements of device fabricated in in-house 180 nm CMOS process. Total number of fitting parameters is 49: 28 for VBIC BJT transistor model, 19 for SGP BJT model and two for substrate and n-well resistance models. Weighting function f_w was not used (constant value equal to one). Total characterization time was less than 19 hours including final NMSA optimization which improved the final result by approx. 20%. Final value of the objective function is 1.52. See comparison of template piece-wise linear and calibrated model I-V characteristics in Fig. 16. Table 2 summarizes the most important points on the I-V characteristics comparing measured data to calibrated. Figure 17 shows a response of the ESD SCR macro-model instantiated inside a digital I/O circuit to 4 kV HBM pulse (both voltage and current though the protection).

Parameter	HBM Measured Data	Calibrated Macro-Model
V_{r1}	19.47 V	18.43 V
V_{sb}	2.06 V	3.54 V
R_{on}	6.65 Ω	4.70 Ω

Tab. 2. ESD parameters comparison between measured characteristics and fitted macro-model of ESD SCR.

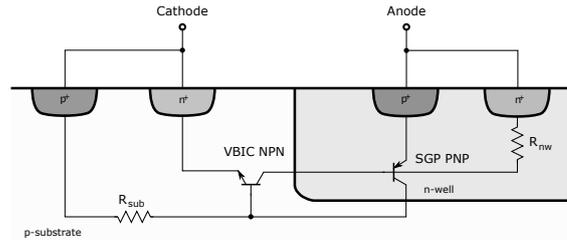


Fig. 14. Simplified structure of SCR.

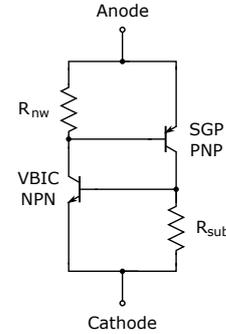


Fig. 15. Macro-model of SCR and MLSCR.

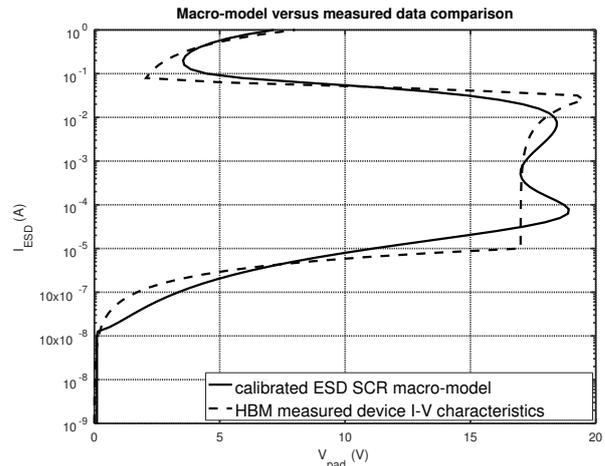


Fig. 16. Final results of ESD SCR macro-model calibration (calibrated macro-model in solid line, calibration data in dashed).

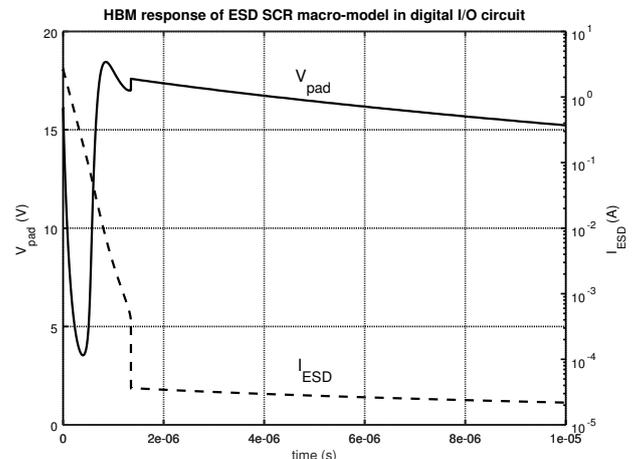


Fig. 17. 4 kV HBM pulse response of the ESD SCR macro-model instantiated inside digital I/O circuit.

5.3 MLSCR Macro-Model

MLSCR is basically a modification of the original silicon-controlled rectifier (SCR) amended by *bridging diffusion* of n+ type (see Fig. 18). This simple modification decreases reverse-breakdown voltage of original junction consisting of low-doped n-well and p-well. The decreased breakdown voltage of the junction is also decreasing breakdown and trigger voltages of the whole MLSCR and thus making it usable in broader spectrum of applications than original SCR with high trigger voltage.

The small layout modification described in previous paragraph also means that the macro-model of MLSCR is formally identical to the one used for SCR in previous section (see Fig. 15). Only the I-V characteristic shows differences that can be reflected by changes of values of some of the macro-model fitting parameters. Total number of fitting parameters is thus the same as in case of SCR, i.e., 49: 28 for VBIC BJT transistor model, 19 for SGP BJT model and two for substrate and n-well resistance models. Weighting function f_w was also not used in case of MLSCR. The MLSCR macro-model is fitted against HBM measurements of device fabricated in in-house 180 nm CMOS process. Total characterization time was less than 15 hours including final NMSA optimization which improved the final result by approx. 54%. Final value of the objective function is 0.73. See comparison of template piece-wise linear and calibrated model I-V characteristics in Fig. 19. Table 3 summarizes the most important points on the I-V characteristics comparing measured data to calibrated. Figure 20 shows a response of the ESD MLSCR macro-model instantiated inside a digital I/O circuit to 4 kV HBM pulse (both voltage and current through the protection).

Parameter	HBM Measured Data	Calibrated Macro-Model
V_{t1}	14.98 V	14.10 V
V_{sb}	2.56 V	1.41 V
R_{on}	5.95 Ω	7.79 Ω

Tab. 3. ESD parameters comparison between measured characteristics and fitted macro-model of ESD MLSCR.

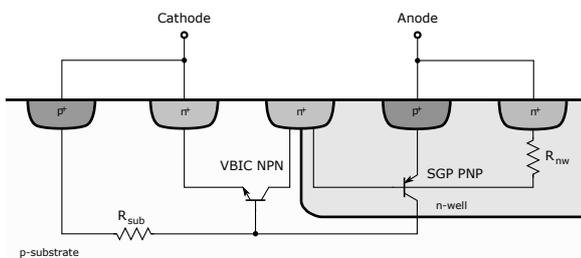


Fig. 18. Simplified structure of MLSCR.

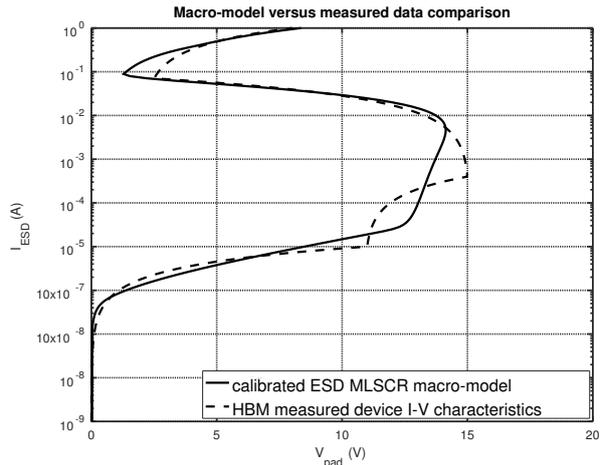


Fig. 19. Final results of ESD MLSCR macro-model calibration (calibrated macro-model in solid line, calibration data in dashed).

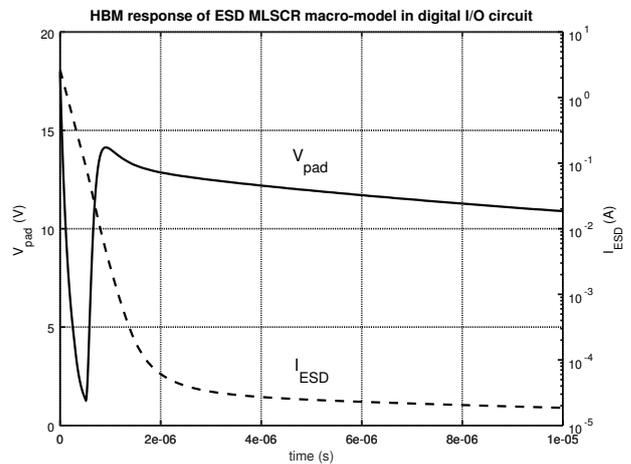


Fig. 20. 4 kV HBM pulse response of the ESD MLSCR macro-model instantiated inside digital I/O circuit.

5.4 LVTSCR Macro-Model

Further decrease of breakdown and trigger voltages was a motivation for another enhancement of the SCR structure that would make it ideal for use as ESD protection device in low-voltage RF pads that are very sensitive to overall parasitic capacitance. Instead of bridging diffusion, whole single-finger NMOST is used to help triggering the embedded SCR structure thus moving the ESD operational window close to voltage levels used in modern low-voltage circuits. See the structure of LVTSCR in Fig. 21.

Used macro-model comprises of four-pin VBIC BJT that models not only the n-type but also the p-type transistor (as parasitic structure). This substantially decreases total number of fitting parameters in comparison with standard approach and should not negatively influence the modeling precision. Macro-model also includes already characterized BSIM NMOST model from a standard PDK with extended drain modeled as lumped diffusion resistance (also part of

the standard PDK) and linear lumped voltage and temperature independent resistors modeling substrate and n-well resistances (fitting parameters R_{sub} and R_{nw}). Substrate current that triggers embedded NMOST is modeled identically to ESD NMOST described in Sec. 5.1. See (7) and (10) for MOST and BJT parts of the total substrate current that is sum of both contributions. See Fig. 22 for macro-model topology.

The LVTSCR macro-model is fitted against HBM measurements of device fabricated in in-house 180 nm CMOS process. Total number of fitting parameters is 33: three for NMOST substrate model, two for substrate and n-well resistance models and 28 for VBIC bipolar transistor model. Weighting function f_w was not used. Total characterization time was 21 hours including final NMSA optimization which improved the final result by approx. 2%. Final value of the objective function is 0.74. See comparison of template piece-wise linear and calibrated model I-V characteristics in Fig. 23. Table 4 summarizes the most important points on the I-V characteristics comparing measured data to calibrated. Figure 24 shows a response of the ESD LVTSCR macro-model instantiated inside a digital I/O circuit to 4 kV HBM pulse (both voltage and current through the protection).

Parameter	HBM Measured Data	Calibrated Macro-Model
V_{r1}	10.91 V	11.32 V
V_{sb}	2.53 V	2.30 V
R_{on}	5.64 Ω	5.83 Ω

Tab. 4. ESD parameters comparison between measured characteristics and fitted macro-model of ESD LVTSCR.

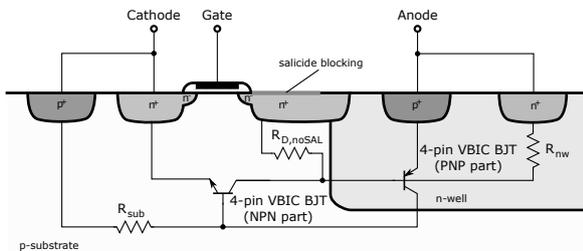


Fig. 21. Simplified structure of LVTSCR.

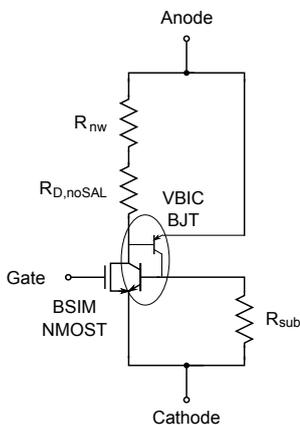


Fig. 22. Macro-model of LVTSCR.

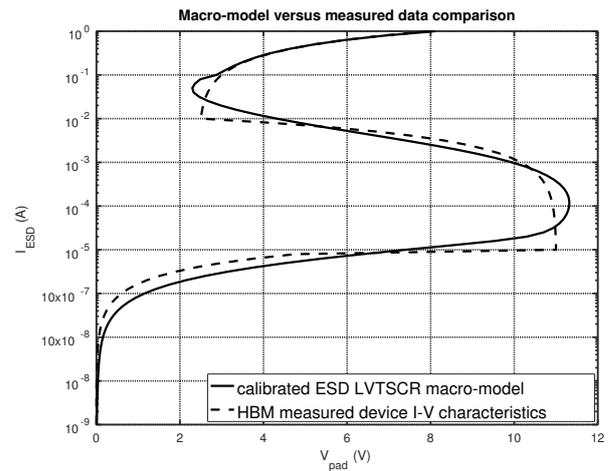


Fig. 23. Final results of ESD LVTSCR macro-model calibration (calibrated macro-model in solid line, calibration data in dashed).

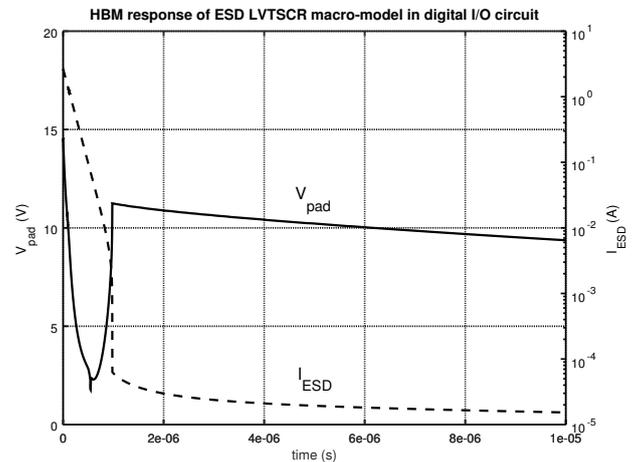


Fig. 24. 4 kV HBM pulse response of the ESD LVTSCR macro-model instantiated inside digital I/O circuit.

6. Conclusion

Presented novel automated simulator-independent ESD model characterization method was successfully verified by four different case studies (characterization of single-finger drain-extended medium-voltage ESD NMOST, SCR, MLSCR, and LVTSCR macro-models). Characterization time seems to be high but considering that only the approx. 1-hour lasting TLP measurements and 10-minutes long initial setup requires work of an engineer, this method is more effective regarding human resources than the traditional manual approach.

Characterization results of NMOST show higher differences between measured data and model characteristics than in case of models calibrated to piece-wise linear data. Authors consider this an issue of the used core NMOST model (BSIM ver3.24) because several consecutive attempts to improve calibration of the macro-model were made with

different parameter bounds setup and initial conditions but in all cases the final value of the objective function was very close to one presented in Sec. 5 and final I-V characteristics were close in shape. This indicates that obtained values of the fitting parameters are most probably very close to the best achievable.

The usage of BSIM ver4 for LVTSCR/NMOST modeling was suggested in [21]. This newer version of Berkeley MOST model includes advanced effects such as drain-induced barrier lowering (DIBL) and substrate-current induced body effect (SCBE) that may increase overall precision of the macro-models. Unfortunately, as the proposed characterization method depends on characterized core models of MOSTs, not having any PDK using BSIM ver4 MOST models available, authors were unable to verify this theory.

As stated in the first section, used ESD macro-models are not equipped neither with technological corners nor temperature effect and in current state of research are not scalable (do not reflect changes in structure dimensions). Based on authors' experience, absence of temperature effects does not present any issues for industrial use of the models and the method itself as characterization and validation of ESD structures are done at room temperature only. Implementation of technological corners would be very problematic due to considerable effort required and more importantly the added value would be questionable as by authors' experience, the properties of ESD structures changes only negligibly due to process variation. Scalability of the models is a future goal for the authors as this enhancement would make system-level ESD design more effective and robust.

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