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STŘEDOEVROPSKÝ TECHNOLOGICKÝ INSTITUT VUT

NEW NANODEVICES FOR ELECTRONICS - FABRICATION AND CHARACTERIZATION

NOVÉ NANOPRVKY PRO ELEKTRONIKU – PŘÍPRAVA A CHARAKTERIZACE

DOCTORAL THESIS
DIZERTAČNÍ PRÁCE

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ABSTRACT

This work proposes a technique for fabrication of a self-ordered nanostructures for electrical applications. The devices were prepared by anodic oxidation in two lengths and three different heat treatments. The structural characterization using SEM, TEM and EDX technics, respectively, were evaluated from structural and material point of view as well. The unique root structure of the highly self-ordered nanocolumn arrays was evaluated and compared after three different heat treatments: as anodized, vacuum annealed and air annealed, respectively. The possible crystallographic orientation of the columns was not observed, however the nano-crystallites under the root structures were found.

The electrical study about the devices shown resistive switching behavior (RS), diode like behavior and a capacitive coupled diode like behavior as well. The active surface, from RS point of view, for the switching mechanism is at the top of the nanocolumns and the gold top electrode. The Schottky barrier height of the Ti/TiO_2 interface was calculated with two methods, and it was lower than 1,11 eV for all three devices.

KEYWORDS

TiO_2, anodic oxidation, resistive switching, Schottky barrier height, nanocolumn, alumina

ABSTRAKT

Táto práca sa zaoberá technikou výroby samousporiadaných nanoštruktúr pre elektrické aplikácie. Prototypy boli pripravené anodickou oxidáciou v dvoch dĺžkach a tromi rôznymi tepelnými úpravami. Štrukturálna charakterizácia bola spravená pomocou techniky SEM, TEM a EDX a vyhodnotenie nielen z štrukturálneho, ale aj z materiálového hľadiska. Jedinečná koreňová štruktúra samousporiadaných nanotyčiniek bola vyhodnotená a porovnaná po troch rôznych tepelných úpravách: po anodizácii, po vákuovom žíhaní, a po žíhaní vo vzduchu. Všetky prototypy obsahujú nanotyčinky s amorfnou štruktúrou, ale našli sa však aj nanokryštály pod koreňovými štruktúrami.
Elektrická charakterizácia prototypov ukázala: odporové spínacie správanie (RS), diódové charakteristiky a charakteristiku podobnú pre diódy s kapacitorom. Aktívny povrch pre spínací mechanizmus je v hornej časti nanoštruktúr na rozhraní nanotyčiniek a zlatej elektródy. Výška Schottkyho bariéry na rozhraní Ti / TiO2 bola vypočítaná dvoma spôsobmi a pre všetky tri zariadenia bola nižšia ako 1,11 eV.

KĽÚČOVÉ SLOVÁ

TiO_2, anodická oxidácia, odporové spínanie, Schottkyho bariéra, nanotyčinka, oxid hlinitý

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DECLARATION

I certify that the work presented in this thesis was performed independently, under the supervision of doc.Ing. Jaromír Hubálek Ph.D., and is original with the sole exception of the technical literature and other sources of information that are acknowledged in the text and reference list, and that the material has not been submitted, in whole or in part, for a degree at this or any other university.

Brno ....

(Ing. Marian Márik)

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Contents

INTRODUCTION

In 1965, Gordon E. Moor said about the semiconductor manufacturers, they had been doubling the density of components on integrated circuits periodically every second year. His prediction, commonly known as Moor's law, has been fulfilled in the last fifty years. [1.] According to the current state of art, that paradigm eventually comes to the end in the next 5 or 15 years. Instead of the focus just on the size reduction, the electronic industry should emphasis more on the increasingly capable devices. [2.]

The common available memory devices were mostly based on transistor oriented electronic design, which is not limited just with decreasing size and basic laws of physics, but also with suitable combination with passive elements. Introduction of a new passive element, called memristor, could be improving the performance of digital circuits. [2.] Main advantage of the memristors is their ability to save information. The memristor is able to ”remember” the last state before the power is switched off.

Since May 2008, when the research laboratory of Hewlett Packard published the first experimental memristor (Strukov et al., The missing memristor found, Nature Letters [3.]), the interest ain the resistive and memristive research suddenly increased. Based on the state of the art of the memristor technology, the possible way to realize a commonly usable resistive memory is extremely wide. Using an oxide-based multilayers is one of the feasible directions.

This essay is dealing with fabrication and characterization of metal/oxide/metal devices with expected resistive switching abilities, which are basics of memristors for non-volatile memory applications.

The first part of this study is dealing with the fundamental theoretical knowledge about memristors, briefly from mathematical background through the current state of the art continuously to the deeper introduction of the titanium dioxide (TiO_2) based resistive memories. The second part of the thesis is oriented on the practical works and experimental results. The fabrication is focused mainly on the TiO_2 nanostructures, prepared, and modified with electrochemical processes. The electrical characterization of prepared structures is discussed as well.

1 STATE OF THE ART

Smaller, faster, cheaper, and simpler structure – these four requirements are determining the direction of the memory development. In last three decades the progress in the traditional memory technology and storage systems was enormous. The requirements for the systems with higher performance and larger capacity are increasing; however, the energy consumption and the space requirements should be lower and lower.

These above-mentioned facts motivated the researchers to find another way, how to fulfill requirements with existing technology possibilities. This resulted strong innovation in the current memory technology and it has also motivated for a development of alternative memory technologies as well.

Among several potential candidates for alternative memory technology, memristors have been recognizing as a viable option due to their simple physical structure, scalability potential and reliable characteristics. The possible answer for question of the 21st century was found in the past at the beginning of the 70's.

1.1 Memristors and resistive switching

In the last 150 years, the known fundamental passive elements were limited to capacitor [C], resistor [R], and inductor [L]. In 1971, Professor Leon Chua at the University of California, Berkley published an underestimated paper about the fourth basic passive element. However, the idea was great, the technology in the 20th century was not enough developed. [4.][5.]

The ,,re-invention,, of the memristors is boiled together with the name Strukov and the HP laboratory, where the first physical model was born and published. The number of the researches and the researchers dealing with memristors exponentially raised. In last 12 years. However we are usually speaking about the memristor oriented research, the difference between the memristors and the memristive switching has to be declared.

The memristor is a two-terminal component with non-linear electrical characteristics, linking magnetic flux and charge, presented in Figure 1.1. [4.]

The resistive switching is a phenomenon observed at devices, which are changing their resistance based on the applied potential / current and when the power is off, the resistance state will not change back.

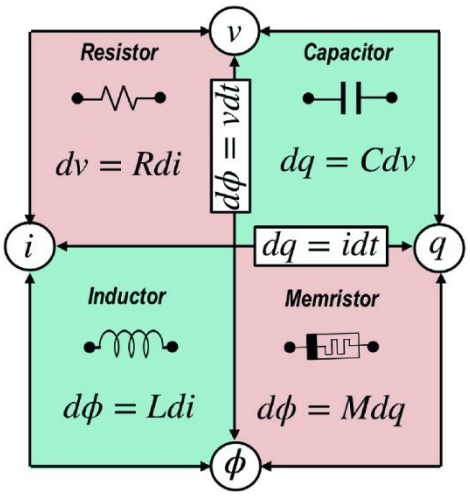


Figure 1.1.: The extrapolated conceptual symmetry between the non-linear resistor, non-linear capacitor, non-linear inductor and the forth possible passive fundamental non-linear element, the memristor. [4.]

1.1.1 Memristors from the mathematical view

From the circuit-theoretic point of view, Chua published the relationship between the four circuit quantities – voltage, current, charge and magnetic flux – which are define by the three basic two-terminal elements (C, R, L). [2.],[5.] Six possible combinations of relationship can be deduced for these circuit variables.

The relationship between the charge and the current is given by the equation 1, and the one between flux and voltage is described by the equation 2. Three other relationships are written by the axiomatic definition of the resistor (equation 3), capacitor (equation 4) and of the inductor (equation 5). [5.]

$$q(t) = \int_{-\infty}^{t} i(\tau)d\tau \tag{1}$$

$$\varphi(t) = \int_{-\infty}^{t} v(\tau)d\tau \tag{2}$$

$$dv = Rdi \tag{3}$$

$$dq = Cdv \tag{4}$$

$$d\varphi = Ldi \tag{5}$$

The functional relation between the charge and the flux from the logical and the axiomatic point of view is possible only with a new two-terminal element (equation 6) which is characterized by □-q curve. The new element was titled memristor [M]. [3.][5.]

$$d\varphi = Mdq \tag{6}$$

The first physical model of memristor was published by HP research laboratories in 2008. This device was a metal oxide metal multilayer controlled by the current. The differential form of the current controlled memristor for circuit analysis is written in equations 7 and 8 [4.],

$$v = \mathcal{R}(w)I \tag{7}$$

$$\frac{dw}{dt} = I \tag{8}$$

where w can be a set of state variables and R and f can be in general explicit functions of time. The simplest way to explain how the memristor works is to consider a thin sandwich film of metal – semiconductor – metal (see Figure 1.2). The semiconductor layer with thickness D is placed between two metal contacts. The specialty of this semiconductive layer is the nonhomogenous concentration of the dopants. Because of this fact, the total resistance is considered between the two metal contacts for the full-length D and it is determined by two resistors in series.

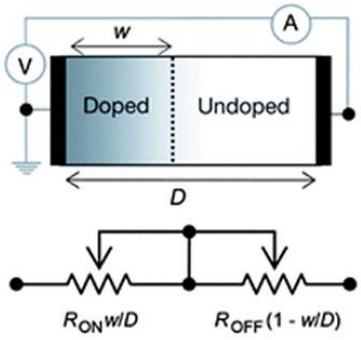


Figure 1.2: The diagram of the memristor with a simplified equivalent circuit. [3.]

The higher dopant concentration causes lower resistance, the lower dopant concentration causes higher resistance. The applied external bias voltage v(t) across the device can move the boundary between the doped and undoped region. The equations for governing of memristance of a thin semiconductor film were obtained using the models in Figure 1.3 and considering the simplest case of ohmic conduction and linear ionic drift in a uniform field with an average ion mobility μ_v:

$$v = \left(R_{on}\frac{w(t)}{D}R_{off}\left(1-\frac{w(t)}{D}\right)\right)i(t) \tag{11}$$

$$\frac{\mathrm{d}w(t)}{\mathrm{d}t} = \mu_v \frac{R_{on}}{D} i(t) \tag{12}$$

which yields in the following formula for *w(t)*:

$$w(t) = \mu_v \frac{R_{on}}{D} q(t). \tag{13}$$

By substituting eq.13 in eq. 11, we obtain the memristance of the system, which for the case Ron << Roff is simplified to:

$$M(q) = R_{off}\left(1-\frac{\mu_v R_{on}}{D^2}q(t)\right). \tag{14}$$

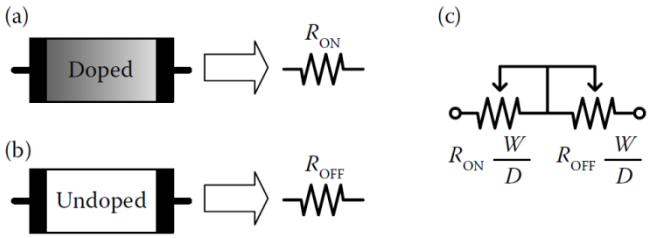


Figure 1.3: Memristor in ON state (a.) and in OFF state (b) with the equivalent circuit (c.). [2.]

1.1.2 Memristors: the emerging memories- type of memristors

Since 2008 memristor became a synonym for the non-volatile memories (NVM). The question, if the non-volatile memories are really memristors or not, will be discussed later. For better understanding why it is important to deal with NVMs and what is the current situation in this field, the types and the basic principles of the NVMs are introduced at first. [6.]

The research in non-volatile memories in the last few years rapidly rises. More and more companies are trying to substitute classical volatile memories as DRAMs, SRAMs or non-volatile NOR-Flashes and NAND Flashes. The main disadvantage of the SRAM and DRAM memories is their volatile character. If the power is turned off, they lose the stored information. At non- volatile Flash memories the information is stored even the power is turned off, but they are limited with amount of read/write cycles and with read/write speed. The new emerging memories are intended to fix disadvantages of above-mentioned memories. The basic comparison of conventional and emerging memories is shown in Table 1 [7.]

Table 1.: The basic comparison of conventional and emerging memories.

	Volatile memory		**Non-volatile memory**		**Emerging non-volatile memory**			
Type	SRAM	DRAM	NOR-FLASH	NAND-FLASH	MRAM	PRAM	FRAM	RRAM
Cell elements	6T	1T1C	1T	1T	1(2)T1R	1T1R or 1D1R	1T1C	1T1R or1D1R
Cell elements					Magneto-resistance	Phase-change	Polarization-change	Resistance-change
Minimum cell size	$140F^2$	$6F^2$	$10F^2$	$5F^2$	$20F^2$	$4.8(4)F^{2b}$	$22F^2$	$4F^{2c}$
Write/ Earse time	0.3ns/ 0.3ns	<10ns/ <10ns	1ms/0.1ms	1ms/ 0.1ms	10ns/ 10ns	20ns/ 50ns	10ns/ 10ns	5ns/5ns
Endurance (cycles)	$>3x10^{16}$	$>3x10^{16}$	$>10^5$	$>10^5$	$>3x10^{16}$	10^8	10^{14}	$>10^{10}$
Application	Cache	Main memory	Storage	Storage	Storage	Storage	Storage	Storage/ Main memory

There are several types of new non-volatile memories, but most of them exist only on laboratory level. The most common classification of emerging memories is based on the phenomenon which allows data storage without external power:

- Ferroelectric RAMs (FRAMs),
- Magnetic or Magnetoresistive RAMs (MRAMs),
- Phase-change RAMs (PRAMs),
- Resistive RAMs (RRAMs)

- Electrochemical metallization memories (ECM)
- Programmable metallization cell memories (PCM),
- Carbon nanotube (CNT) memories,
- Millipede memories
- Molecular memories,
- Nano-crystal floating gate FLASH memories,
- DNA memories.

From above mentioned memory types, only FRAMs, MRAMs, PRAMs and RRAMs could overcome limitations of DRAMs or FLASH memories. The principles and technologies of data storage used in these memories are discussed in the next chapter.[7.]

1.1.3 Principles and technologies in most promising memories

1.1.3.1 FRAM

Ferroelectric RAMs use ferroelectric phenomena in ferroelectric materials. When an electric field E stronger than coercive field Ec is applied to a ferroelectric material, the change in the ferroelectric polarization get hysteresis character. The data storage is possible when the polarization versus the electric field loop presents two distinguishable polarization states. [7.]

Two classes of ferroelectric materials are used for FRAMs:

- perovskite structures ($PbZr_xTi_{1-x}O_3$ - PZT)
- layered structures. ($Sr_{1-y}Bi_{2+x}Ta_2O_9$ – SBT or $Bi_{4-x}La_xTi_3O_{12}$ - BLT)

Polarization occurs as a lattice deformation of the cubic form below the Curie point, the temperature above which the material becomes paraelectric. Moving of Ti atom in PZT is possible into two stable positions by an electric field. One of the positions is above the second one below the oxygen plane of the structure (see Figure 1.4). The residual permanent polarization of ferroelectric materials is in the range of 10 to 30 μC/cm . The voltage range required to switch the permanent polarization for deposited layer thicknesses ranging from 70 to 100 nm is between 1.5 to 3 V. From this information is clear the ferroelectric memories are suitable for low voltage applications. [8.]

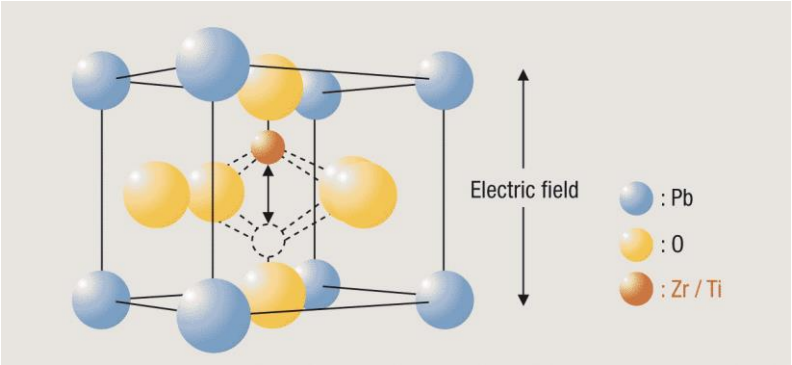


Figure 1.4: The information (logically 1 or 0)is contained in the polarization of the PZT. [9.]

1.1.3.2 MRAM

Magnetic RAMs are possible candidates to replace the current memories, mainly embedded SRAMs and NOR-Flashes. Two types of MRAMs are distinguished based on the used phenomena for data storage:

- Field-writing MRAM – the writing is done by a magnetic field around the current line. Promising results were shown at developing three terminal devices where the magnetic state of magnetic tunnel junction (MTJ) act as a memory bit. [10.]
- Spin-transfer torque MRAMs – the writing is done by spin polarized current which can manipulate magnetization orientations in the magnetic multilayer nanostructures.

The MTJ is schematically shown in Figure 1.5. It is composed from pinned magnetic

layer, tunnel barrier and free magnetic layer. The magnetic layer polarizes the electron spin, which traverses the tunnel barrier. The parallel alignment of the free layer with respect to pinned layer results in a low resistance state, while an antiparallel alignment results in a high resistance state. [8.] Moreover, one of the advantages of the MTJ MRAMs is the non-destructive read with very fast access cycles and the adequate read/write cycles. The major disadvantage of these memories is the high write current, which is in mA range.

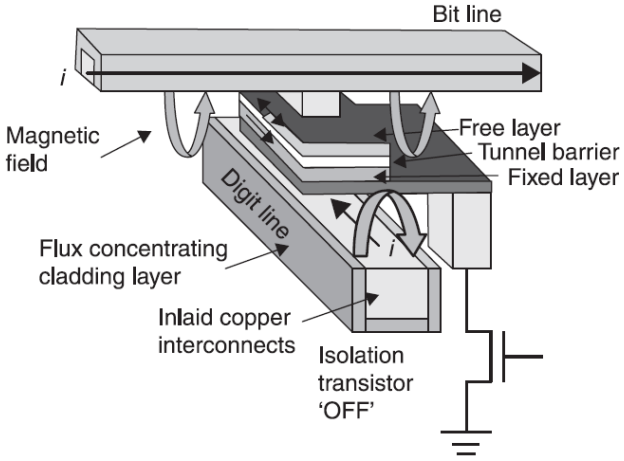


Figure 1.5: Schema of the programming operation mode at the MRAM cell in the 1MTJ/1transistor option [8.]

The Spin-Transfer torque MRAMs are also based on MTJ structures, where a current induced switching caused by spin-transfer torque is exploited.[8.]

1.1.3.3 PRAM

Phase change memory (PCM) exploits the resistance contrast between the amorphous and crystalline states in materials. This simple change is related only to special group of materials, called phase change materials. Indeed, it is not possible to change amorphous phase to crystalline or vice versa in all materials. As a result, it allows distinguishing high electrical resistivity at amorphous state and low resistivity at crystalline state. [12.]

The change between the two states is provided by current induced joule heating. With miniaturization, the energy of 1 pJ should be sufficient for programming for one memory cell. According to the last research results, 40 nm technology is real for mass production.

To realize a PCM cell, usually two types of cell structures are used: either contact minimized cells or volume minimized cells (see Figure 1.6). The contact minimized cell structure is based on a narrow cylindrical metal electrode, which is contacted to a thin phase change material film. This cell structure is also called a mushroom cell. [8.]

The volume minimized cell structure is similar to the mushroom cell, but the fabrication processes more challenged. The most obvious structures in this category are pillar and pore cells. At the pillar cells a narrow cylinder of phase change material is placed between two

electrodes. The fabrication of this kind of structure is difficult, because the pillar is too small and the patterning of the large bottom and top contact must be precise. [14.]

The pore cells are fabricated by filling a sub-lithographic hole in the insulating material at the top of the bottom electrode. The conformal filling of the holes with conventional PVD processes is difficult, but results in filling the hole via ALD and CVD deposition techniques are promising. [14.]

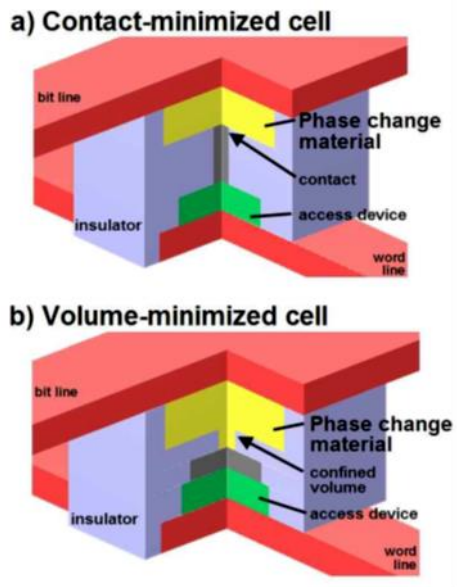


Figure 1.6: Typical device archetypes for PCMs.[8.]

1.1.3.4 RRAM

The basic idea was set up on Chua's paper from 1972, which was a two-terminal resistor with a memory. Resistive switching memory cells are usually presented as a three-layer metal – insulator – metal (MIM) sandwich systems. By applying an appropriate voltage on a MIM cell, the electrical resistivity of the system can be changed substantially. The change from the high resistance state (HRS) to the low resistance state (LRS) or vice versa can represent the logic values 1 and 0. As it was mentioned in the Chapter 1., the main advantage of this change is the state remaining after the electrical power is removed. The switching between two states could be provided with changing the size and the polarity of the electrical potential.

Depending on the voltage polarity, the memristors (or RRAMs) are classified to unipolar, bipolar and nonpolar devices based on the switching behavior. The unipolar switching is provided with a voltage at the same polarity, but with a different magnitude. The bipolar switching is provided by using of both polarities. One polarity is for changing the device from LRS to HRS, the second one is responsible for the switching from HRS to LRS. The nonpolar or threshold devices are capable to switch from LRS to HRS and back from HRS to LRS in positive and also in negative voltage range.

The scientists make efforts to achieve the best performance in all computing and storage applications. The most important performance parameters can be summarized into seven points. [6.][12.]

1. **Operating voltage** – in practical applications the lower power consumption and the lower thermal loss is preferred. Most of the memristor prototypes are using up to 10V operating voltages, but some research labs are decreased switching voltage to 1 – 2V. This voltage range could be lower at thinner layers or at special type of materials.
2. **Operating speed** – is the shortest time, which covers the reading/writing process for one memory cell. The average switching speed is around 5 to 100ns.
3. **Resistance ratio** – the ratio between the HRS to the LRS plays important role at the reading and writing process. To distinguish the two states in circuit design, the resistance ratio must be greater than 10. Some resistive switching devices are working with a very high resistance ratio (6-7 orders of magnitude), which can be used at the fabrication of multibit or multilevel storages. [12.]
4. **Endurance** – the lifetime of the RRAMs is depending on the distinguishable HRS and LRS. The device can be switched frequently, but every switching operation can introduce a small degradation of the device. Usually at the FLASH memories the maximum write cycle is between 10^3 and 10^7 cycles. To achieve a large success on the memory market a good RRAM should provide at least the same or bigger endurance, than the FLASH memories.
5. **Retention time** – the longest time, during the memory cell is capable to retain the information without any change. Nowadays this time is around 10 to 40 years.
6. **Multilevel storage** – ability to store more than one bit in one memory cell. It's enhanced storage density if the resistance ratio between the resistance states is enough large.
7. **Device yield** – uncontrollability of the oxygen concentration in nonstoichiometric oxides generally indicates a fatal flaw of low device yield More papers were published in this field, where the device yield improvement was proposed by suitable electrode material, stoichiometric structures instead nonstoichiometric ones, intentionally used metal nanocrystals in oxide and utilizing doped metal oxide.[6.]

1.1.4 Switching behavior in valve metal oxides

Resistive switching phenomenon has been observed at most of the transition metal oxides. The switching behavior could be observed from physical and from electrical point of view. In unipolar RS, the switching direction depends on the applied voltage amplitude. At the memory cell prepared in HRS, usually a high voltage stress is used to put it into LRS. After this step so called" forming process ", the cell from LRS is switched to HRS by applying a threshold voltage (RESET). For switching from HRS to LRS a voltage higher than the threshold potential is needed. In the SET process the current must be limited. This type of switching has been observed mainly at the highly insulated binary metal oxides. [15.]

At the bipolar RS the dependence of the directional RS on the polarity of applied voltage has been shown. This type of RS behavior has been mainly observed at many semiconducting oxides, such as perovskite oxides.

Threshold switching is a less frequently used and observed than bipolar or unipolar RS. That phenomenon is similar to the unipolar switching. It works with one stable state with no external bias. The device from the HRS to LRS is switched by V_{set}, and the LRS is stable over only a certain range of applied biases. The device reverts to the HRS in moment, when the applied bias falls below this range. The threshold switching due to the instability of CFs in LRS is not suitable for NVM.

The RS behavior based on the conductive path is commonly categorized into two classes. The first class is the filamentary conductive path, where the ON and the OFF state are depending on the formation and the rupture of the conductive filament in an insulating matrix. (Figure 1.7.c.) [15.]

The second class is the interface type path, where the RS takes place at the interface between the metal electrode and the oxide. Electrochemical migration of oxygen vacancies, charge carrier (hole or electron) trapping or Mott transition induced by carriers doped at the interface are the mostly used models for driving mechanism in RS involving an interface type conducting path. (Figure 1.7.d.) [15.]

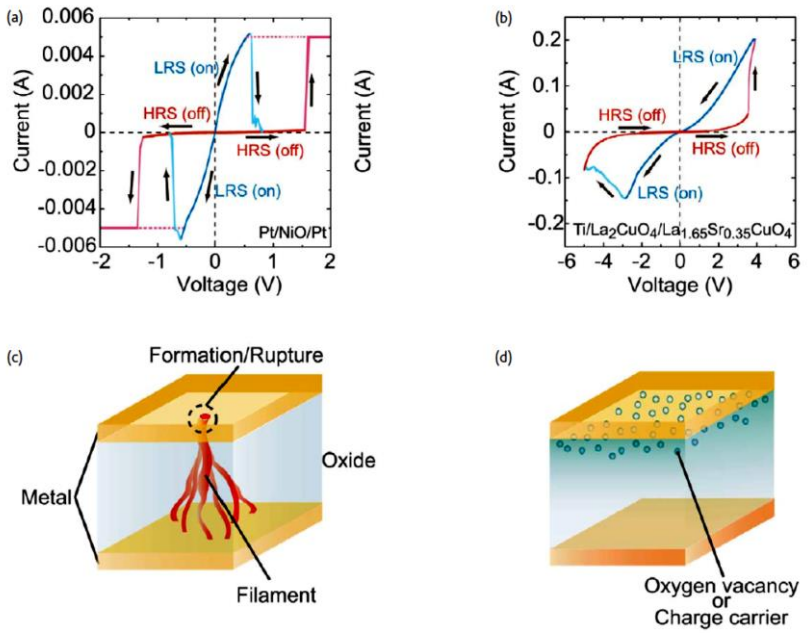


Figure 1.7: Schematic view of the unipolar (a) and bipolar (b) switching behavior. Schema of the filament type (c) and interface-type conductive paths (d). [15.]

1.1.4.1 Unipolar switching in oxides

Forming and Set processes

As-grown oxide cells are good dielectrics without capability of RS. To crate RS device from an as-grown oxide is obligatory to change the oxide properties. By applying a large external bias, oxygen vacancies or CFs are generated. This process called electroforming in unipolar switching is known to be triggered by the soft dielectric breakdown. Soft dielectric breakdown is a controlled breakdown limited by the compliance current, and it provides thermal energy to the ions in an oxide cell. When a large electric field is applied to a pristine oxide cell, the negatively charged oxygen ions move to the anodic interface.

The formation of one oxygen vacancy can be described in Kröger–Vink nomenclature as follow:

$$O_O \leftrightarrow \frac{1}{2}O_2 + V_O^{"} + 2e^- \qquad (18)$$

Based on a paper from Kröger and Vink the O_O denotes an oxygen ion in a regular lattice and $V_O^{"}$ indicates an oxygen vacancy. [23.][24.]

The dominant force for oxygen vacancy migration – electric field effect or Soret force – has primary effect on the growth behaviors of the CFs during the forming process.

In case, when the dominant force is the electric field effect, the oxygen vacancies are migrating toward the cathode. In this process the CFs composed of oxygen vacancies accumulating near the cathode and subsequently growing through the cell. This type of CF generation has been observed with a conical structure in TiO_2 [23.][25.] [Figure 1.8. a.] The second case, when the Soret force is dominated, the oxygen vacancies are moving mostly perpendicularly to the electric field. The CFs usually are expected with cylindrical shape and

highly oxygen concentrated pathways. [Figure 1.8 b.] [25.]

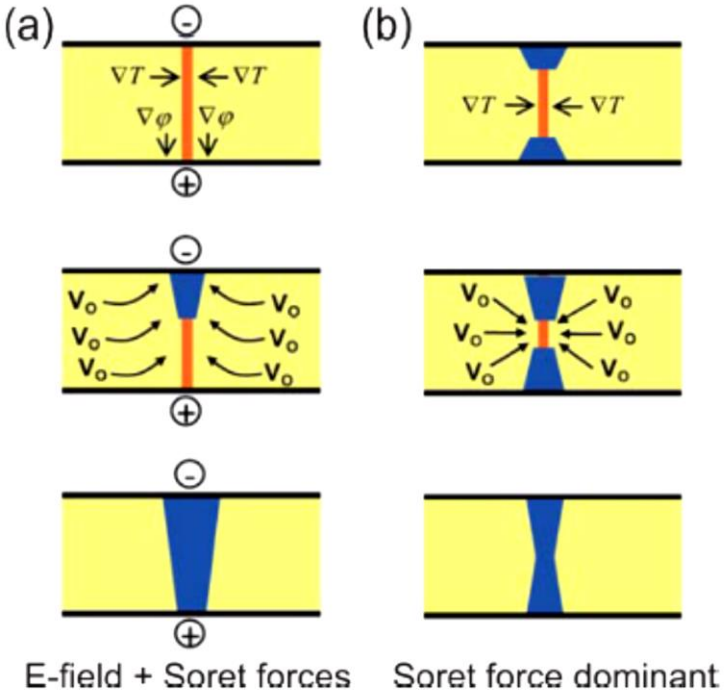


Figure 1.8.: Two filament growing models initiated by Joule heating. The CF is built by positively charged vacancies, attracted toward the cathode (a.). CF built is induced by Soret and Fick forces if the vacancies are electronically neutral (b.). [25.][23.]

The localized CFs in an oxide samples generated by forming process brings local change in conductance, which is is related to changes in the chemical stoichiometry of the oxide. The mechanism of the local conductance changed by the oxygen stoichiometry is depending on the material, mainly on the phase diagram of the composing oxide. During the RS formation in metal oxides the formation of Magnéli phases of formation of metal-rich (or metlallic) region is used for CF generating. As Kwon et.al. published they found besides the nanofilaments in the connected shape several disconnected nanofilaments in Magneli phases as well. The diameter of the CFs at the cathode side was bigger which is a proof the CFs are growing mostly from the cathode side. [44.]

When the current limit reaches the compliance limit, the bias voltage is significantly reduced to prevent a further growth of other CFs. Figure 1.9**. a.** show a complete CF with conical shape grown from the top electrode down to the bottom electrode. The not completed or disconnected nanofilament kept the conical shape with a wider diameter at the TE. (Figure 1.9**. b.**)

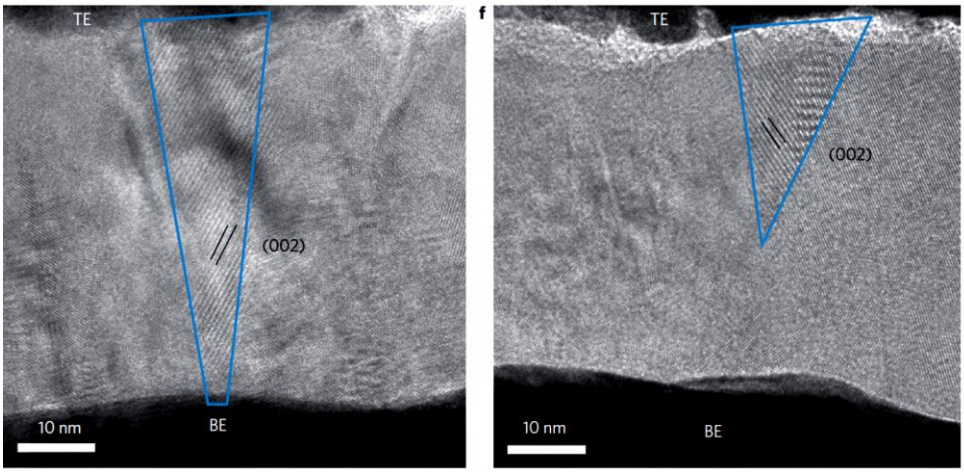


Figure 1.9.: Magne´li structures in the SET sample. High-resolution TEM image of a connected Ti_4O_7 / Ti_5O_9 nanofilament (left) and a disconnected filament (right). [44.]

Reset process

The flown current during the forming or set process can produce in the formed CF Joule heating. Thereby the temperature in nanometer scale temporary can reach few hundred Kelvins. As Chang et.al. observed in a Pt/NiO/Pt unipolar switching cell, the maximum temperature in the vicinity of the CF could reach higher than 900 °K with a bias of 2 V applied to the electrodes. If we took into consideration the fact, the TiO_2 can be transform from amorphous phase into crystal phase from 400 °C by thermal annealing, or even at lower temperature in case of hydrothermal treatments, and then it is clear the switching mechanism can be more complex in few cases. [44.][45.]

The current generated Joule heating can provide the oxygen vacancies with sufficient thermal energy to overcome the energetic barrier for hopping. In this case the Soret force and the Fick force are acting perpendicularly to the electric field. The Soret force can be characterized as an effect where the temperature gradient attracts the oxygen vacancies toward the CF. The Fick force is an effect where the density gradient repels the oxygen vacancies from the CF.

Both forces are playing important role in resistive switching. The Fick force is dominating during the reset process, where the CF is ruptured. [46.][46.]

1.1.4.2 Bipolar switching in oxides

Bipolar switching in oxides means polarity dependence of the Set and Reset operations. The basic mechanism for bipolar switching can be defined on the movement of oxygen vacancies or by the electron trapping/de-trapping.

Oxygen vacancies should always exist in any oxide due to entropic disorder. The creation of the oxygen vacancies can be created by partial substitution with dopants, as Y-doped ZrO_2 or Ca-doped $BiFeO_3$, or via the forming process, as a result of electrolytic reaction – explained by Kröger – Vink nomenclature.

The oxygen vacancy motion is forced by an external electric field, the direction of the detailed motion of the vacancies is vary, however for the vacancies formed in a solid with periodic potential, the motion can be described by a thermally assisted hopping process. [75.][76.] The disordered interfaces or the grain boundaries can also have effect on the oxygen vacancy migration.

The electron trap/detrap in oxides usually is presented by three models:

1. Pool-Frenkel emission, where the emission model is related to the thermal fluctuations of trapped electrons. The trapped electron gets energy from the random thermal fluctuation for the transfer from the localized state into the conduction band, where it can transport through the crystal. The I(V) behaves as $I \sim V\exp^{(V1/2)}$
2. The space charge limited current model describes situation, where the external charge carriers from the electrode are more dominant than the free carriers in the film. At low voltage the films conduction is dominating (the I(V) curve is linear), at increasing voltage the amount of the externa charge carriers increasing, therefor the electrons are gradually trapped into the defects (non-linear I(V)). If the applied potential is high, the electrons are trapped in defects, however the excess electrons can flow and therefor the linear relationship of $I \sim V$ is recovered.
3. Trap-assisted tunneling model describes tunneling of the electrons between the traps *via* hopping. The conduction is dominated by cathode-trap or anode-trap hoping, resulting I(V) curves as $\ln(I/V^2) \sim 1/V$.

Forming process is required due to first conductive filament formation. The forming is not necessary for all oxides, especially if the bulk region is eliminated by a low thickness (about 4 nm), however for some oxides, like (TaO_x, TiO_2), the CFs can be created only by forming process. The CFs can be detectable by TEM, EELS or by hard X-ray spectromicroscopy, if channels are formed by exhibited metallic properties and ordered planes of oxygen vacancies, or by comparison of oxygen-deficient regions with as-grown material.

Briefly the forming process is the first step, when the virgin sample (also called pristine sample) under applied external bias a CFs are grown, mostly in the bulk region. Between the CF and the top electrode, a gap region is formed as well, however the gap has lower resistance (R_{LRS}) then the CF (LRS state). The HRS state appears after Reset process, when the Gap region with resistance R_{LRS} is transformed back to the initial resistance state of the oxide (HRS).

The importance of the CF in bipolar switching is significant mainly due to the current localization. The CF localizes current into conducting spots and therefor the switching will take place always at the same position in the same gap region.

The resistance of the device will be independent on the electrode area, the determining is the CF nanoscale gap area at the top of the CF. In studies, where the electrode surface had effect on the RS resistances, the switching behavior can be called as interface type switching or laterally uniform switching among the interfaces.

Bipolar switching can be achieved by growth/shrinkage of a virtual cathode by oxygen vacancy movements, by modulation of the Schottky barrier by oxygen vacancy movements and by trap/detrap of electrons. The modulation of the Schottky barrier by oxygen vacancy

movements is typical for n-type semiconductors with a metal electrode with a large work function, as Au or Pt.

This work is focusing on the TiO_2 based MOM devices with Ti and Au electrodes, therefor the modulation of the Schottky barrier height by oxygen vacancy movements will be briefly described.

The interface between the Ti (low work funciton) and the oxide is usually ohmic. The Schottky barrier appears at the oxide and Au interface, where the oxygen vacancies in the oxide are behaves as donors. Therefor any change in the oxygen vacancy concentration can significantly change the barrier width and along with it the electrical resistivity of the device, respectively. The width of the Schottky barrier between the oxide and the Au electrode, has width inversely proportional to the square root of the dopant concentration.

The negative polarization of the anode forcing the positively charged electrons towards the electrode, therefore the Schottky barrier width is decreased, the resistance state from HRS is changing to LRS. At positive anode polarization the barrier width is increasing and with the barrier width the resistance is growing as well. Simulation of a semiconductor with mobile dopant model for bipolar switching was published by Lee at al., [73.] Another models were described by Jeon et al., about the effect of Helmholtz layer in $Pt/TiO_2/Pt$ devices, where the barrier height was modulated by electrochemical reactions involving oxygen vacancies at the metal oxide interface. [74.]

1.2 Valve metal oxides

Valve metals are part of group *IV*B and *V*B, as Ti, Zr, Hf, V, Nb, Ta, from *III*A Al, and they are immediately reacting with the oxygen or humidity to form a protective oxide layer. For their fast self-protection oxide layer, they are widely used in the construction of chemical apparatus.

The other usage for the valve metals or valve metal oxides, respectively, is in electronics, where their excellent metal oxide properties are used in piezoelectric, multifrerrocity, sensing or resistive switching researches.

Dielectric properties of valve metal oxides are well known due to the high dielectric constants, therefore the high-κ oxide can be also a proper naming. Other oxide properties, like the vacancy defects formed by oxygen disorder in the lattice is used in electronics, as band insulators or Mott insulators.

Memristive research is using valve metal oxides from the beginning – the first memristor published by Strukov et al., was fabricated with a TiO_2 layer – and with the different preparation methods, the physical properties or even the shape of the prepared oxide can be controlled.

The spine of this work is TiO_2 structures, prepared by electrochemical anodization. The TiO_2 is described in chapter 1.2.2. and the fabrication process is explained in chapter 3.5., respectively.

1.2.1 Anodic aluminum oxide

The aluminum layers in ambient atmospheres becomes quickly coated with a native oxide layer in thickness 2-3 nm. This thin oxide layer inhibits the aluminum surface from corrosion in common environments. Corrosive chemicals or environments containing chlorides, sulfates etc. can cause local corrosion of metal.

Buff in 1857 discovered the aluminum can be electrochemically oxidized in aqueous solution to form thicker oxide layer than the native one. The aluminum part in the electrolytic cell was used as anode and the process has been named „anodization". Anodic oxidation of aluminum surfaces was commercially used as a protection layer since the beginning of the 20th century.

Generally, the aluminum oxide has two type of morphologies: the nonporous barrier oxide and the porous oxide. The morphology is mainly determined by the chemical nature of the electrolyte. A compact barrier type film (BTF) can be formed in electrolytes with pH 5-7. The most common solutions for preparation are oxalate, citrate, phosphate, adipate. The porous anodic alumina (PAA) is formed in acidic electrolytes. Oxalic, malonic, selenic, tartaric, citric, phosphoric, malic and chromic acids are widely used for anodization. The pores are formed due to the lower pH, because the AAO is slightly soluble at lower pH.

The oxide growth kinetics are different at BTF and PAA. The thickness of the BTF oxide formation is limited with the applied potential. During the oxide growth process at constant voltage (U) the current density (J) is decreasing exponentially with time (t). The film growth rate is decreases almost exponentially with the time, which means the film thickness is limited. Experimentally has been defined the thickness of the BTF is proportional to the applied potential.[47.]

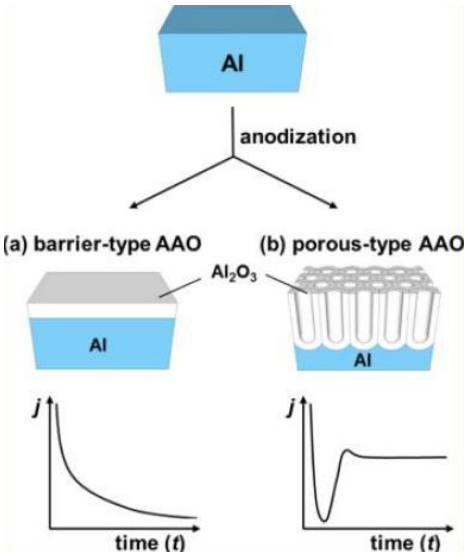


Figure 1.10.: Aluminum oxide fomed by barrier type anodic oxidation and porous type anodic oxidation. [47.]

The PAA growth process is mainly depending on the current density (J). At potentiostatic (U is constant) conditions the current density is almost constant during the anodization. The stable current density is due to the constant thickness of the barrier layer at the pore bottom. The PAA thickness is linearly proportional to the total amount of the charge during the anodization. The diameter of the pores is depending on the applied potential and on the used electrolyte.[47.]

1.2.1.1 Fundamental interfacial reactions

Empirical exponential dependence of the ionic current density (j) on the electric field (E) was established for aluminum anodizing. During the anodic oxide growth a high-field conditions are present. The current density (j) under high-field conditions can be related with the movement of the charged ions in the barrier oxide as well as the potential drop (ΔU) across the barrier oxide through the exponential law of Güntherschulze and Betz:

$$j = j_0 \exp\left(\frac{\beta \Delta U}{t_b}\right) \quad (19)$$

where j_0 and β are material-dependent constants at a given temperature, and $\Delta U/t_b$ is the effective electric field (E, usually 10^6–10^7 Vcm^{-1}) impressed on the barrier layer with thickness t_b. For AAO a wide range of j_0 and β values were published ($j_0 = 3x10^4$ to 10-^{18} Acm^{-2} and $\beta = 10^{-7}$ to $5{,}1x10^{-6}$ cmV^{-1}).

The anodic oxidation of metals in electrolytes are explained based on rate-determing steps for oxide formation in three different theories.

The Mott−Cabrera theory is explaining the ion transfer across the metal/oxide interface, the Verwey theory is using explanation for ion transfer through the oxide bulk, and the Dewald theory presents the ion transfer across the oxide/electrolyte interface.[47.]

In the point defect model of Chao et al.,[77.] the oxide film is assumed to contain a high concentration of non-interacting positive and negative point defects, and the rate-determining step for the oxide growth is assumed to be the transport of metal and oxide vacancies across the oxide film.

Above mentioned theories can explain the empirical relationship proposed by Güntershultz and Betz. On the other hand, transient experiments favorably indicate that the rate-determining step is the movement of charged ions within the oxide. [47.]

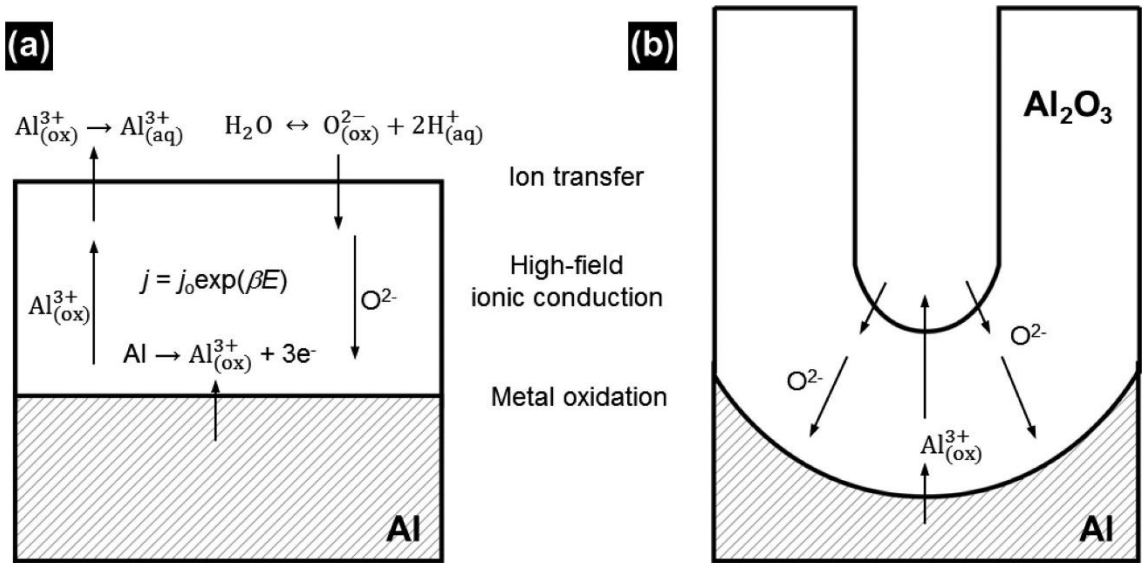


Figure 1.11.: Elementary interfacial reactions for barrier type (a.) and for porous type (b.) anodization. [47.]

The thickness of the consumed aluminum during anodization with 0,3M oxalic acid electrolyte is counted with equation

$$0{,}33 I_a t = h_a \qquad (20)$$

where I_a is the current density, t is time of the anodization and the h_a is the thickness of the consumed aluminum layer in nm.

1.2.2 Titanium dioxide

Titanium dioxide (TiO_2) is a widely used material since the early 20th century. The properties of this binary oxide allow to use as a pigment in sunscreens, paints, toothpaste, etc. The discovery of the phenomenon of the photocatalytic splitting of water on TiO_2 electrode under UV light in 1972 launched a wave of research based on TiO_2. Promising applications in areas ranging from photovoltaics, photo catalysis, gas sensors and non-volatile memories were developed and invented. The TiO_2 is a widely used and easy modifiable material. The photoactivity, the sensing properties or the electrical behavior are depended on the crystallographic orientation, the doping, the surface structure, etc.

The TiO_2 as a material could be prepared in several ways. In dependence of the preparation process the TiO_2 producing is possible with several methods: [50.]

a. sol-gel method
b. micelle and inverse micelle method
c. sol method
d. hydrothermal method
e. solvothermal method
f. chemical vapor deposition
g. physical vapor deposition
h. electrochemical method
i. sonochemical method
j. microwave method
k. mesoporous/nanoporous materials
l. aerogels
m. opal and photonic materials
n. nanosheets.

Due to the length of the list, only some of the above-mentioned technologies will be characterized.[50.]

Sol-ge l method

The sol-gel method is a versatile process used in making various ceramic materials. In case of the TiO_2 from hydrolysis of titanium precursor with sol-gel method the nanomaterial have been synthetized. The sol-gel prepared by mixing tetrabutyl-titanate or titanium isopropoxide in acetic acid is proper for preparation of nanorods with low diameter. TiO_2 nanorods with diameter 5nm was synthetised with sol-gel method by Joo et al.[51.]

Sol-gel methods are often combined with PAA membranes for fabrication of TiO_2 nanotubes (NT) and nanorods. Deposition of TiO_2 into PAA template with well aligned parallel pores with well controlled dimensions is a cheap, low temperature easy controlled wet chemical process. The PAA template after the deposition of TiO_2 is removed by wet etching. The dimensions of the deposited oxide array are depends on the PAA template pore alignments and dimensions.[50.][51.]

Physical vapor deposition (PVD)

PVD methods are variously used for metal layer depositions. The layer adhesion, the deposition speed or the various possibilities of set ups to control the material properties of the deposited layers are the biggest advantages of the PVD methods.

TiO_2 layers deposited by reactive radiofrequency magnetron sputtering system from highly pure Ti target at low argon/oxygen gas flow and crystallized to rutile phase are primary recommended for optoelectronic devices. The disadvantage of the RF magnetron sputtering is mainly the physical limitation of the deposition into deep narrow pores. [52.]

Electrochemical method

Electrochemical methods for preparation of TiO_2 layers or structures could be distributed in two main groups. Electrodeposition of TiO_2, where the Ti or the TiO_2 layer is deposited on the substrate, and anodic oxidation, where the previously deposited Ti layer is oxidized in electrolyte.

Electrodeposition

Electrodeposition is commonly used method to perform usually metallic coating on a surface by electrochemical reduction on the cathode side. The metallic ions are attracted to the cathodes surface and reduced to a metallic form. Based on the masking method the 2D geometrical shape is controlled by lithography techniques (masking by photoresist layers or using sacrificial layers removed by selective etchants).

The 3D shape of the reduced metals is prepared in assistance of supporting matrixes, as highly ordered porous anodic alumina oxides or other submicron structures.[53.]

Electrochemical anodization

Electrochemical anodization of valve metal oxides is a universal method with several possibilities. With anodic oxidation of the Ti layer, depending on the used electrolyte, from compact oxide layer – oxalic acid-based electrolytes – to different nanotube fields – ammonium fluoride-based electrolytes – can be prepared.

The anodized TiO_2 layers are mostly amorphous, the crystallographic orientation from anatase to brookite are achieved with annealing at higher temperatures. The crystallization process can be achieved for the same crystallographic orientation at different temperatures due to the anodizing conditions. The process of the Ti anodization for TiO_2 nanocolumns is explained in chapter 3.5 Anodization of Titanium.

Crystallography of the pure TiO_2

TiO_2 exists naturally mainly in three crystalline phases: anatase (tetragonal), rutile

(tetragonal), and brookite (orthorhombic) (Figure 1.12). Anatase and rutile have a tetragonal structure with a=0.536 nm and c=0.953 nm (anatase), a=0.459 nm and c=0.296 nm (rutile) and Brookite has an orthorhombic structure with a=0.915 nm, b=0.544 nm, and c=0.514 nm.[54.]

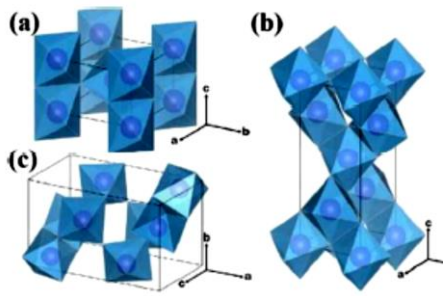


Figure 1.12.: Crystal structures of TiO_2 polymorphs: Rutile (a), Anatase (b), Brookite (c). The purple spheres represent Ti atom.[54.]

Among the different polymorphs, rutile is generally considered to be the most stable bulk phase, while at the nanoscale, anatase and brookite are more stable due to lower surface energy. The crystal phases are affected by the experimental conditions (synthesis method, annealing temperature, pH, duration etc.).[54.]

The XRD pattern of the TiO_2 nanotube arrays before annealing did not contained obvious peak. The amorphous phase of the TiO_2 NTA started to converse to anatase phase at approximately 250°C. From 250 to 650°C the relative intensity of the anatase peak is increasing. The anatase phase change observed at 650°C shown conversion of part of the anatase into rutile phase. With the increasing annealing temperature from 650°C up to 850°C the anatase phase is decreasing and the rutile phase is increasing.[55.]

Pure TiO_2 synthetized by hydrothermal method conversed into TiO_2 (B) has the same formula as TiO_2, it has more open framework structure, a relatively low density and large specific capacity than other polymorphs. This phenomenon began to grow applications in the fields of energy conversions as photocatalysis solar cells and lithium batteries.[55.]

2 AIM OF THE WORK

Considering the variability of the valve metal oxides preparation and the possibilities of its usage in electronics, the aim of this thesis is to seek a fabrication technique using self-ordered anodic alumina arrays with TiO_2 nanocolumns and investigate its electronic properties.

The particular aims of this thesis are:

- Preparation of the self-ordered AAO supporting matrix with self-grown TiO_2 nanocolumns and realization of the electric contacts for further measurements.
- Investigation of the functional material and the structure analysis of the nanocolumns grown at different conditions.
- Electrical characterization of prepared samples, evaluation of achieved resistive switching phenomenon.

3 EXPERIMENTAL

The fabrication complexity and expensive techniques used for memristor realization in HP lab (written in cap. 2.2) are not very popular in the most of research and industry laboratories. Even their idea is genius it could be further improved. Anodic oxidation of aluminum is a well-known process. This process can produce the porous films possessing high pore density, uniform pore size. The other important advantage is the versatility and low cost. [23.]

In 1999 Mozalev et al. published an article about the microresistors fabricated by anodic processes. [24.] They produced nanoscale metal-oxide coatings, using Ta-Al layers and anodic oxidation. Main advantage was the self-growing of tTa_2O_5 nanostructures with high electrical resistance. Later in 2005, Mozalev et al. also characterized the growth and electrical transport properties of self-organized Ta–Al bilayers formed by anodization. [8.] During the material characterization of the cross-section sample of tantalum oxide nanohillocks in anodic aluminum oxide (AAO or porous anodic alumina PAA) layer, a non-homogenity of the oxygen concentration was detected. Using the information, it might be possible to prepare self-ordered memristive structures via anodization. [25.]

The schematic of the experimental plan (Table 2.) was set up with a purpose to compare different nanocolumn properties and find a way to prepare samples with resistive switching behavior. Samples, where resistive switching is achieved, will be analyzed in detail in electrical and in material point of view as well. If the sample was successfully prepared and it shown resistive switching behavior, the field can be green, if it was successfully prepared, but it is without resistive switching the field will be yellow. In case of failure at the fabrication, the field is red.

Table 2.: Experimental plan

Anodization potential	**Sweep rate for re-anodization**	**Sweep rate for re-anodization**	**Annealing set up**		
	0,2 $V \cdot s^{-1}$	**2 $V \cdot s^{-1}$**	**As-Anodized**	**500°C/2h in Vacuum**	**500°C/2h in Air**
40V					
40V rA 100V					
40V rA 130V					

3.1 Layer preparation

The Ti layers, deposited by PVD evaporation or magnetron sputtering method, are not ideal for template-based anodization. Obviously in the evaporated/magnetron sputtered layers is observable a material stress or the layers crystallographic orientation is not uniform.

The Ion beam assisted deposition is a highly precise sputtering technique which fulfills every requirement of Ti layers for anodic oxidation.

Thermal-oxide-coated Si wafers of diameters 100 mm were used as starting substrates. Titanium layers with thickness 300 nm were deposited by sputtering of 99.95% Ti target, using an ion beam sputtering. The deposition chamber was initially evacuated to $5 \cdot 10^{-7}$ mbar, with subsequent sputtering using 99.998% argon at $5 \cdot 10^{-3}$ mbar. The Ti/Al bilayers (aluminum-on-titanium) were prepared by sequential sputter-deposition of Ti and Al layers, respectively 100 nm (Ti) and 100 to 1000nm (Al) thick.

The wafer was cut on pieces with dimension 1x1 cm and categorized in four groups, based on Al thickness. The rest of the wafer was considered as scrap pieces, with a thinnest Al layer. (Figure 3.1.)

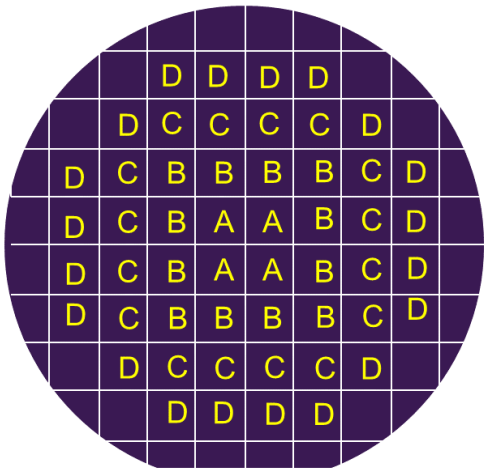


Figure 3.1.: Wafer drawing with marked section groups. The wafer was cutted into 1x1 cm pieces with diamond scratcher.

Based on previous experiences about anodization of sputtered Al layers a non-uniform layer thickness was observed. The thickness differences may cause undesirable inaccuracy mainly during two step anodization, where the precise thickness control during the Al anodizing is obligatory. The different anodization times are presented in Figure 3.2.

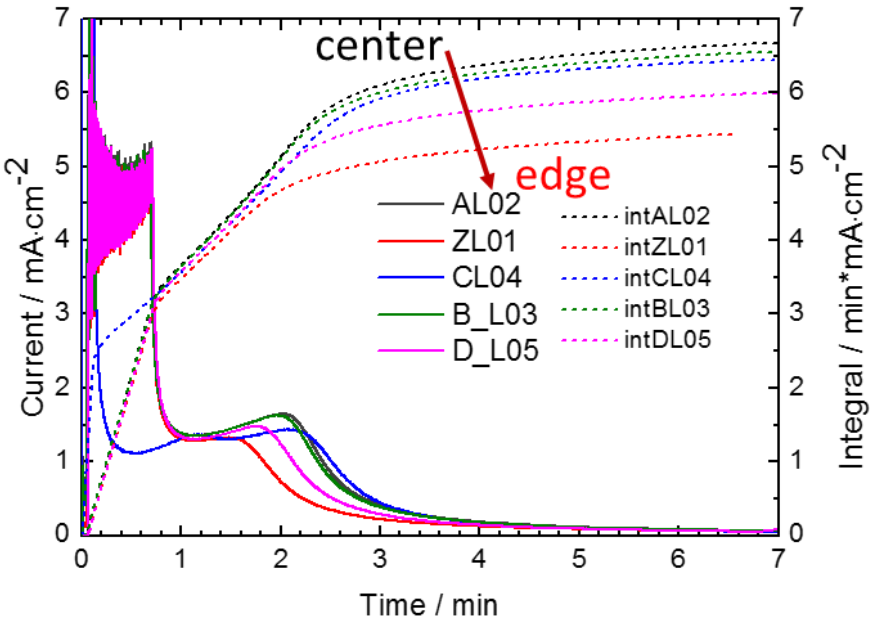


Figure 3.2.: Current time curves of anodized Al layer sputtered by IBAD. Anodization was performed at different wafer positions. The integral of the curves showing clearly, the thickness of the Al layer from the center to the edge is decreasing.

3.2 Anodization of Aluminum

Valve metals as Al, Ti, Ta, W, are specific metals which are suitable for anodic oxidation.

The first part of the experimental work is optimization of the anodic oxidation of Ti/Al structures. The initial surface was sputter-deposited metal bilayer of Ti/Al on the silicon wafer (previously covered with 500 nm of SiO2). Titanium layer with thickness of 300 nm was covered with 550 nm thick Al layer. The anodization was performed at 5 °C with a 0.3 M oxalic acid solution at the circulation speed of 70 mL/min. The apparatus was equipped with poly-tetrafluor-ethylene (PTFE) cylindrical head with internal diameter 6.9 mm equipped with a stainless steel electrode. (Figure 3.3.)

During the anodizing process, the current was always limited to 5 mA and the potential for the aluminum layer was constantly kept at 40 V. The diameter of the pores in AAO is approximately 36-40 nm. The surface of the AAO for more detailed evaluation was chemically decorated with selective AAO etchant. (Figure 3.4.)

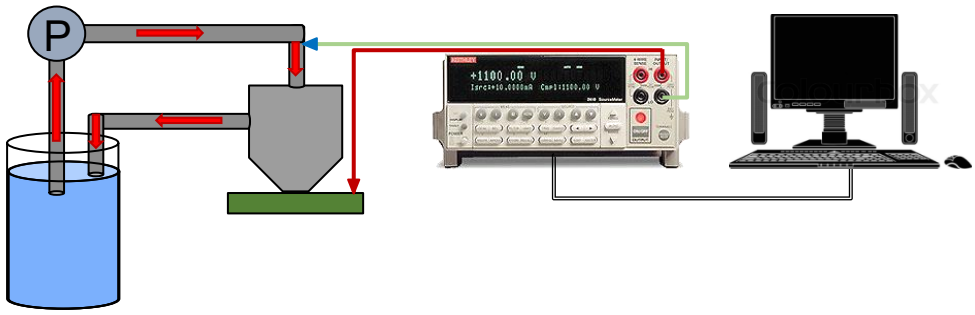


Figure 3.3.: Schematic view of the anodization station.

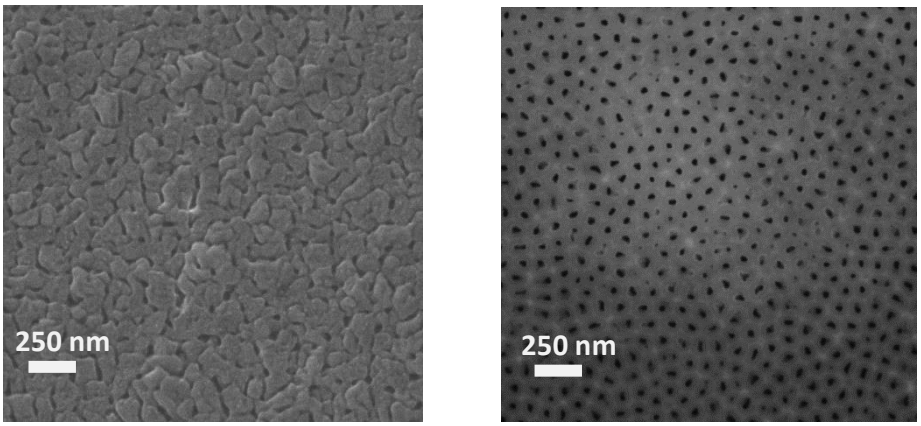


Figure 3.4.: Surface of the AAO template anodized at 40V before chemical decoration (left) and after decoration for 20 seconds (right).

3.3 One step anodization

The first part of the experimental work is optimization of the anodic oxidation of Ti-Al structures. The initial surface was sputter-deposited metal bilayer of Ti/Al on the silicon wafer (previously covered with 500 nm of SiO2). Titanium layer with thickness of 300 nm was covered with 550 nm thick Al layer. The anodization was performed at 5 °C with a 0.3 M oxalic acid solution at the circulation speed of 70 mL/min. The apparatus was equipped with poly-tetrafluor-ethylene (PTFE) head with internal diameter 6.9 mm equipped with a stainless steel electrode.

During the anodizing process, the current was always limited to 5 $mA \cdot cm^{-2}$ and the potential for the aluminum layer was constantly kept at 40 V. The diameter of the pores in AAO is approximately 40–50 nm.

Anodization of the titanium layers were provided at potential of 40 V and 60 V (see Figure 3.5.). Both potentials are suitable to prepare self-grown TiO_2 nanowires in AAO, the difference is in height of TiO_2 nanowires in the pores. At the potential of 60 V the TiO_2 columns are higher than at 40 V. The thickness of the AAO has no influence on the length of the nanocolumns. (Figure 3.6.)

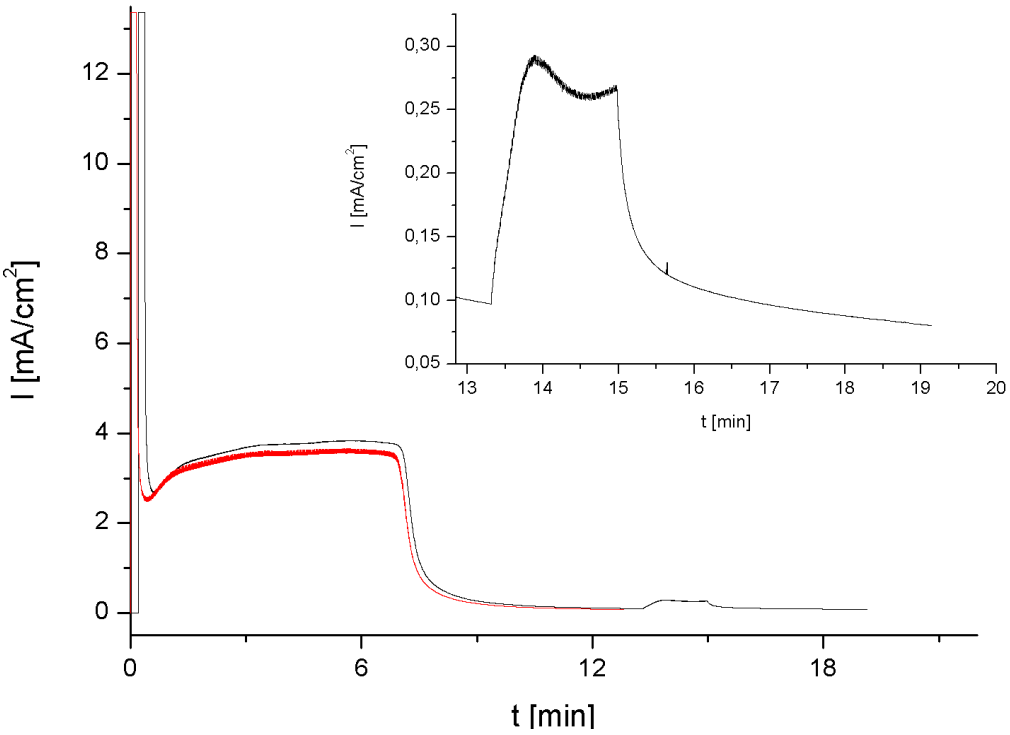


Figure 3.5.: Anodization curve for Al/Ti bilayer. During the anodization of Al, the voltage was kept at 40 V for both sample (red and black curves). The first sample was anodized for 13 min including Ti anodizing at 40 V (red curve). The second sample was anodized for 19.25 min. In case of the second sample after 13.5 minutes the voltage was increased from 40 to 60 V (black curve)

After the first successful and repeatable test the anodization parameters and the type of the samples for comparison purposes were fixed.

The temperature of the electrolyte for the anodization was fixed for 5°C, the flow rate of the electrolyte in the cylindrical PTFE cell was fixed for 70 ml. The anodization voltage for the aluminum layer and for the titanium oxide bulks was constant as well (40 V).

Three column length respectively anodization potential was fixed too. For the shortest column length 40V was used and for higher nanocolumns 100V were applied.

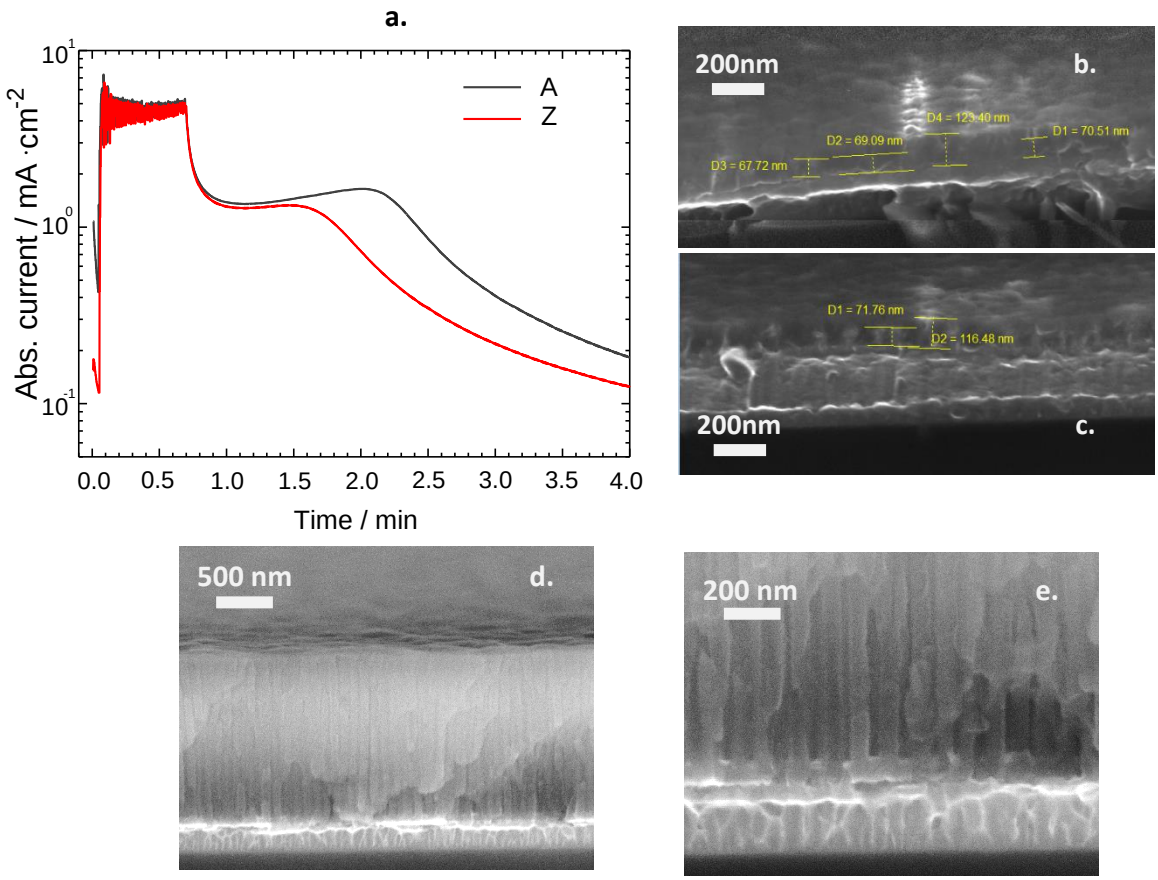


Figure 3.6.: Anodization of an 80 nm thin Al layer at potential 40 V and re-anodized at 60V. The current time curve shows the difference between the anodization time of the Al layer at the center of the wafer and on the edge (the re-anodization part of the curve was removed for better visualisation). The differencies in the final AAO layer thicknesses are approximatley -6 % at the edge in comparison with an anodized center. The re-anodized nanocolumns are about 70 nm.

The figures d and e are presenting an AAO prepared from 1000nm thick Al layer. The final AAO layer is extremly thick in comparison with tha layers in figures b and c, however the height of the nanocolumns are about 70nm, which means the thickness of the AAO has no influence on the growing process of the TiO_2 nanocolumn arrays.

3.4 Two step anodization

In previous chapter the one step anodizing and re-anodizing process was explained. The two-step anodization from the electrochemical point of view is like the one step anodization. The main difference lies in the way of the AAO control. Due to the physical limitation of the AAO growing mechanism, the layer thickness control is possible only with removement of the undesirable layer thickness.

Differences between the final AAO thickness and the initial AAO thickness is depending on the length of the nanocolumns. The height of the nanocolumns is controlled by the re-anodization potential and the initial thickness of the AAO was counted by equation *20* written in chapter 1.2.1.1. The calculation was verified with several thickness measurements from cross sections after the anodization. The samples were marked from the back side with dentification sign showing from which part of the silicon wafer was the sample taken. The distribution of the samples was explained in previous chapter 3.1. *Layer preparation*. The samples from the same bar have identic thicknesses and the undesirable layer thickness is definable precisely and easily.

The thickness of the consumed AL layer and the time of the anodization to reach the proper thickness of the undesirable layer specified as $6{,}5 Å \cdot s^{-1}$. The anodization of the aluminum was performed with identic setup for all experiments and therefore the speed of the Al layer consumption was in every case the same.

The process of anodization and the process of chemical etching of the AAO before the second anodization step is provided in the same anodization cell without dismounting. Rinsing of the AAO surface after the anodization was done by constant circulating of demineralized water (200 ml of H_2O at room temperature for every rinsing respectively). The selective etching process with tempered etchant to 58°C at constant circulation for 20 min at speed 75ml/minute was implemented. The selective AAO etchant for the AAO decoration and for the removal was the same. The etching was finished with rinsing to remove the etchant residues from the surface.

Second step of the anodizing process was performed in an identic way as the one step anodization. The results of the two-step anodization are presented in figures Figure 3.7., Figure 3.8. The advantages and disadvantages of between the one step and two step anodization are presented in Table 3.

Table 3. Comparison of the one- and the two-step anodization – advantages, disadvantages.

One-step anodization	Two-step anodization
Advantages Continuity of the anodizing Probability of the structure/layer contamination is low Probability of the trapped air bubbles in the apparatus above the sample surface is low	**Advantages** Thickness of the AAO layer is controlled Blind pores are occurring rarely Deposition of top electrode with PVD techniques primary on the top of the nanocolumns.
Disadvantages The thickness of the final AAO layer depends on the thickness of the initial Al layer	**Disadvantages** Probability of the trapped air bubbles in the apparatus above the sample surface is higher, than at one step anodization Probability of the structure/layer contamination is higher The total time for the sample preparation is few times higher, than at one step anodization

If the thickness of the AAO layer or the minimal height difference between the nanocolumns and nanopores is required, the two-step anodization can be an option. The final AAO must have thickness min. 2x height of the barrier layer (for example in case of 35nm thick barrier layer the final thinnest AAO must have 70 nm or higher). Therefore, the two-step anodization is appropriate only for re-anodized nanocolumns.

The nanocolumns after two step anodization and Ti re-anodization respectively should be visible during SEM observation. For better visibility the surface was decorated for 20 sec in selective etchant for AAO. (Figure 3.8.)

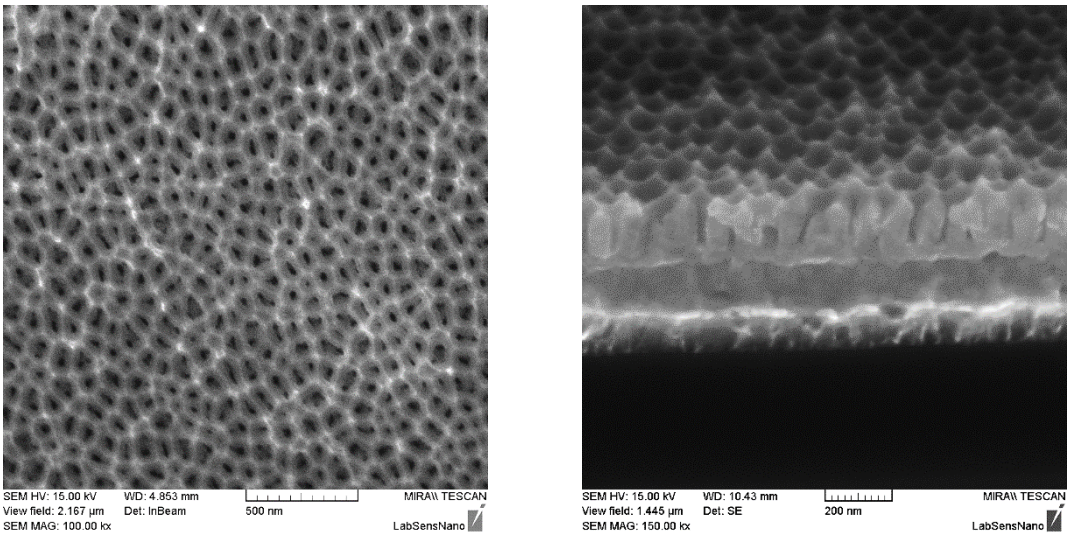


Figure 3.7.: AAO surface (left) after the second anodizing before re-anodization of Ti. Tilted cross section (right) about the AAO template before re-anodization of Ti. After a re-anodization the pores should be filled with TiO_2. The not completely flat AAO surface has no negative effect on a later magnetron sputtering or on the electrical contacts.

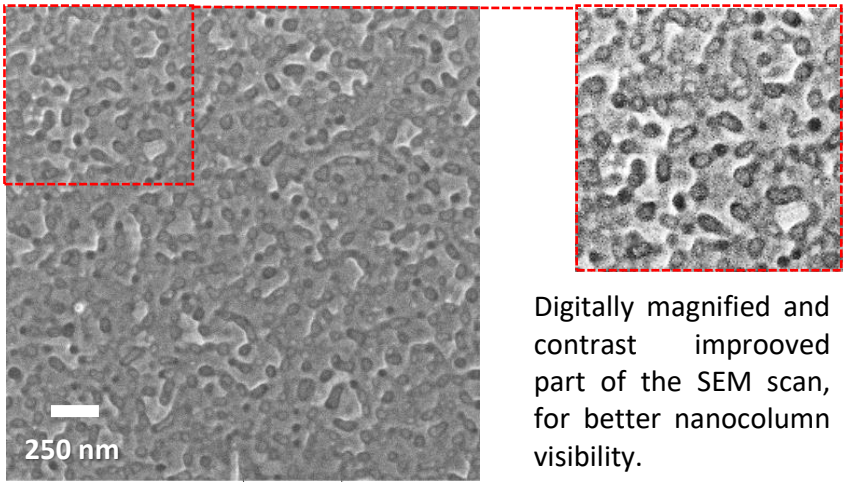


Figure 3.8.: Surface of a re-anodized AAO template prepared with two step anodization. The surface was decorated in selective AAO etchant for 20 seconds for better visibility. The top of the nanocolumns are clearly visible.

3.5 Anodization of Titanium

The anodization of the Ti layer in aqueous oxalic acid solution with sequential anodizing technique was realized. The anodizing process of the Ti layer is starting with the formation of the TiO_2 nanodots at the bottom of the AAO pores on the barrier layer. The speed of the anodic reaction at constant voltage is depending mainly on the electrolyte temperature. Higher is the temperature, the reaction is faster. At higher electrolyte temperature the oxidation process is faster than the growing speed, therefore the nanostructure can be instable and dissolve during the anodization causing a breakthrough across the layer. Due to this phenomenon after several experiments 5°C was chosen as an electrolyte temperature.

Titanium ion migration through the AAO barrier layer is depending on the temperature, on the anodization potential and current. Basic column, which is a titanium dioxide column anodized at potential 40 V as an AAO was prepared, has two main parts, the root and the column itself.

The Ti4+ ion migration through the AAO barrier layer are leading to a growing mechanism. Higher anodic potential leads to a better anodic titanium oxide (ATO) growing and the AAO nanopore filling redounds ATO nanocolumns. However, the anodizing process results titanium oxide growing, also an inward O_2 ion migration appears on the interface of the AAO barrier and Ti layer. (Figure 3.9.)

The I–t curves from the anodization process were presented in chapter 1.3, where the correlation between the anodization time and the AAO thickness was shown. To control how many pores are filled with nanocolumns, the AAO was removed. The pore saturation is around 95 to 100%. (Figure 3.10.) After a partial AAO removal the nanocolumns becomes visible, however the most of the nanocolumns were felt down or removed after a full template removal.

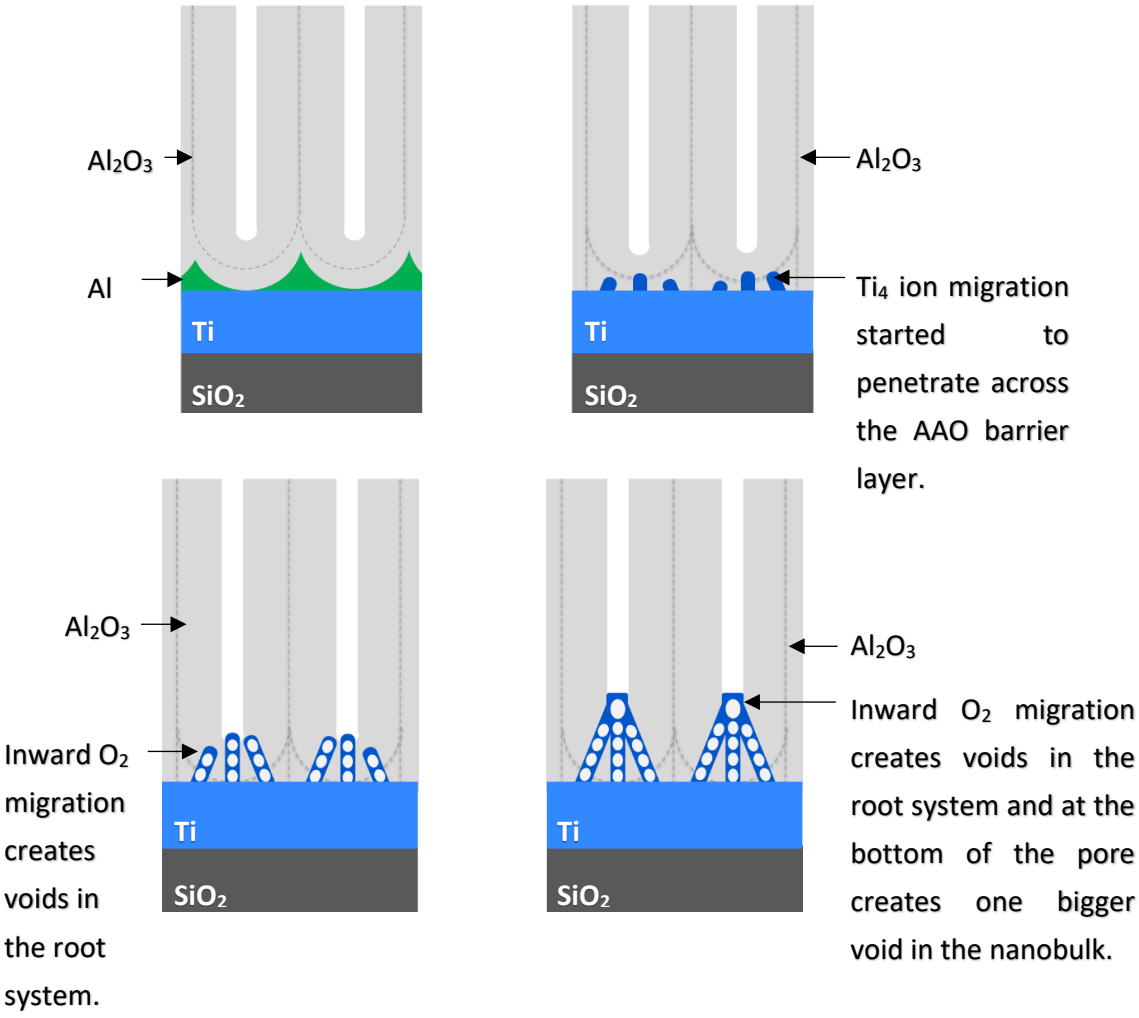


Figure 3.9.: Schematic view of the TiO_2 growing through the AAO barrier layer at potential 40V. During the anodization at first all of Al is anodized (a.), then the Ti starts to penetrate through the barrier layer at the thinnest places respectively at the places with a lowest resistence.(b) The inward O_2 migration creates voids in the stems and later in the cap on the nanocolumn as well.(c., d.)

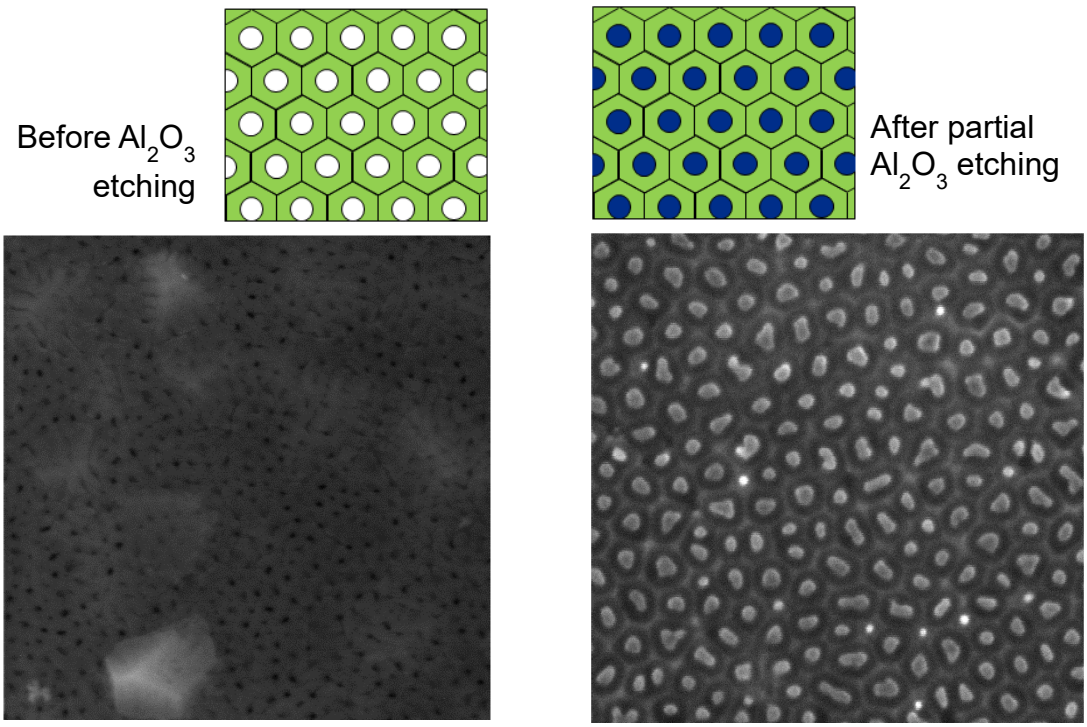


Figure 3.10.: The pore saturation was controlled by a partial AAO removal. The surface of the AAO after the re-anodization (on left) before decoration, and the nanocolumns in the partially removed AAO template (on right). To see the effectivity of the saturation in detail, after an AAO removal only a part of the surface is shown.

The negative effect of the voids, besides the nanocolumns are not stable after AAO removal, is the possible lentil surface during the anodization. Where the sample was ruptured or over-burned due to the high current density in a local point. Based on these experiences at anodic oxidizing we initiate higher amount of O_2, migrating into the barrier layer. The shape of the roots and amount of the root filaments are changing simultaneously. During a long time finishing the voids are merging filling up the barrier layer. Later, the voids are spreading above the Ti layer and breaks up the AAO template. (Figure 3.12. Figure 3.12)

Re-anodizing sweep rate at reaching of the final re-anodizing potential has influence on the grown speed and on the electrical properties of the columns as well. This chapter briefly explain the differences in the grown process at sweep rate difference from 0,2 $V \cdot s^{-1}$ to 2 $V \cdot s^{-1}$.

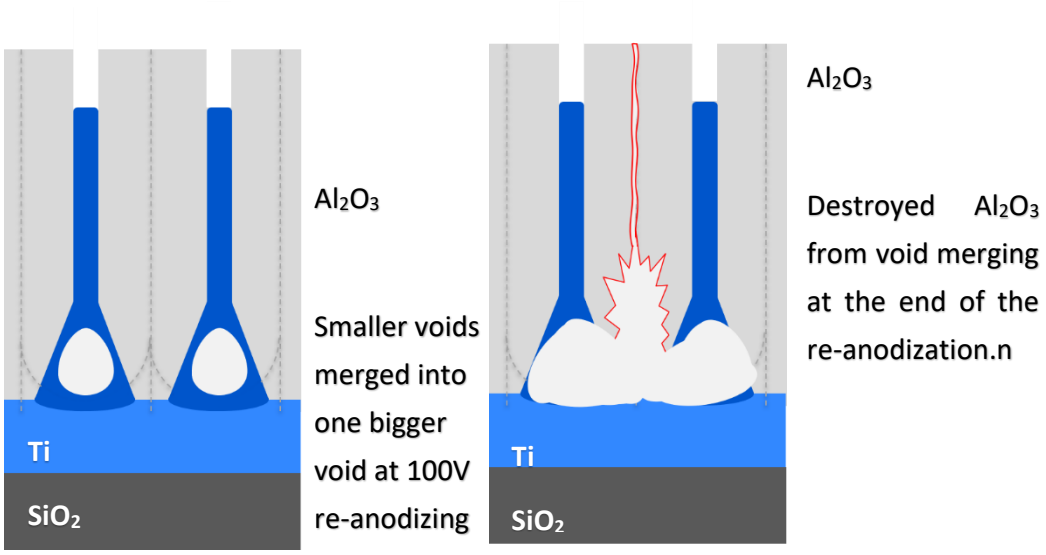


Figure 3.11.: The re-anodization at potential 100V reached at slow sweep rate leads to long nanocolumn growing, but the inward O_2 migration, respectively the voids in the nanocolumn in the AAO pores are not present. The root system in the AAO barrier layer due to the re-anodization is changing its structure. The voids from the O_2 migration are fulfilling the barrier layer and transforms the stem structure into one flask shaped root with 1 to 3 voids. (left) The long-time anodization finishing leads to a void merging between the roots and to a layer destruction. (right)

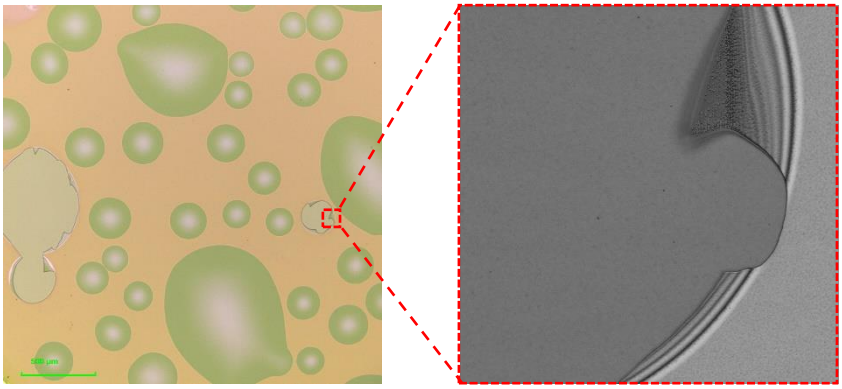


Figure 3.12.: Lentil like damage on the AAO layer caused by long finishing anodization. (left) The magnified damage after eruption is magnified on a laser scanned image (right)

The nanocolumn grown speed is higher and the final nanocolumns are about 10% higher than at lower speed. If the growing process is faster the inward O_2 ion migration is causing bubble merging slower than at lower sweep rate. The nanocolumn can be anodized at higher potential as well (at 130V without any AAO damage).

The different grown speed assuming different material or root structures and electrical properties respectively.

The differences in low and high sweep rate are presented (Figure 3.13), where the anodizing charts are explained the growing phases are illustrated.

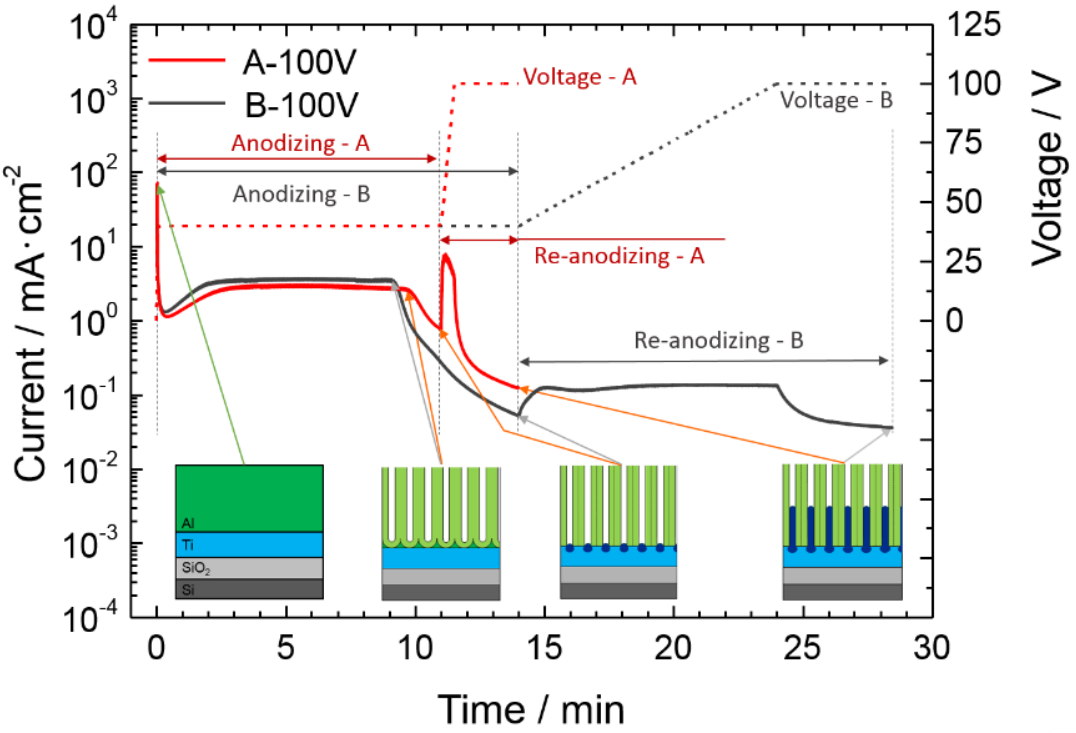


Figure 3.13.: Comparison of sweep rate of re-anodizing potential. Current-time and potential-time transients recorded during the AAO-assisted anodization of arrays A-100V (red) and B-100V (black). The different regions (anodizing and re-anodizing) are marked and the images show schematically the arrays at the corresponding current or potential changes.[43.]

3.6 Deposition of top electrode arrays

This chapter is dealing with the fabrication of the metal contact pads of TiO_2self-ordered nanoarrays for electrical characterization. The bottom electrode of this two-terminal element is the Ti layer itself. The highly conductive pure metal layer is perfectly connected with the nano column array and it is easily accessible from the side of the chip.

The top electrode material based on the literature should be a noble metal, as platinum or gold layer. Regarding to the available techniques and sources electrochemically or magnetron sputtered gold layers were chosen. The magnetron sputtering of Au was performed at standard set ups (prepared in CEITEC Core facilities in form of order) and therefor only the electrodeposition will be discussed in detail.

The AAO surface before deposition was decorated for 10second with *AAO etchant,* later on rinsed in demi water and dried with hot air at 80°C for 2 minutes. The clean and dry micro channels are obligatory for a successful electro-deposition. Every contaminant decreasing the deposition quality and distorting the results form later electrical characterization. The back side and the edges of the chip were isolated by a nitrocellulose-based polymer (nail polish).

The electrolyte tempered for 45°C was stirred in an open electrochemical cell with gold counter electrode. The distance between the working and the counter electrode was 4mm. The continuous stirring serves to keep stable temperature and a constant amount of gold ions above the working electrode.

Deposition set up for pulsed galvanostatic method:

Electrolyte:

- 0.183g $K[Au(CN)_2]$ + 250ml H_2O
- T = 45°C
- Stirring = 300rpm

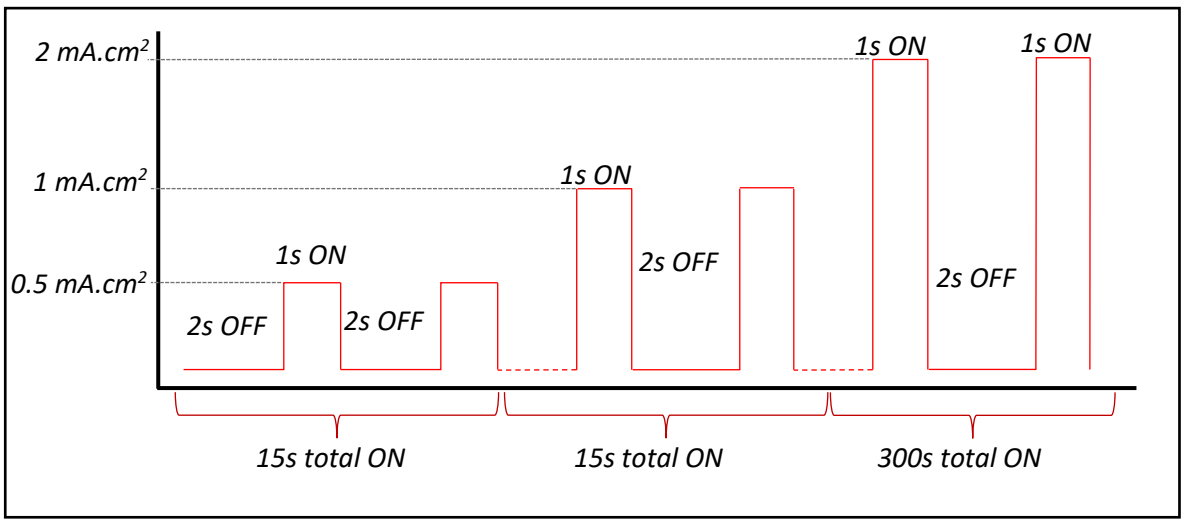


Figure 3.14.: Schematic view on the deposition set up for Au electrodeposition into AAO.

During the deposition three different current pulse limits were used with length 1 s and with relaxation time 2 s after pulses in all cases. The first two low limits serve for soft deposition starting. At low current limit in the pores a very thin gold basic layer can grow. In case of the third current limit, when the electric potential is moving between 3 to 20 V the pores are fulfilled with gold and on the top of the chip is covered by a homogenous gold layer. Stabilization of the top electrode was performed with a 10min long heat treatment at 200°C on a hot plate.

3.6.1 Critical parameters of the deposition process

Electrochemical deposition of gold into pores on oxide layer has few important limits like working electrode conductivity and deposition speed of the gold, which are critical for a successful top electrode preparation.

The electrochemical deposition is a well working deposition method for most of the conductive materials. If the conductivity is low the ion transport can be low, or it is not possible. With heat treatment the conductivity of the TiO_2 nanocolumns can be increased, and they will be suitable for electrochemical deposition. The devices without heat treatment had very low conductivity; they behaved as a dielectric layer and therefore the Au deposition with low current limit was not possible. High current limit (20mA) and higher potential (limited for 100V) started the ion transport but the devices surface was damaged, or the gold was not homogenously distributed on the layer.

High deposition speed can cause similar problem as low working electrode conductivity. The gold is not distributed homogenously; the pores can be sealed at the top of the pores by a fast-growing gold bulks without a primary contact with the bottom oxide layer. The rest of the gold ions will accumulate into bigger bulks, and the rest of the surface will be uncovered. (Figure 3.15)

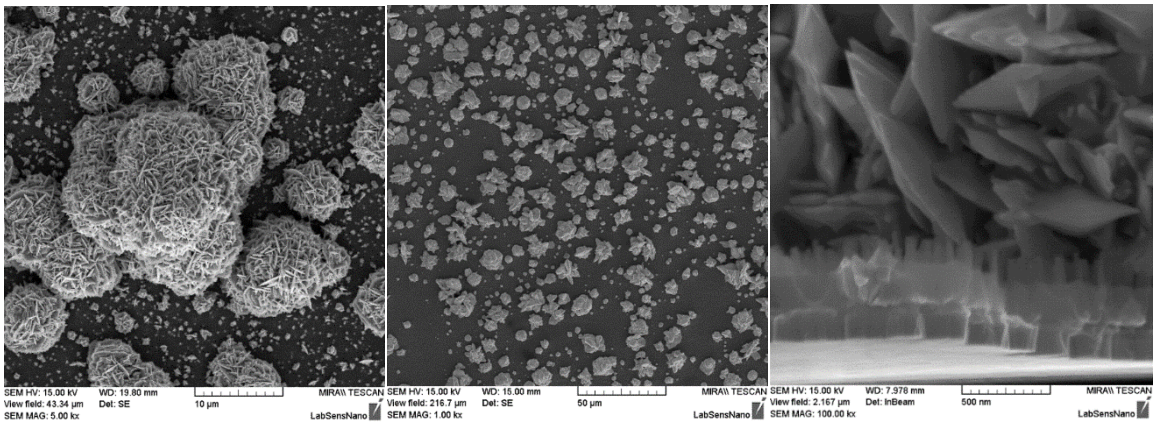


Figure 3.15.: Improper gold deposition set up caused gold bulks on the surface (on left and in the middle) and therefore the nanocolumns are not covered homogenously (right). For evaluation the AAO was partially etched at the sample on the right.

Gold deposition on non-conductive or low conductive surfaces is easily possible with PVD techniques. For gold top electrode preparation, a magnetron sputtered gold layer with thickness 200nm was used. The gold layer was stabilized in a same way as the electrochemically deposited layers, with a 10 minutes long heat treatment on a hotplate at 200°C

The gold sputtering has only one limitation, which is the pore size. There are physical limitations for a full nanopore filling with magnetron sputtering technique and at low pore diameters the Au is not reaching the top of the columns. (Figure 3.16.) All the samples for magnetron sputtering were prepared with a thin AAO matrix where the top of the columns

reached the surface. To ensure better contact, the AAO surface was decorated for 20 seconds in CrO3 based etchant.

Top electrode structure in both cases (for electrodeposited and for sputtered gold as well) were prepared using lithography techniques using top down method.

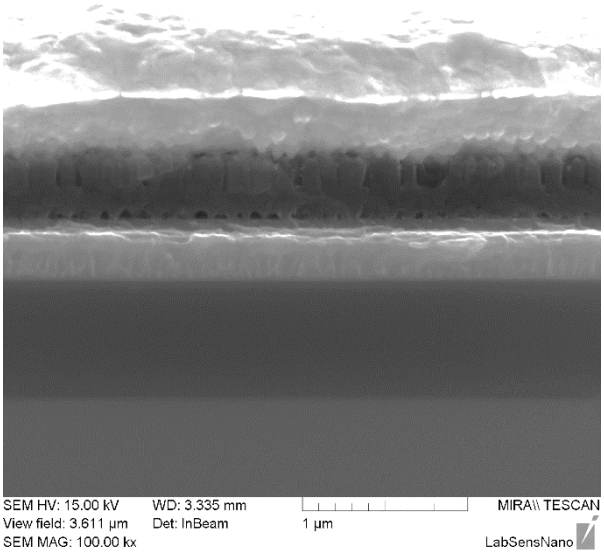


Figure 3.16.: Sputtered gold layer on the top of the AAO template. The galvanic connection between the Au layer and the nanocolumns is 0%. The gold get into the pores only few nanometers. The gap between the nanocolumns and the gold layer is excluding the proper electrical contact, with this deposition method. For sputtered top electrodes the two step anodization may an option.

3.6.2 Lithography

The top electrodes of the chip were prepared using top down method using UVA lithography. UVA lithography with PET-G mask is an easy and trustful technique to realize a polymer protection mask for etching processes at room temperature.

The sample was rinsed in IPA and dried on a hot plate at 80°C for 2 minutes, cooling time of the sample to room temperature was about 1 minute.

The positive photoresist was spin coated on the sample to create uniform film appx. 1,8 um thick.

Table 4.: Spinning parameters:

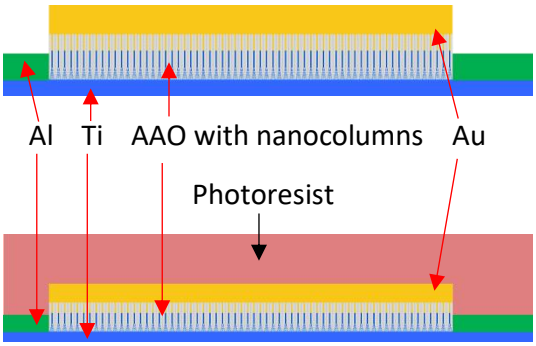
	Rotation speed	Spinning time
Step 1	500 rpm	5 sec.
Step 2	4000 rpm	45 sec.

The soft bake was provided on a hot plate at 100°C for 2 minutes.

The lithography mask was printed on a PET-g sheet with pad size 100x100 um. The layer was exposed with 2500 mJ/cm^2 at 405 nm. After the exposure the post bake at 200°C for 1 minute was done.

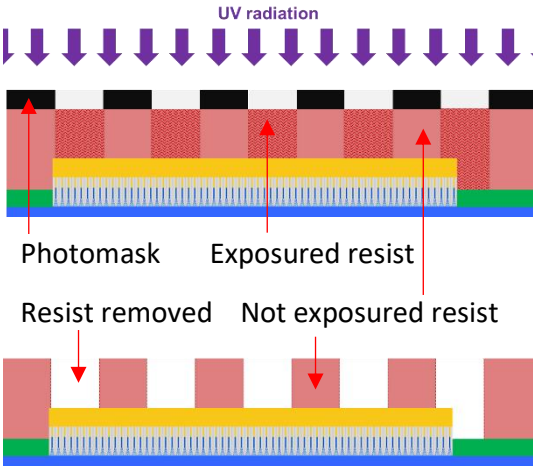
The development of the mask was realized in AZ 327 resist developer for 40 seconds. Hard bake on the resist layer was not implemented.

The lithography process is visualized below. (Figure 3.17.)



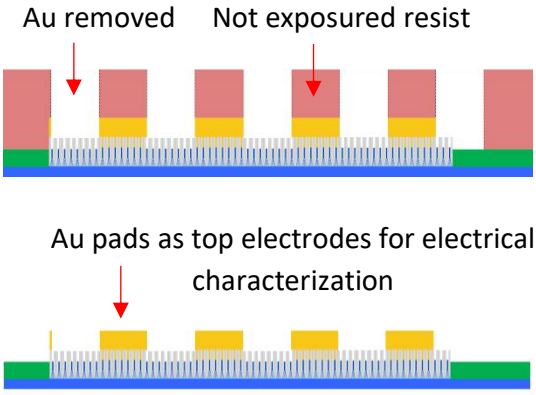
Electrodeposited or magnetron deposited gold layer with thickness min. 200nm, stabilized at 200°C for 10 minutes. The chip was cleaned from polymer residues (used as an insulator of the sides and the back side of the chip) before the resist coating.

Positive photoresist spin coated on the whole surface. The resist thickness after soft baking (60 seconds at 90°C) reaches final thickness about 2um.



Resist exposure with UVA for through PET G photomask. During the exposure a photochemical reaction weakens the polymer structure and it becomes soluble in photoresist developer.

Resist developer removes the exposed layers. Post baking after an exposure is obligatory.



The gold layer was removed with wet chemical etching, using Gold etchant Standard from Sigma Aldrich. The etching time about 5 minutes at room temperature has no negative effect on the photoresist or on the AAO respectively.

The resist mask was removed by Dimethyl-sulfoxide (DMSO). The chip is ready for the electrical characterization.

Figure 3.17.: Fabrication of top electrods *via* top-down method.

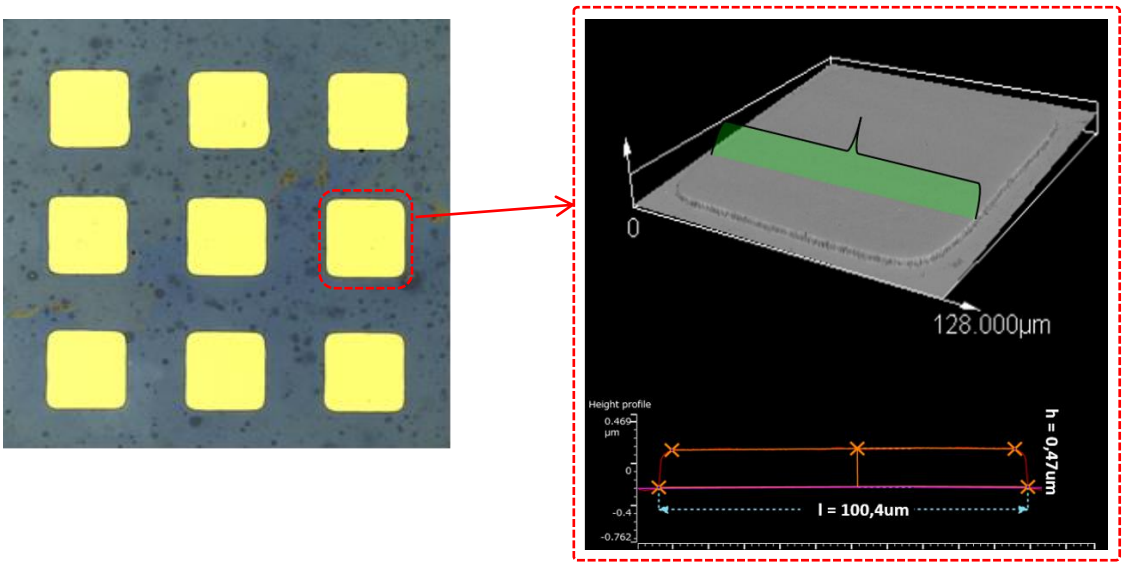
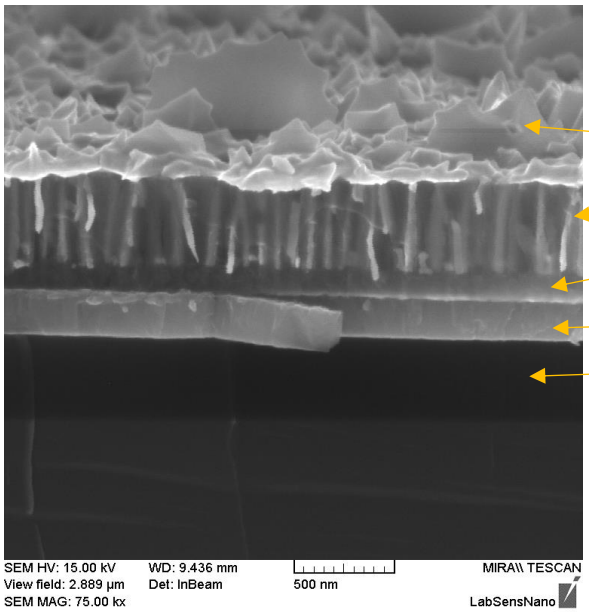


Figure 3.18.: Top contact pads after lithography and Au etching (left). 3D image with dimensions about a top contact scanned by Olympus LEXT OLS 5000 confocal microscope (right).

The top gold contacts after lithography and etching were prepared and measured. The proper electrical contact between the top electrode and the nanocolumns is ensured by fulfilled AAO nanopores with electrochemically deposited gold. The cross section of the sample in place of top gold pad was observed with SEM. (Figure 3.19.) The gold surface contains mostly thin gold flakes, most of the nanopores are homogenously fulfilled with gold, in some pores gold was not deposited or there is no primary contact between the nanocolumns and the gold filling.



SEM cross section image of electrochemically deposited gold plate.

a. Gold on surface,
b. gold in alumina pores,
c. TiO_2 nanocolumns in alumina pores
d. titanium base layer,
e. silicon dioxide

Figure 3.19.: Cross sectional view of the sample with electrochemically deposited gold.

The gold pad after electrodeposition and soft annealing was removed in a mechanical way. The gold in the pores splits off from the top gold pad, and with SEM the gold filling residues are visible. The difference in between the atomic numbers of the Au and the AAO, makes good contrast between the gold and the AAO. The amount of the filled pores was evaluated with freeware software FIJI. Based on the evaluation the saturation of the Au filled nanopores is approximately 60%. (Figure 3.20.) The saturation of the gold contacts at sputtered samples is about 90%, because the columns are reaching the top and the magnetron sputtered Au layer homogenously covers the whole surface.

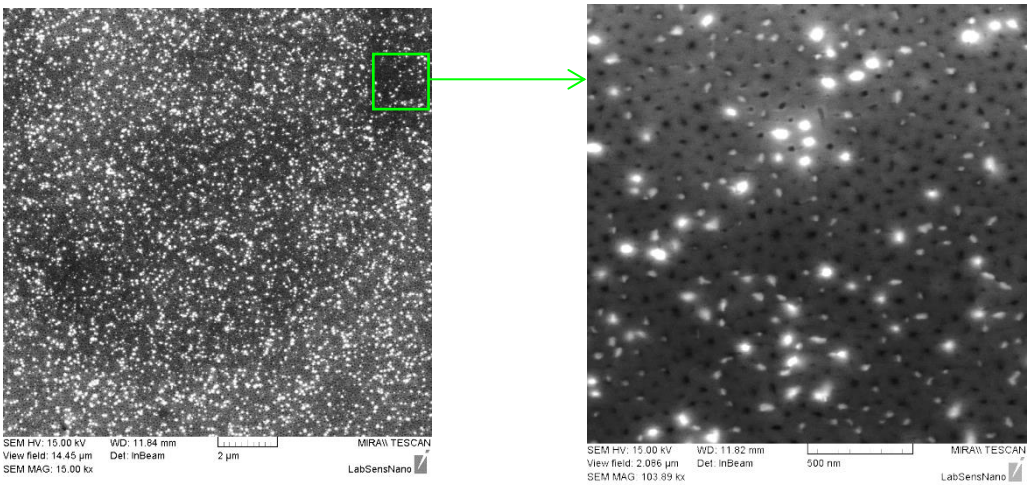


Figure 3.20. Nanopores with electrochemically deposited gold rod residues. The gold layer above the AAO was removed mechanically.

3.7 Material and structure characterization

Electrochemically deposited TiO_2 nanoarrays were analyzed and characterized in detail. Every small change in the preparation set up has direct effect on the self-grown nanocolumns material structure. In next chapter the characterization and the growing process will be written.

Main techniques for layer characterization were chosen SEM, TEM observation and EDX material analysis. SEM microscope Mira II LMU and Lyra 3 from Tescan Orsay holding was used. During SEM analysis the previously cleaned and in case of cross sections chemically decorated samples were observed by SE and InBeam secondary electron detectors were used at working distance 1 to 8 mm with acceleration voltage 15 to 30kV. The sample surfaces were not deposited by a conductive layer before the SEM analysis.

Chemical decoration was provided by a selective aqueous highly toxic etchant 0.6 M H3PO4 and 0.15 M CrO3) at 60 °C respectively for 5 to 20 seconds. The selective AAO etchant in a short time etches the AAO surface and at cross sections the walls of the AAO pores, therefore the contrast between the TiO_2 nanocolumns and the AAO is improved

The TEM samples were prepared on FEI Helios FIB/SEM microscope and analyzed on FEI Titan transmission electron microscope.

Observation, analysis and evaluation of selected samples were subjected to fast furrier transform (FFT) analysis for determination of crystallographic orientation in the columns, roots, AAO matrix and in pure Ti layer as well.

FFT imaging and final image processing was performed by software FEI TEM Imaging and Analysis ver. 4.14.

EDX investigations were performed by a high sensitivity FEI Super-X detector. The observed are was scanned with a with the 300 kV electron beam and using a beam current of 0.15 to 0.5 nA, dwell time of 20 µs, and a spot size 0.3 to 1 nm. The thickness of the lamella under the observed surface was always about 50 nm or lower.

Quantitative evaluation of the data was completed with FEI software Velox version 2.2.1. Over selected parts of the anodic films and within the lines along selected nanocolumns a data integration was performed.

3.7.1 TEM sample preparation

The chip was rinsed with IPA and dried under nitrogen flow to remove incidental dust or other solid particles. Sample holder for FIB microscope used for fixing conductive carbon tape. After loading the sample into the microscope chamber the chased area was covered with platinum sacrifice layer by ion beam deposition from gas precursor. The platinum layer is protecting the oxide layers from the non-desirable backscattered or non-focused gallium ions. A rough milling was performed at 30 keV, followed by a final polishing at 5 keV. The milling and polishing sequence is briefly visualized below. (Figure 3.21.) The final lamella with thickness up to 50nm is suitable for the observation by FEI Titan Themis 60–300 TEM at acceleration voltage of 300 kV in bright-field mode.

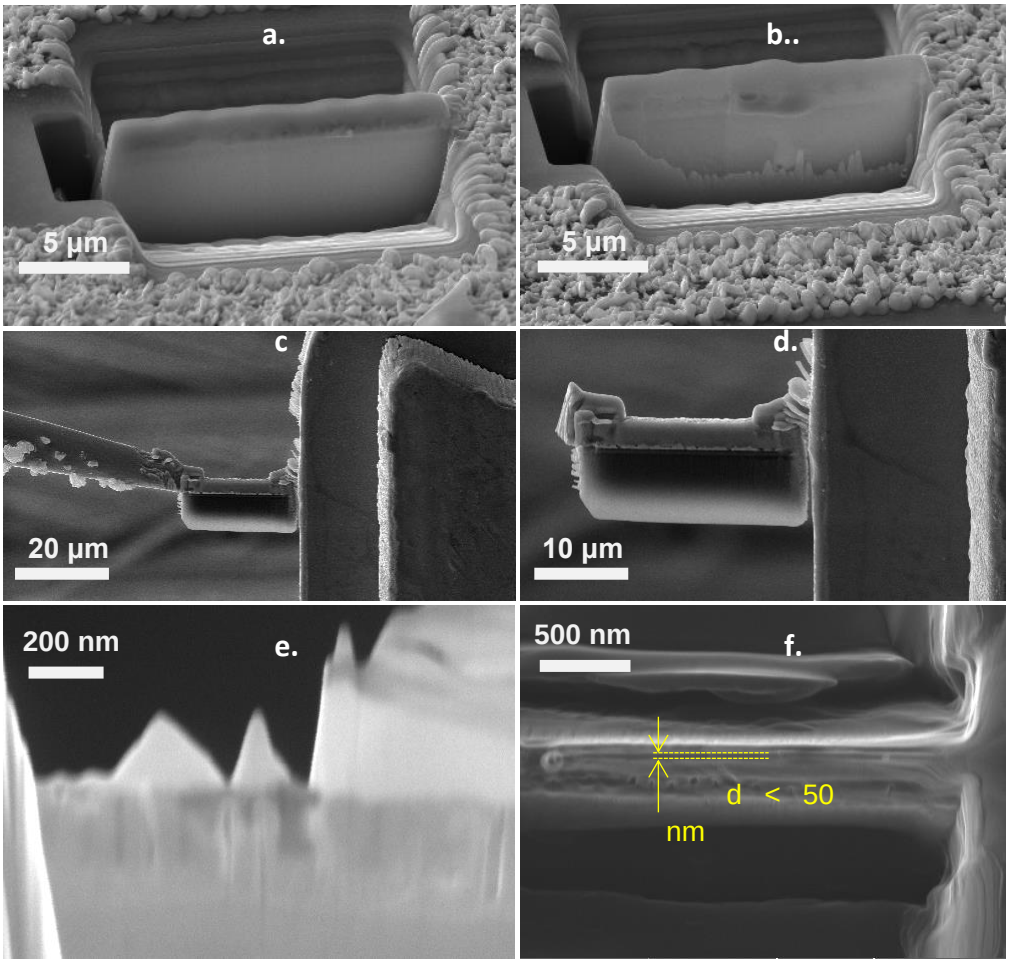


Figure 3.21.: Lamella preparation for TEM analysis. Sample after rough milling with preset current > 5nA (higher is the current, higher is the milling speed) (a.). Edges of the milled area are deformated/melted due to high milling energy, the structure under the Pt layer is untouched. (b.) Rough milled and under-cut lamella is soldered on the Cu grid holder. (c.,d.) Fine milling is removing material at low speed but high precision. The low milling current ~1nA is thinning the lamella close to the final thickness. After fine milling the lamella is at thickness ~100nm or less. Last step of the lamella preparation is the polishing on the final thickness (polishing current <0.8nA) (f.). To improve contrast the both side of the lamella is fine polished with current 0.1nA. (e)

3.7.2 Material characterization by TEM and EDX

The structure of the AAO layers was written in previous chapter. Regarding to the same preparation conditions of the AAO templates in every case, the barrier layer properties are considered constant for all experiments.

Anodization of the Ti layer starts , when the barrier layer of the AAO matrix reaches the top of the Ti layer.

Titanium ion migration through the AAO barrier layer is depending on the temperature, on the anodization potential and current. Basic column, which is a titanium dioxide column anodized at potential 40 V as an AAO was prepared, has two main parts, the root and the column itself.

Everything between the pure titanium layer and the bottom of the pore is considered as a root. (Figure 3.22.) In current case the characteristic root stems are penetrated through the barrier layer. Number of the root stems is obviously depending on the anodization potential and on the barrier layer properties, such as thickness, surface of the bottom of the pore, etc.

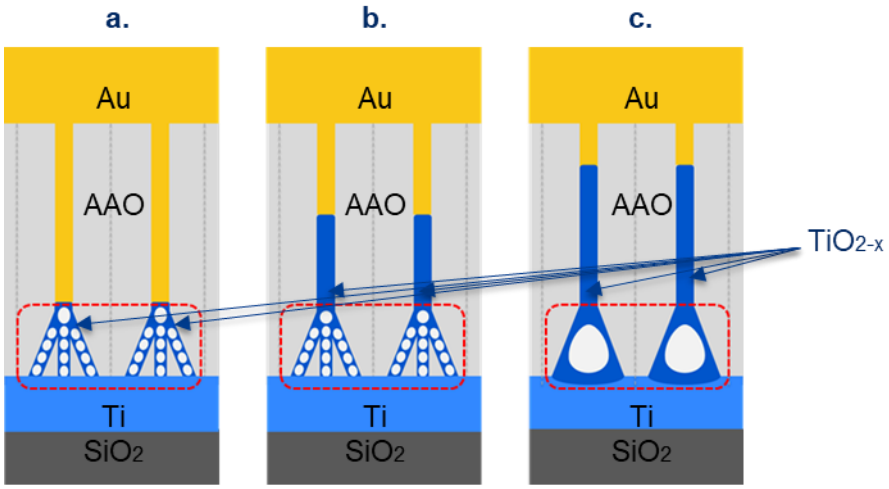


Figure 3.22. Schematic of the nanocolumns at different anodizing potential: 40V (a.), 60V (b.), 100V (c.). The roots are marked with dashed red line.

Various possibilities of using of TiO_2 nanocolumns sensor or photovoltaic techniques motivated to observe columns after the AAO removal. The AAO was removed by selective chemical etchant at 58°C and the column field was observed by SEM. After AAO removal there were no nanocolumns visible on the surface. This is because of the nanoroots that connect the columns with the bottom Ti layer are undergo a modification during the re-anodizing, owing to the oxygen evolution followed by creating of nano-bubbles and voids, and grow as an alumina contaminated TiO_2 nanoroots in the barrier layer. This small amount of alumina in root walls and the extremely thin wall thicknesses next to the voids caused 100% column devastation. We can consider the pure titanium layer is not suitable for mechanically stable AAO less TiO_2 arrays grown by anodic oxidation technique. More detailed information about the mechanical stability was published in article *Influence of*

*nitrogen species on the porous-alumina-assisted growth of TiO_2 nanocolumn arrays (Bendova, Kolar, **Marik** et al).*

The shortest and the longest nanocolumns anodized with one step anodization at 40V (shorter) and re-anodized at 100V (longest) and annealed for 2h at 500°C in vacuum were investigated in structural and material point of view. The nanocolumns re-anodized at 100V without annealing (as-anodized) and air annealed were observed as well.

Crystallographic orientation in different materials was measured in TEM by fast Fourier transform (FFT) analysis, results were evaluated by FEI software TEM Imaging and Analysis version 4.14. Diffraction images are showing local crystallographic orientation. (Figure 3.23.)

In case of Si wafer and Ti layer the results were compared with the wafer datasheet and with results from Gablech et.al. [78.] about preparation of (001) preferentially oriented titanium thin films by ion-beam sputtering deposition on thermal silicon dioxide.

The p-type Si substrate with orientation (111) was observed as a first. The diffraction image shows the perfect (111) orientation. The thermal oxide layer followed the substrates crystallographic orientation.

The Ti layer sputtered by IBAD shows (001) orientation and the AAO was completely amorphous.

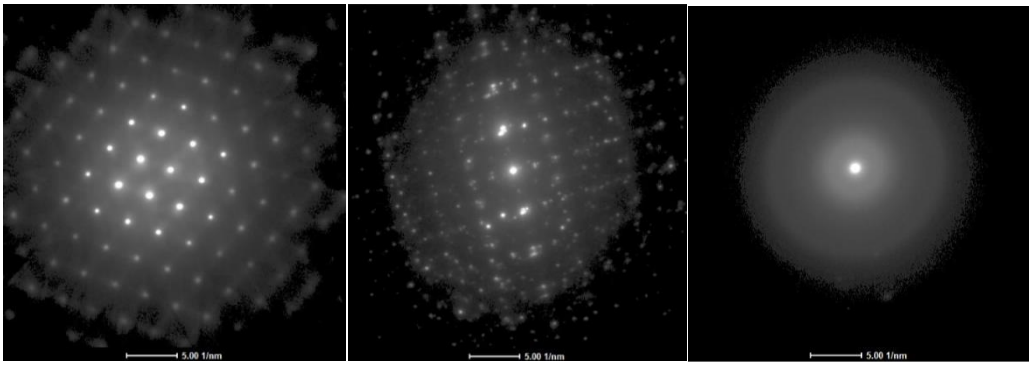


Figure 3.23.: Crystallographic orientation in silicon wafer (111) (a.), in sputtered Ti layer (001) (b.) and in AAO [amorphous](c.) was measured in TEM by FFT analysis. The AAO kept their amorphous character after annealing in vacuum and in air as well.

3.7.3 Characterization of nanocolumns anodically grown at 40V

The root structure at anodization potential 40V is non-homogenous. The root system contains one main stem at the bottom of the pore, where the barrier layer has the smallest thickness and 2 to 5 side stems. The stems are full of voids (full of nano-bubbles), which has significant influence on the column stability after the AAO is removed. The thickness of the stem walls next to the voids are about 1-2 nm. The diameter of the main stem is about 9 to 10 nm, and the side stems are 4 to 6 nm in diameter. The length of the stems is depending on the AAO barrier layer thickness, which is about 36 to 40 nm. (Figure 3.24.)

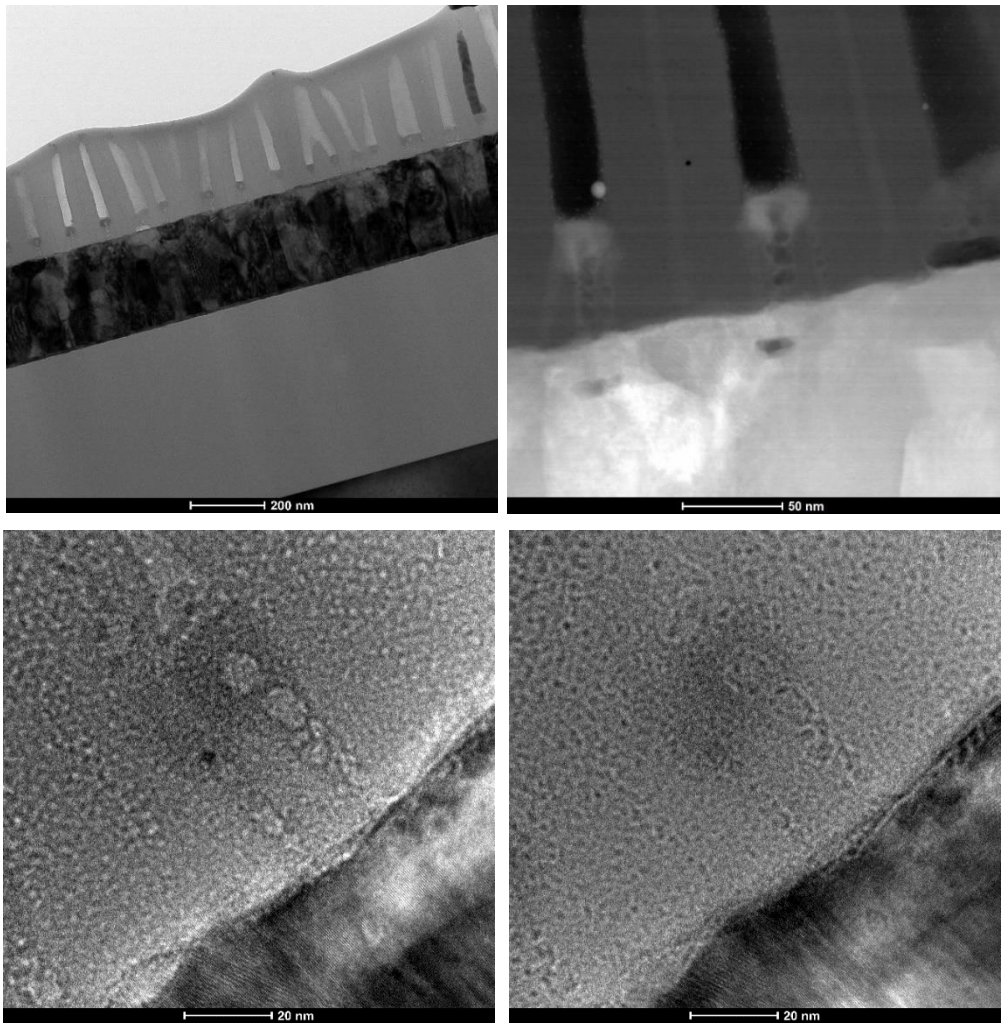


Figure 3.24.: Wide field scan with TEM about the nanocolumns in AAO. One nanopore obviously contains one nanocolumn, but rarely a nanopore can be divided in two sub pores or two pores can merge during anodization as well. (a.). Magnified view on a short nanocolumn with root system contains void full stems. (b.) Verifying of voids with under and over focusing of the electron beam during the column observation. With under focusing the surface and with under focusing the edges are visible.

The TiO_2 nanocolumns were studied using FEI Super-X detector by scanning a selected nanocolumns from the lamella with the 300 kV electron beam. To achieve the best scanning parameters a beam current of 0.15 to 0.5 nA was used with dwell time of 20 µs, and a spot size 0.3 to 1 nm.

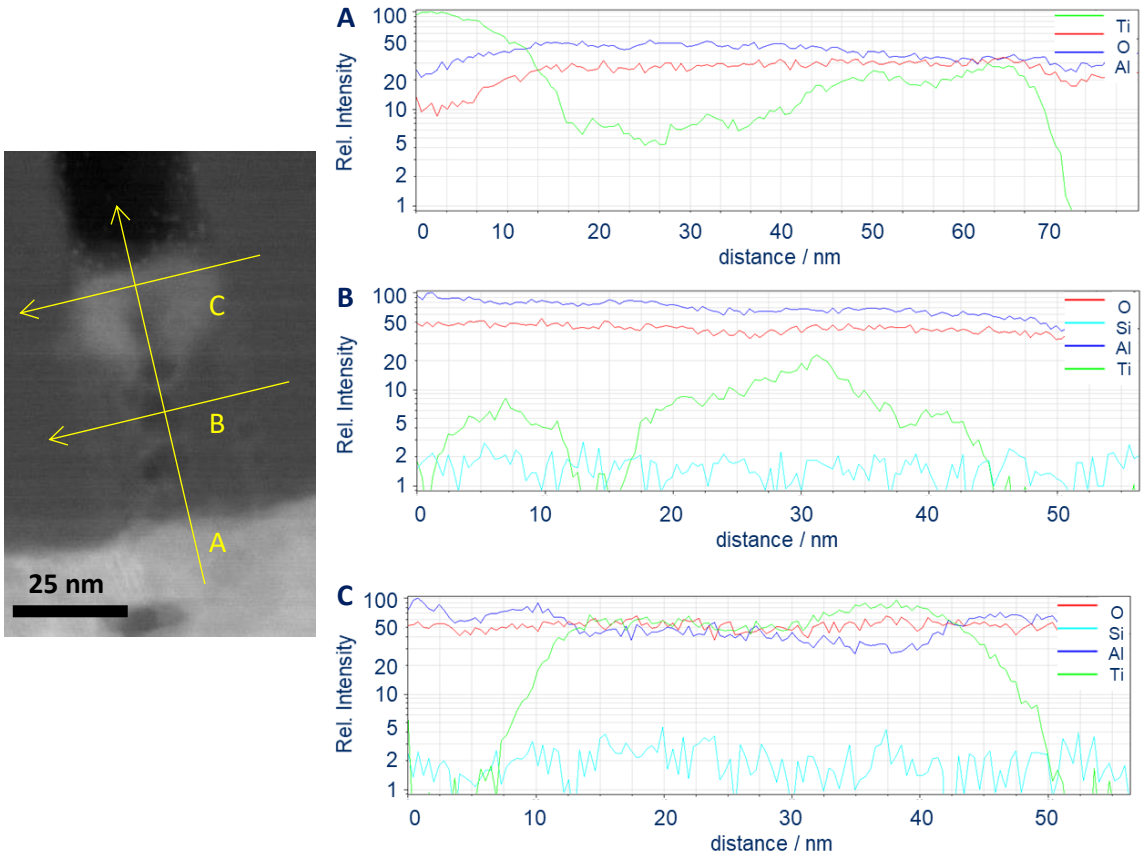


Figure 3.25.: EDX line scans performed on the TiO_2 nanocolumns at three different positions. The line A dealing with a nanocolumn material structure from the Ti layer to the AAO pore. Line scans B and C were collecting material information though the nanocolumns root system (B) and through the top of the column (C).

The EDX line scans about the 40V sample presents distribution of Ti in the nanocolumn. (Figure 3.25.) The results from a vertical analysis are showing non-homogenous distribution of Ti in the root system. The Ti penetration scheme through the AAO barrier layer during anodization was influenced by the electrical resistivity and by the mechanical properties of the barrier layer. Lower resistivity allows better growing possibilities of the TiO_2. Closer to the top of the barrier layer the amount of the Ti in the root system is increasing. The edges of the TiO_2 in the barrier layer during the anodization may slightly mix with an AAO. The O_2 inward migration is visible on the line scans too.

The horizontal scans about the root system are presenting three or four stems, where the middle stem with a bigger diameter, about 22 nm, can be considered as a main stem. The side stem on the left side with diameter appx. 11 nm is clearly separated, however on the right side the stem is close to the main stem and it is slightly backwards. The fourth

possible stem can be placed at position 16 to 24 nm in the line scan, because the Ti line is not continuously decreasing, however the stem on the TEM figure is not visible.

The EDX elemental maps of Ti, O, Al are presented as well. The roots of the nanocolumns are shown amorphous character in as-anodized, in vacuum annealed and in air annealed condition as well. The amorphous character of the nanocolumns on the HR-TEM image is corresponding to the FFT image. The (001) oriented Ti layer confirmed by FFT image is visible under the nanocolumn on the HR-TEM image.

The EDX elemental maps are corresponding to the line scans. The distribution of the Ti in the barrier layer confirms the root structure. Due to the small stem wall thicknesses and the anodizing conditions the AAO and TiO_2 mixture in the walls is possible. Additional oxide layer under the nanocolumn and between the border of the Ti layer was not observed by HR-TEM and neither by EDX elemental maps. (Figure 3.26.)

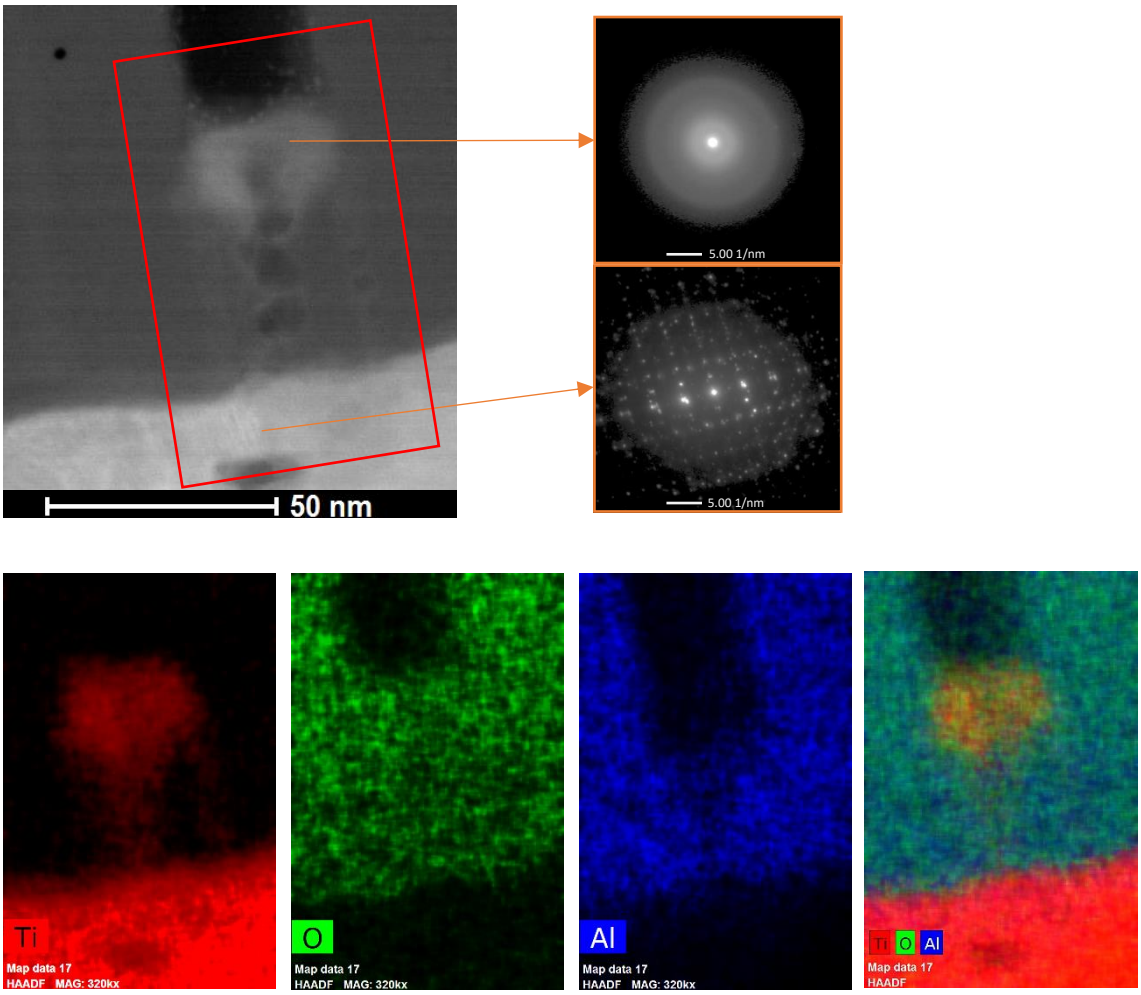


Figure 3.26.: EDX elemental maps about the nanocolumn anodized at 40V. (b,c,d,e) On the HR-TEM image (a) in the Ti layer a crystallographic orientation is visible and it was confirmed by FFT(g). The top of the nanocolumn has amorphous character (f) similarly to the AAO.

Electrodeposited gold was observed by HR-TEM and EDX as well. The nanopore is filled perfectly, the gold filling is homogenous without voids or cracks. Between the top of the nanocolumn and the electrodeposited gold is direct contact overall the TiO_2 surface. EDX line scan from the Ti to the top of the Au column was investigated. The results of the analysis proved the TiO_2 nanocolumn is not mixed with the Au column. In the line scan approximately from 85nm to 95nm the elemental lines are covering each other. This phenomenon is caused by a convex shaped top of the nanocolumn. The convex shape of the column is used to be visible on the HR-TEM images, if the TEM lamella is polished through the nanocolumn. (Figure 3.27Figure 3.27.)

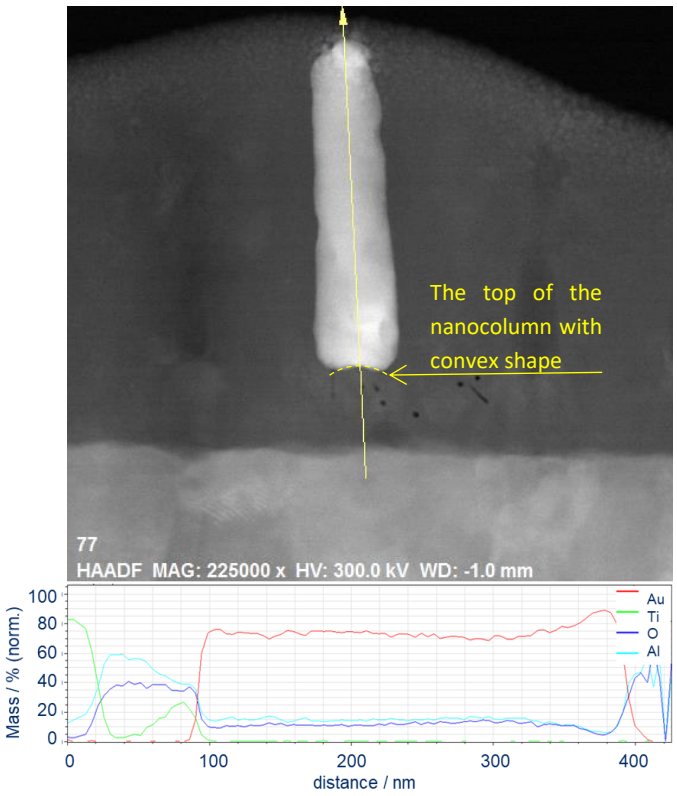


Figure 3.27.: EDX line scan overall the nanocolumn and the electrodeposited gold column. The convex shape on the top of the nanocolumn is marked with yellow dash line.

3.7.4 Characterization of nanocolumns re-anodized at 100V

HR-TEM observation shown significant differences between samples anodized only at 40V and samples re-anodized at 100V.The growing mechanism of the AAO was already written above and published as well by many researchers, as Mozalev, Habazaki, etc. The growing mechanism of the TiO_2 nanocolumns in presence of water based oxalic acid solution brings several changes in column structure, especially in root structures.

From top down view the column structure in AAO pore is homogenous, the length of the column depends mainly on applied potential. The higher is the potential, the longer are the columns.

Re-anodization increases the column length about $1.6nm \cdot V^{-1}$ of re-anodization potential (re-anodization at 100V = 40V basic potential + 60V re-anodization potential with sweep rate $0,2V \cdot s^{-1}$).

The top $\frac{2}{3}$ of the column length is a void less amorphous $TiO_2 + TiO_{2-x}$ combination where the Oxygen content increases in the direction of the surface.

The bottom $\frac{1}{3}$ contains low number of smaller voids penetrated from the root into the column.

The root structure due to re-anodization is transforming into a simpler structure. The stems are obviously missing, with higher potential the stems are merging, the voids are expanding and merging as well, and it lasts until the main root contains 1 to 3 bigger voids with width about 65 to 70 nm. If the re-anodizing potential is too high, the voids expands through the AAO sides and they merge into bigger bubbles, which destroys the AAO layer.

The nanocolumns re-anodized at potential 100V without annealing were already published in article *Influence of nitrogen species on the porous-alumina-assisted growth of TiO_2 nanocolumn arrays (Bendova, Kolar, **Marik** et al).* where a crystallographic orientation of the nanocolumns with FFT was presented. The bottom of the roots, under the border of the Ti layer, reveals presence of nano-crystallites, however the rest of the nanocolumn had amorphous structure. (Figure 3.29.)

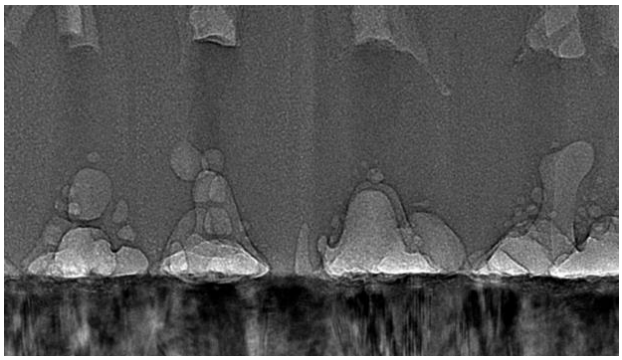


Figure 3.28.: HR-TEM image about the merged voids in the root system. The stems are transformed into one bell shaped root.

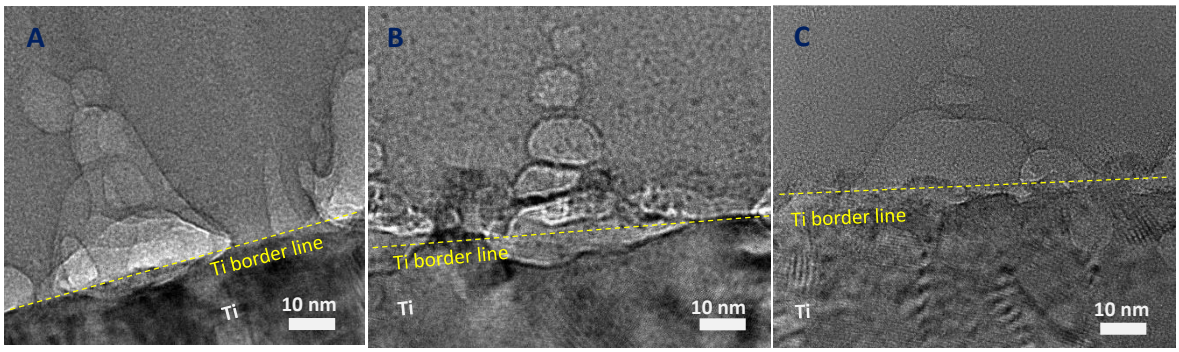


Figure 3.29.: HR-TEM images about the roots of re-anodized samples at 100V in as-anodized (A), vacuum annealed (B) and air annealed (C) conditions respectively. The crystalline structure of the Ti layer is visible with a nano-crystallites at the bottom of the roots under the Ti border line. The rest of the columns has amorphous structure.

The re-anodized samples were annealed in different conditions, therefore the oxygen distribution in the nanocolumns may change. The as-anodized sample considered as initial structure was observed by HR-TEM and EDX as well. Due to the low lamella thickness we can consider the observed nanocolumns were in one line and the scanned spectrum was not affected by other columns behind. EDX elemental maps of Al, Ti and O about the as-anodized samples were already published. Thin oxide layer at the bottom of the roots was compared with HR-TEM image, the thin oxide layer is under the Ti border line. This kind of disposition explains the above-mentioned nano- crystallites which are crystal residues from the Ti layer, mixed with amorphous TiO_2. The area of the oxide layer with nano-crystallites can be considered as an affected zone of anodic oxidation and the depth of the oxide under the Ti border line is considered as oxidizing depth. The oxidizing depth for as-anodized samples (re-anodized at 100V) is about 5 nm. Between the AAO and the Ti there is no affected zone and therefore the oxidizing depth for Al in Ti is 0nm. (Figure 3.30.)

Samples annealed in vacuum at 500°C for 2 hours and samples air annealed at 500°C for 2 hours respectively, were observed by TEM and EDX similarly to as-anodized samples. The heat-treated samples were re-anodized at 100V into a thin AAO, appropriate for sputtered Au top contacts. The initial Al layer after anodization reached a thickness which corresponded to a re-anodized TiO_2 column length. Before the lamella preparation a top Au contact was sputtered on the vacuum and air annealed samples, with a thickness about 200 nm. (Figure 3.31.)

The root system compared in Figure 3.29. showing a similar root structures with a few nanometers thin oxide mixture under the Ti border line. The top of the columns is different at annealed samples in comparison with as-anodized one. The as-anodized nanocolumns were re-anodized in a thick template, where the end of the columns has convex shaped top and they are located deeply in the AAO nano pores.

The annealed nanocolumns due to the thin AAO are branched or widened at the top of the template. The disposition of the pores at the beginning of the Al anodization forms some

thin pores which are merging in depth appx. 40-50 nm under the surface. This phenomenon leads to wider TiO_2 column tops.

The sputtered gold layer perfectly covers the nanocolumns, on the elemental maps there is no Au penetration into the TiO_2, however gold contaminants appeared on the side of the lamella at air annealed sample. This kind of contaminations are residues from lamella polishing.

The column length at both annealed parts are about 130 nm, measured from the Ti border line up to the top of the columns. The columns are affected by voids up to height 45-50 nm, measured from the bottom oxide under the borderline. Similarly, to the as-anodized sample, for the bottom oxide with nano-crystallites appx. 5 nm thickness was measured for both annealed samples, however the EDX elemental maps are shows for air annealed columns affected zone deeper than 5nm.

The samples were observed in STEM mode with bright field and dark field preset as well, where the differences between the vacuum annealed and air annealed affected zone were realized.

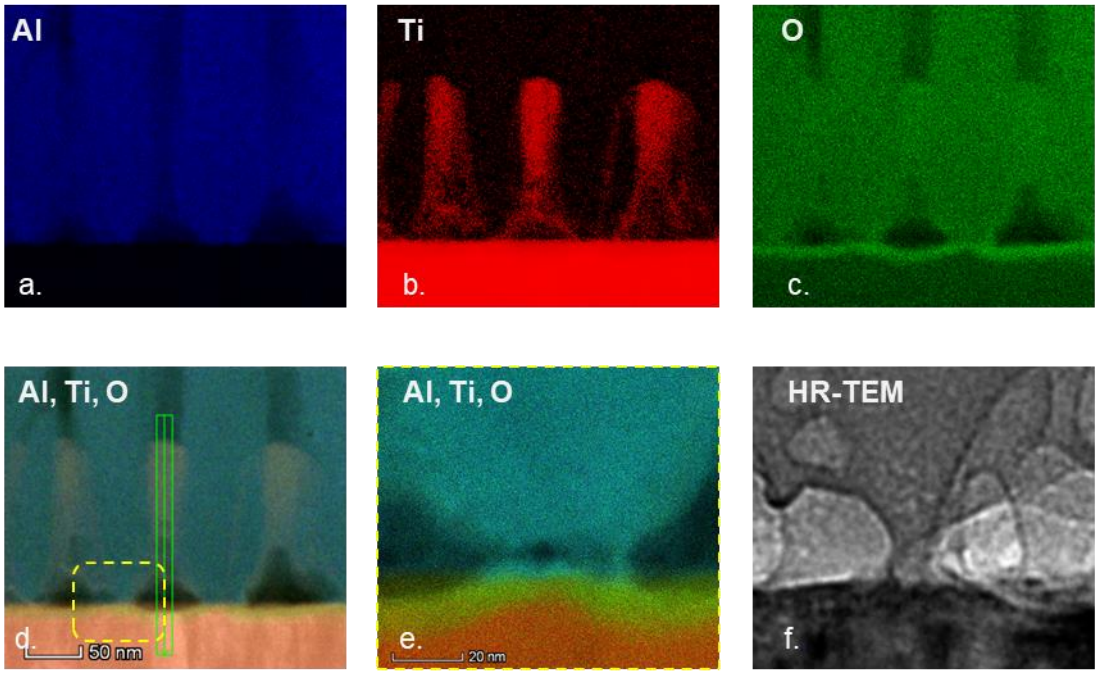


Figure 3.30.: Elemental maps from EDX analysis shown the distribution of the Al (a.), Ti (b.), O (c.) in the lamella from as-anodized sample. The position of the bottom oxide under the Ti border line is presented (d.), for better visibility magnified (e.). The nano-crystallite structure is visible on the HR-TEM image as well.

Under the air annealed roots in depth 10 to 20 nm a void zone was detected. The gap between the Ti border line and the void zone is crystalline Ti. This kind of inward oxygen migration during the anodization was not detected, respectively the vacuum annealed columns are consisting only bottom oxide with nano- crystallites.

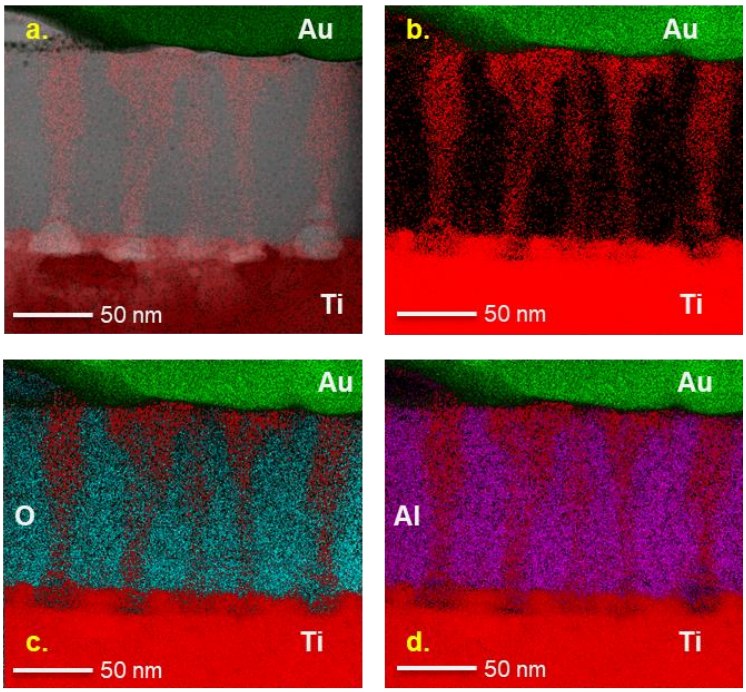


Figure 3.31.: Elemental maps about the nanocolumns after vacuum annealing. The STEM image fitted with elemental maps of Ti and gold shows the distribution of the Ti in the columns and the contact between the Au and the TiO_2 columns. (a.) Fitted maps without STEM image in combination of Ti – Au (b.), Ti-O-Au (c.), Ti-Al-Au (d.) are presented as well.

Responsible for such a deep oxygen migration can be only the air annealing. Air annealing is used for reduction of oxygen vacancies and during a heat treatment. At high temperature if the metal oxide is in reduced oxygen state it tends to balance the O_2 amount from the air. Through a saturated oxide the oxygen migration is possible in few cases. The nanocolumns prepared by anodic oxidation has amorphous structure with different oxygen proportion through the length of the column, moreover the roots are full of oxygen voids. The oxygen from the air penetrated through the amorphous columns and forced the O_2 voids under the bottom oxide layer. The distribution of the voids in the zone is not homogenous and their sizes are not steady as well. (Figure 3.32., Figure 3.33.)

The TiO_2, grown by anodic oxidation, obviously is a very good insulator. The vacuum annealed nanocolumns during the annealing were not crystallized, however the raise of their electrical conductivity was significant. The explanation for this phenomenon is the oxygen reduction in the columns which increases the amount of the oxygen vacancies.

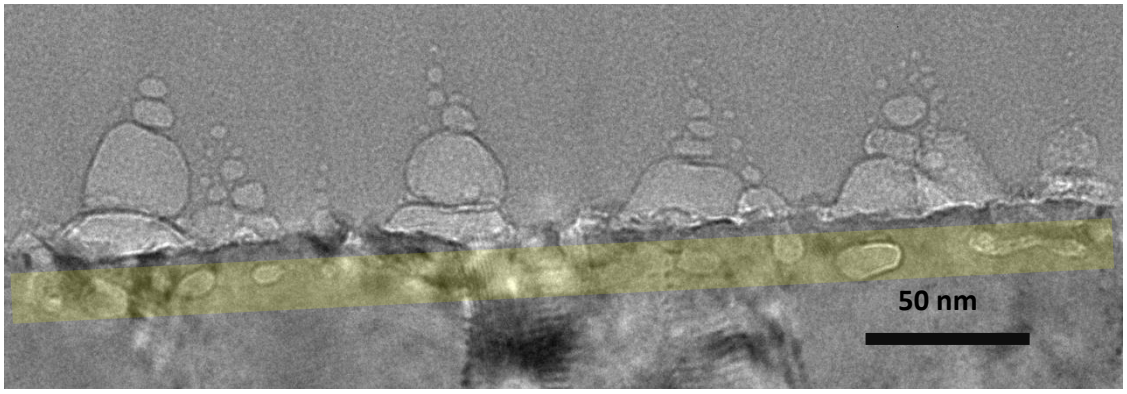


Figure 3.32.: Void zone under the air annealed columns is a unique and unexpected phenomenon found in depth 10 to 20 nm. The zone is highlighted with a transparent yellow band.

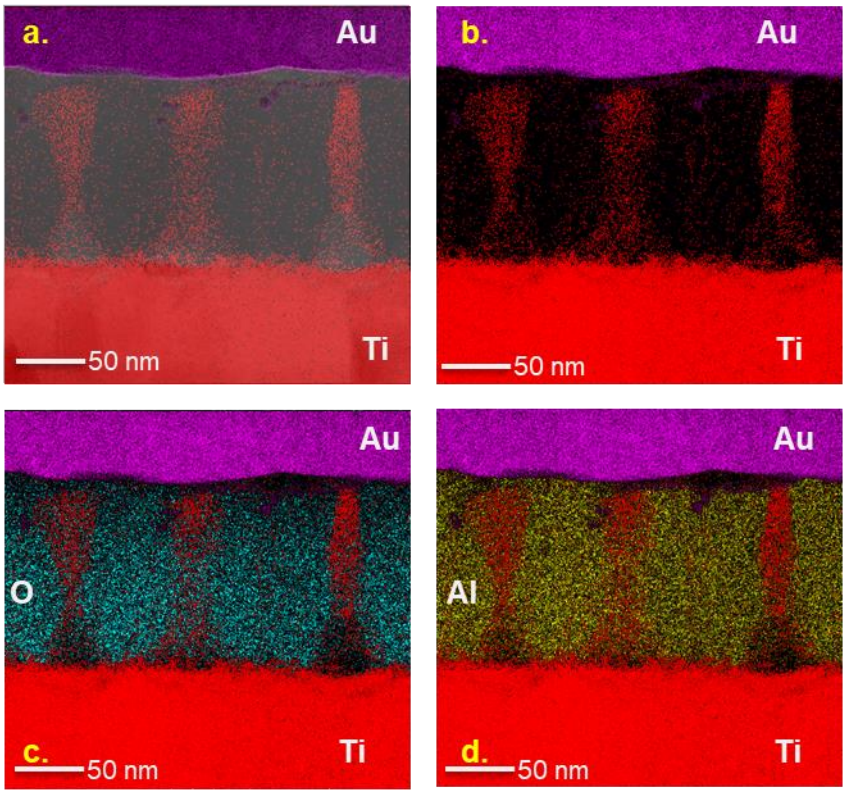


Figure 3.33.: Elemental maps about the nanocolumns after air annealing. The STEM image fitted with elemental maps of Ti and gold shows the distribution of the Ti in the columns and the contact between the Au and the TiO_2 columns. (a.) Fitted maps without STEM image in combination of Ti – Au (b.), Ti-O-Au (c.), Ti-Al-Au (d.) are presented as well.

3.8 Electrical Characterization

This chapter is dealing with electrical characterization of devices with TiO_2 nanocolumns. Every field of nanocolumns under one Au pad is considered as a two terminal electronic device. To identify the basic parameters and to get acquainted with the electrical behavior of the TiO_2 based MOM devices the current-voltage characteristics were measured and presented. The electrical characterization and the calculations of the Schottky barrier height are written below for some selected samples, however the characterization of the nanocolumns grown at sweep rate 2 $V \cdot s^{-1}$ is quoted literally from article *Resistive switching in TiO_2 nanocolumn arrays electrochemically grown (Marik et al)*. [*3.8.1 Quotation 1*]

The top electrodes were prepared with top down method, where the same photomask was used for every sample. To minimize the fails and the irrelevant results during the electrical characterization, the surface of the gold pads was measured with optical microscope. During the lithography and the chemical etching, the size of the top electrodes can be different, therefore the results are presented after recalculation of value of the electrical unit on a top electrode surface (as $A \cdot cm^{-2}$ or $\Omega \cdot cm^2$).

The initial cycle (the first cycle) usually can be considered as a forming cycle, especially if a current drop or jump is appeared. Initial cycle without current drop or jump was repeated on another device with higher potential up to 20V or up to reaching the current compliance level.

The potential for the consecutive cycling is always chosen based on the current jump/drop potential rounded up to a whole number in the forming curve.

3.8.1 Quotation 1.: Electrical characterization of nanocolumns electrochemically grown at sweep rate 2 V·s^{-1}.

The electrical characterization was performed at room temperature using a Keithley 4200 SMU system connected to a CASCADE M150 probe station with magnetic micromanipulators, by recording I(V) curves with a scan rate of 100 mV·s^{-1} from 0 to +5.0, then to −5.0 and back to 0 V in each cycle. To avoid damage of the microcells, the current compliance limit was set to 100 mA. The top Au pad was biased in all I(V) measurements, while the bottom Ti layer, remaining after the PAA-assisted anodizing and being common for all devices prepared on a single chip, was grounded. The measured current and the calculated resistance were related to the projected area of the microcells.

Typical initial I(V) characteristics of the arrays A (i.e. having the higher potential sweep rate during re-anodizing) processed to different final potentials are shown in figure 3a in a logarithmic representation to emphasize the differences between the samples. Each of these arrays, comprising TiO_2 nanocolumns of various lengths, reveals non-linear shape of the corresponding I(V) curve, also showing substantial current drops and jumps for the 70V and 130V arrays and an asymmetric diodelike behavior for the A-100V and A-130V samples. The initial resistance at 0 V (Rinitial,0V) increases with increasing re-anodizing potential, from ~0.25 Ω·cm^2 for sample A-70V to ~7.5 Ω·cm^2 for both A-100V and A-130V arrays. Further I(V) cycling (see figure 3b) shows again non-linear characteristics with an increased current density as compared with the initial state, being asymmetric only for the A-100V and A-130V arrays. The cycling resistance at 0 V (Rcycles,0V) is thus lower than that in the initial measurement by about ten and two times in case of sample A-70V and samples A100V and A-130V respectively

The electrical characterization of the arrays A therefore does not reveal any resistive switching behavior, for which a substantial decrease of resistance after the initial I(V) cycle accompanied by a presence of high- and low-resistance states (HRS and LRS, respectively) in the following cycles is expected. [57.] The observed current jumps and drops in the initial I(V) curves of arrays A (Figure 3.34. a.) are rather caused by imperfect contacting, and there are no signs of distinguishable HRS and LRS in the following cycles. On the other hand, the resistance increases with the re-anodizing potential, which is in line with the increasing length of the nanocolumns and with their semiconductive nature. In addition, as samples A-100V and A-130V have their initial and consecutive I(V)'s similar to each other but different from those of sample A-70V (see the curve shape and symmetry), different conduction mechanisms are expected in these array groups. The oxygen-deficient root structure [79.] of A-70V columns in the PAA barrier may prevail in the shorter nanocolumns, whereas a more stoichiometric, i.e. less conducting column body situated over the roots may lead to the diode-like behavior of A-100V and A-130V arrays, possibly with a Schottky barrier created at the Au/TiO_2 interface. [57.] To alter the electrical behavior of the PAA-assisted TiO_2 nanocolumns, an array of type B (i.e. having the lower potential sweep rate during re-anodizing) was also prepared and electrically characterized. An initial I(V) curve of sample B-100V (Figure 3.34. c.) shows a non-linear asymmetric behavior with $R_{initial,0V}$ of ~6·10^5

Ω·cm^2 and a current jump at 5.0 V, leading to a drop in the resistance of about one order of magnitude. The consecutive cycling (Figure 3.34. d.) reveals also a non-linear asymmetric I(V) characteristic and, in addition, the presence of HRS and LRS having $R_{cycles,0V}$ of ~3·10^4 and ~8·10^3 Ω·cm^2, respectively. The array B-100V shows therefore signs of bipolar resistive switching. During the initial, forming I(V) cycle, a conducting filament is probably formed within the columns or at one of the interfaces. [57.]

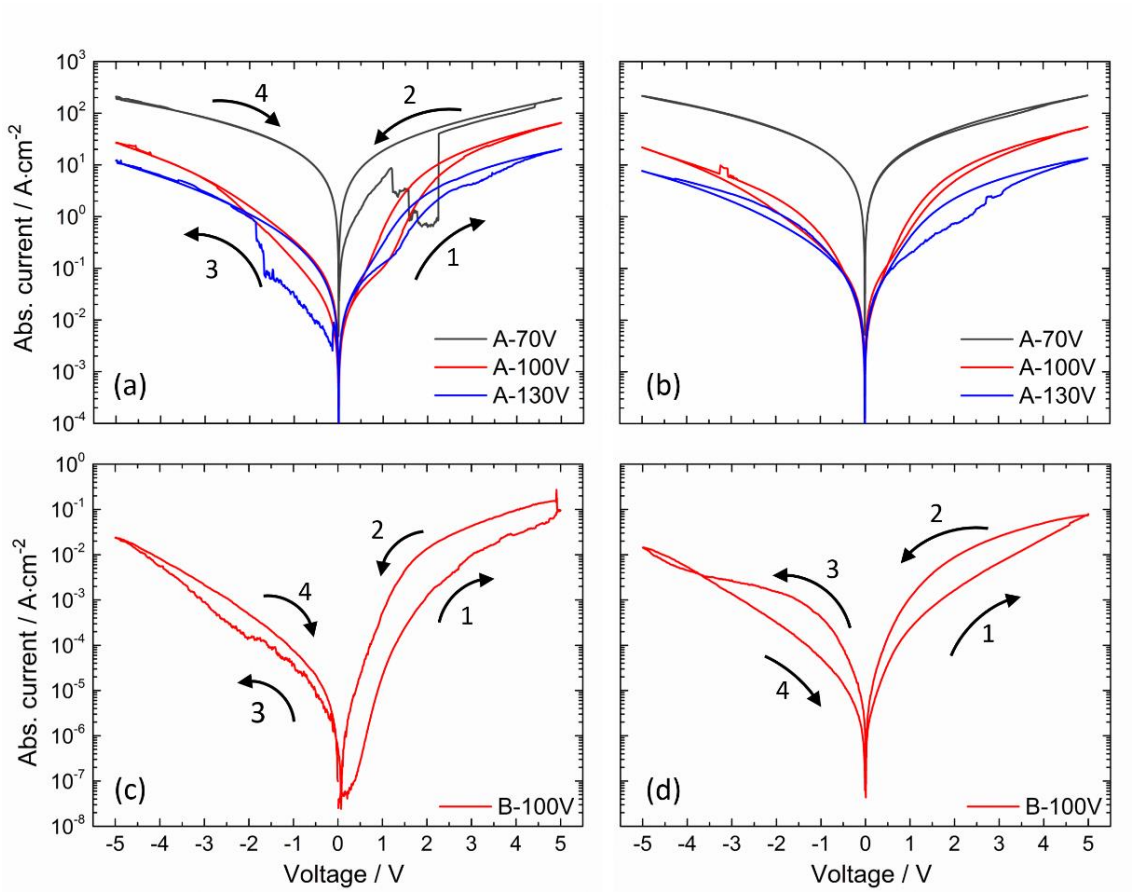


Figure 3.34.:(a, c) The initial and (b,d) further *I*(*V*) cycles obtained (a, b) for arrays A (i.e. formed at the higher potential sweep rate during re-anodizing) and (c, d) for arrays B (i.e. formed at the lower potential sweep rate during re-anodizing). The cycling was performed in the order 0 → +5.0 → −5.0 → 0 V without any break in applying voltage, at a scan rate of 100 mV·s^{-1} at room temperature. The top Au electrode was biased while the bottom Ti layer was grounded. The arrows indicate the scan direction

The switching direction, i.e. the transformation of HRS into LRS, happening at the positive polarization of the top Au electrode, followed by a transition from LRS into HRS at the negative polarization, indicates that the switching interface is the bottom one (TiO_2/Ti). [57.] The absence of abrupt current or resistance change during one of these transitions may indicate synaptic behavior of the array, [59.] executed in this case by inhomogeneous switching events in the multiple channels present in the array. Comparing the anodizing conditions during the nanocolumn growth with the electrical behavior of arrays A and B, we see the following relations, summarized schematically in Figure 3.35.. The higher potential sweep rate during the re-anodizing (arrays A) leads to the formation of nanocolumns having

a relatively low initial resistance (between 0.25 and 8 Ω·cm^2), whereas the lower potential sweep rate (array B) seems to increase the resistance (6·10^5 Ω·cm2). This may be explained by a formation of more oxygen-deficient and thus more electrically conducting nanocolumns in the case of the faster sweep rate during the column formation (arrays A) as compared to more stoichiometric oxide formed during the slower sweep rate (arrays B). [60.] Such higher-resistance, more-stoichiometric TiO_2 nanocolumns would be expected to lead to bipolar resistive switching behavior, [6.] as it is indeed observed in the present study. In addition, the length of the nanocolumns seems to have also an influence on their electrical resistance, possibly due to an inhomogeneous distribution of oxygen vacancies along the nanocolumn material, as manifested in arrays A by the increase in the resistance with increasing nanocolumn length, accompanied by the diode-like I(V) characteristics of the longer A-100V and A-130V nanocolumns. To confirm this mechanism, as well as to elucidate the role of the annealing in vacuum on the concentration and distribution of oxygen vacancies, further analytical and electrical characterization of the arrays is being performed. Additionally, TiO_2 nanocolumn arrays grown at modified electrochemical conditions are currently under investigation; the results to be reported in due course.

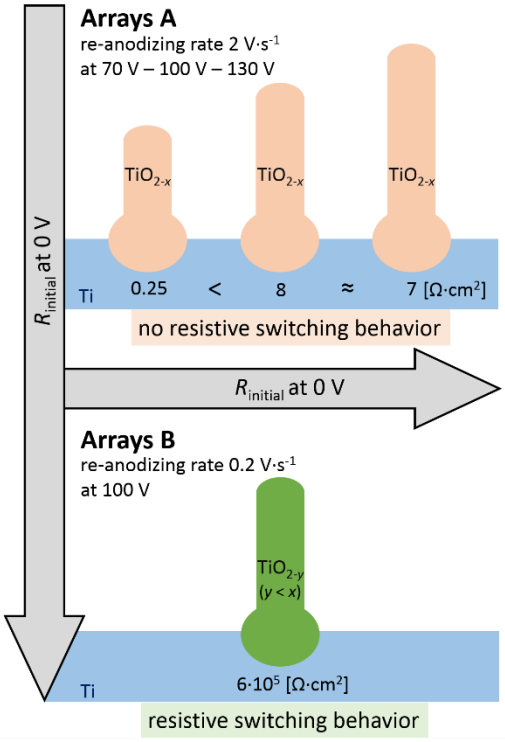


Figure 3.35.: Schematic representations of PAA-assisted-anodized TiO_2 nanocolumns re-anodized to different potentials showing the relations between the anodizing conditions, oxide stoichiometry, and electrical properties. The faster re-anodizing rate (arrays A, upper part) results in a lower $R_{initial,0V}$ and reveals no sign of resistive switching, whereas the slower re-anodizing rate (arrays B, lower part) leads to the formation of more stoichiometric columns having a high $R_{initial,0V}$ and showing the resistive switching.

End of the Quotation 1.

3.8.2 Electrical characterization of nanocolumns electrochemically grown at 40 V

Current-voltage curves for short nanocolumns anodized at 40V with electrodeposited gold top electrode and for long nanocolumns re-anodized at 100V with electrodeposited gold top electrode, above mentioned in the quotation as sample B-100V, were plotted. (Figure 3.36.) The values of the differential resistance were calculated, because the current and the voltage are not linearly proportional. The final resistance changes were presented as R_{dif} *(d V /d I)* – voltage curves.

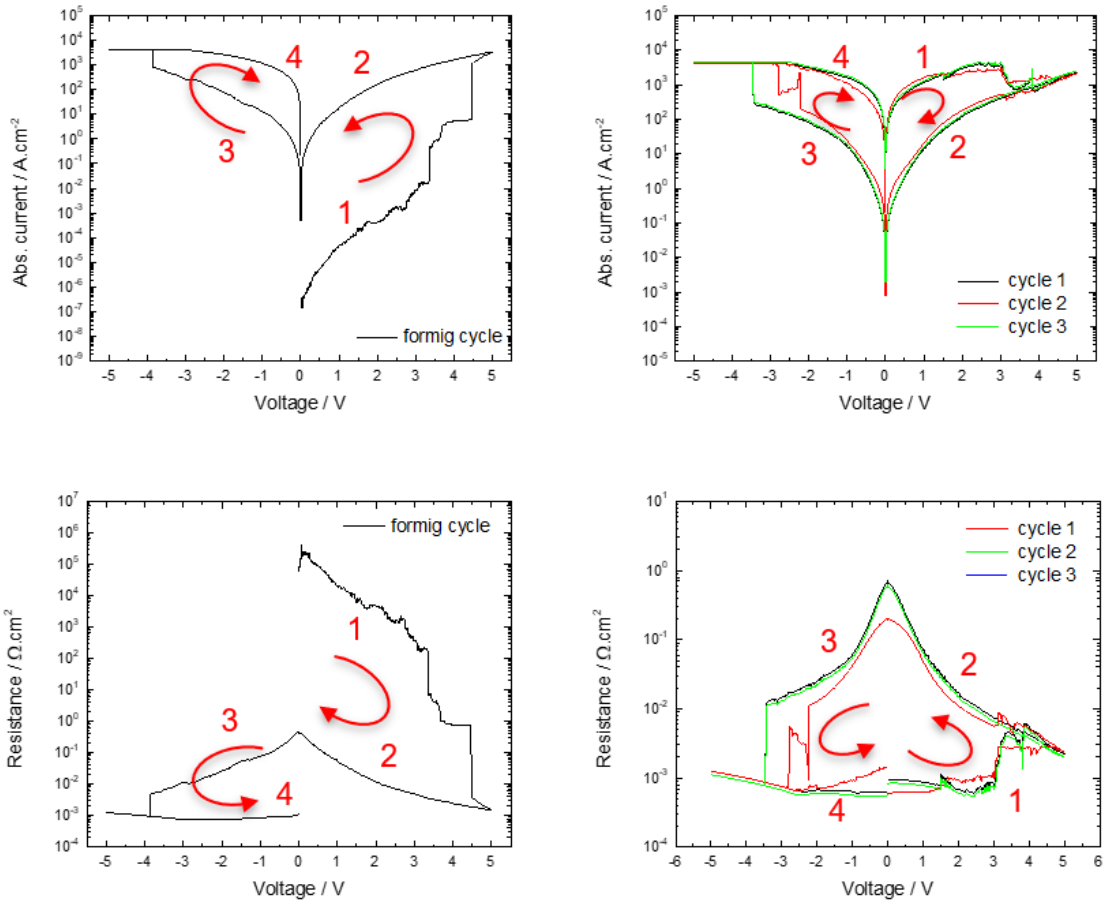


Figure 3.36.: Current - voltage and differential resistance - voltage curves from analyzed samples with columns anodized at 40V. The current and the resistance changes are marked and numbered for better understanding.

The initial I(V)curve similarly to the sample B-100V, quoted above, showing a non-linear asymmetric behavior with $R_{initial,0V}$ of ~$1{,}3 \cdot 10^5$ Ω·cm^2. The initial cycle can be considered as a forming cycle because a current jump at 4,5V leads to drop in the resistance of about two orders of magnitude. The resistance-voltage curves for short columns and for long columns (device B-100V) are presented and compared in Figure 3.37..

The consecutive cycling shows a non-linear and slightly asymmetric behavior, where at increased voltage at 3V a current drop increased resistivity from ~$1 \cdot 10^{-3}$ Ω·cm^2 to ~$8 \cdot 10^{-3}$ Ω·cm^2 and in-between -2,2V to -3,5V a current jump decreased resistivity approximately about one order of magnitude, form ~$1 \cdot 10^{-2}$ Ω·cm^2 to ~$1 \cdot 10^{-3}$ Ω·cm^2. The presence of HRS and LRS states during the cycling at 0V were observed with a resistance difference about two to three orders of magnitude. $R_{\_cycles,0V}$ were about ~$5 \cdot 10^{-1}$ Ω·cm^2 to ~$8 \cdot 10^{-4}$ Ω·cm^2.

The conductive filament during the initial cycle was formed. The transformation of LRS into HRS was observed at the positive polarization of the Au electrode and the transition from HRS to LRS at negative polarization. The switching interface probably is at the TiO_2/Au, nevertheless the realization process of the columns and the top electrode should be considered.

From previous material and structure evaluation the properties of the short nanocolumns were presented and the electrodeposition of the Au into the pores was written as well. Due to the small resistance values and the low potential at the current drops/jumps, the influence of the electrodeposition on the device is considered.

To avoid undesirable influences, the devices with re-anodized nanocolumns at 100V were prepared with sputtered Au top contacts in as anodized, air annealed and vacuum annealed conditions.

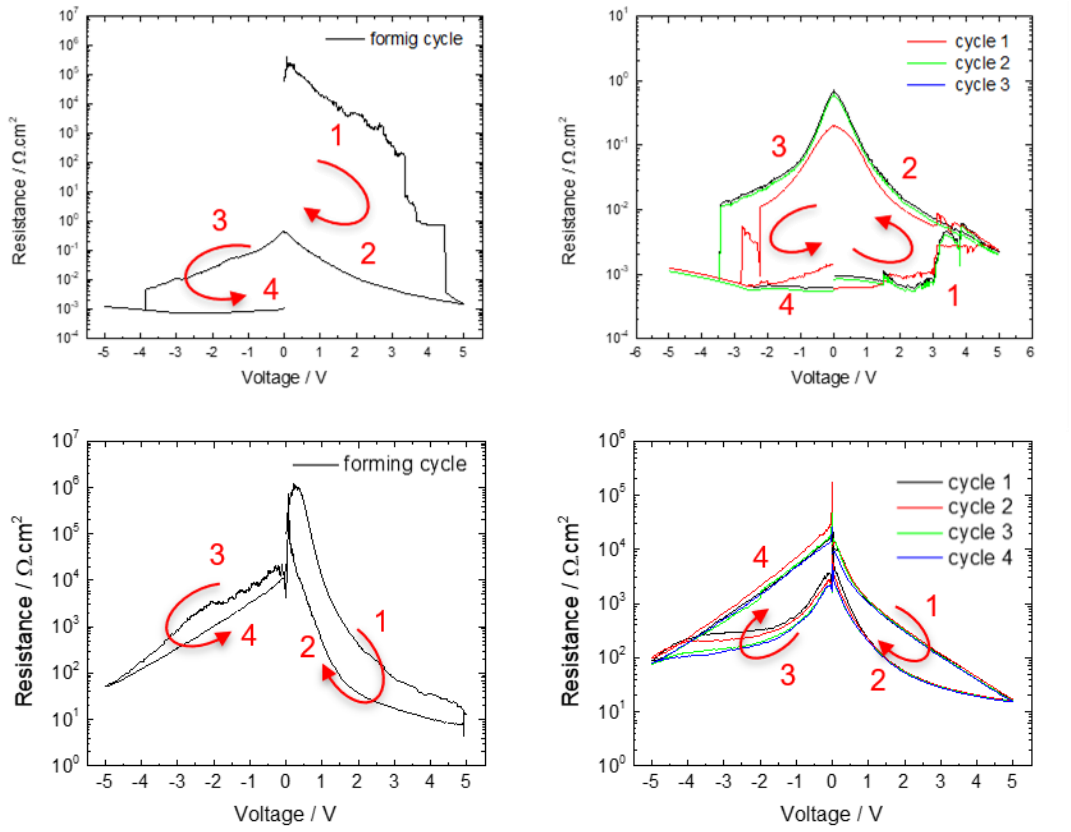


Figure 3.37.: LRS and HRS transition at devices with short and long nanocolumns. The switching direction is different, which suggests the switching interface is the TiO_2/Au for the short columns (a.) and Ti/TiO_2 is used at long columns. (b.)

3.8.3 Electrical properties of nanocolumns differently annealed

This chapter is dealing with electrical characterization of long nanocolumns, re-anodized at 100V into a thin AAO. The top of the columns reached the AAO surface, therefor the top Au contact was magnetron sputtered and shaped by lithography and wet etching respectively.

To ensure identic nanocolumns for all annealing set up, one anodized device was divided into four pieces. First quarter was left without annealing – device: A*s-Anodized*, the second quarter was annealed in vacuum at 500°C for 2 hours – device: *Vac500*, and the third quarter was annealed in air at 500°C for 2 hours – device: *Air500*. The fourth quarter was saved as a reserve piece. The top gold layer was prepared by magnetron sputtering on all three devices in a same time.

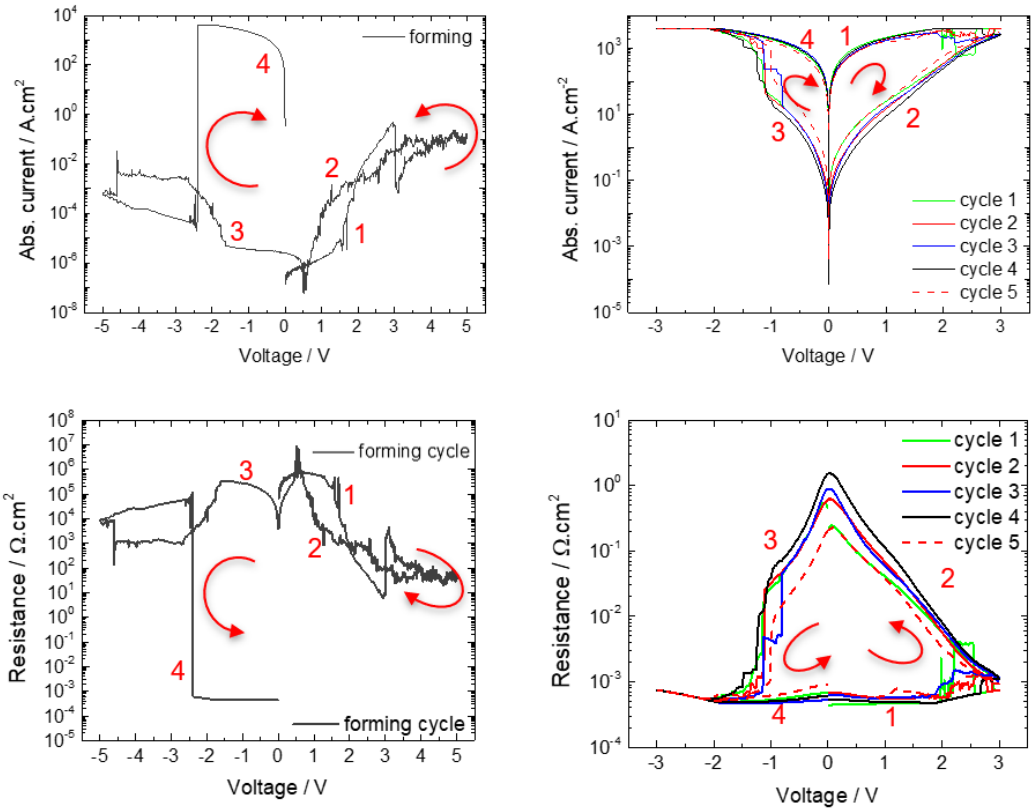


Figure 3.38.: LRS and HRS transition at AsAnodized device with long nanocolumns. The switching interface is probably the interface TiO_2/Au, similarly to the device with vacuum annealed short nanocolumns and electrodeposited top contact.

The initial I(V) curves were measured at room temperature (Rt) for all devices. As-anodized device was characterized at initial cycle ±5V, for the Vac500 and the Air500 ±10V was applied respectively. As-anodized sample shown interesting behavior at positively polarized top electrode, where increasing current from 1,7V to 3V was observed with a steep rising character from 1,7V to 2V and with linear rise from 2V to 3V, where a current drop about two orders of magnitude appeared. The current jump at negatively polarized Au electrode about 8 orders of magnitude at -2,5V reached current compliance level and the

high current was held between -2,5V to -1,7V, then the current decreased significantly. The same initial cycle set up was repeated on several As-anodized devices and similar current jump up to the current compliance level was observed between potentials about -2V to -4V.

The consecutive cycling potential range was set up for ±3 V, based on the potential levels of current drop/jump. (Figure 3.38 .) The device shown during the cycling nonlinear behavior, with a resistance difference at positively polarized top electrode about three orders of magnitude, $R_{\_cycles,0V}$ were about ~$7 \cdot 10^{-4}$ Ω·cm^2 to ~$6 \cdot 10^{-1}$ Ω·cm^2. At negatively polarized top electrode a current jump, about three orders of magnitude, was observed between -1,2 V to -1,5 V, that leads to RESET the device form HRS to LRS. Due to the transformation from LRS to HRS at positively polarized Au electrode, the switching interface is probably at the TiO_2/Au.

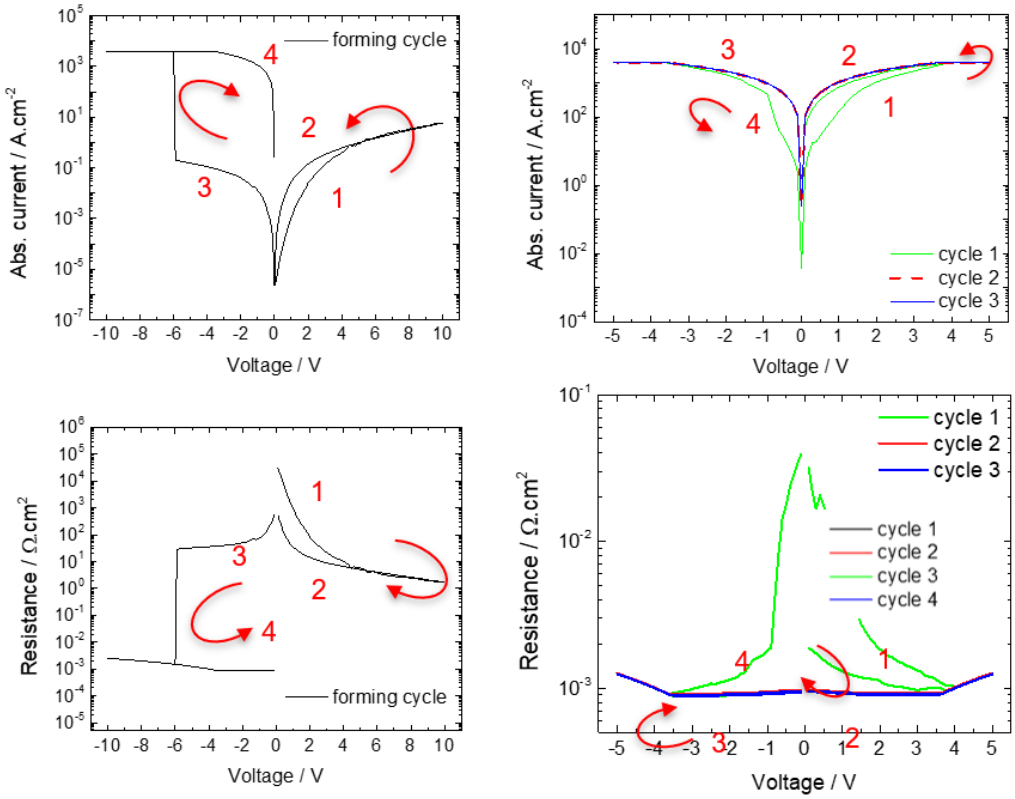


Figure 3.39.: Electrical characterization of vacuum annealed device. The forming cycle with current direction is comparable with AsAnodized sample. The consecutive cycling from the 2nd cycle shown symmetric diode like character, without HRS and LRS switching tendency.

Device Vac500 was characterized at three different cycling potentials, at ±5V, ±10V, ±20V. Attempts to find a proper potential range for formation of the device were unsuccessful at ±5V and at ±20V as well. The initial cycle at ±5V shown a diode like behavior at positive and negative top contact polarization. The device at potential range ±20V shown a diode like behavior at positively polarized top contact, however at negative polarization a current jump at -6 V was observed. The current jump about four orders of magnitude

reached the current compliance level and the device did not shown any switching behavior at consecutive cycling. Similar results were achieved at ±10V cycling set up, where at -6V at negatively polarized top contact a current jump about four orders of magnitude reached the current compliance level. Due to above mentioned results from initial cycling at different ranges a consecutive cycle range was declared as ±5V. The device shown symmetric diode like behavior from the 2nd cycle at positive and negative polarization of the Au contact. At cycle 1 a small difference about one order of magnitude, $R_{\_cycle1\_0V}$ were about ~$1 \cdot 10^{-2}$ Ω·cm^2 to ~$2{,}8 \cdot 10^{-1}$ Ω·cm^2.

The symmetric diode like character of the device is probably caused by a Schottky barrier on TiO_2/Au interface at positively polarized Au. The Ti/TiO_2 interface behaves as an ohmic contact in this case. Calculating of Schottky barrier height, if there is any Schottky contact available on Ti/TiO_2 interface, can help to understand electrical behavior of this device.

Air annealed device was characterized at potential ranges ±5V, ±10V and ±20V. The current compliance level was reached from 19,6V to 20V and then the device shown only non-linear diode like character for both polarizations of the top electrode. The initial I(V) curve after cycling at potential ±10V shown asymmetric non-linear character with a steep current rise from $I_{\_initial\_7,6V}$ = ~$6{,}5 \cdot 10^{-5}$ A·cm^{-2} to $I_{\_initial\_8,3V}$ = ~$4{,}3 \cdot 10^{-4}$ A·cm^{-2} and then with a moderately steep rising a current level $I_{\_initial\_10V}$ = ~$5 \cdot 10^{-3}$ A·cm^{-2} was observed. With decreasing potential, a steep current rising was observed from 0,5 V to 0 V. Similar current behavior was observed at negatively polarized top electrode from potential -3,1 V to 0 V, where the current level increased about one order of magnitude. (Figure 3.40.)

The consecutive cycling shown current level difference at positively polarized top contact at 9V about 2 orders of magnitude. The current decreased in almost linear way between potential 8 V to 1 V. From 1 V to 0 V the current drop and jump was observed, and similar current behavior appeared at negatively polarized gold contact between ranges -5,5 V to -4,5 V and -2 to -1 V.

If the above-mentioned current behavior at the positive and at the negative Au polarization is appearing, probably a capacitive coupled diode like behavior was measured, [68.] Moreover, the non-zero crossing current voltage behavior also proofs the presence of the capacitive state in the device.

The presence of HRS and LRS states during the cycling was not observed, however at 0V a resistance $R_{\_cycles,0V}$ about ~$4{,}3 \cdot 10^{-5}$ Ω·cm^2 to ~$9{,}6 \cdot 10^{-5}$ Ω·cm^2 was measured.

The electrical behavior of the Air500 device can be caused by more stoichiometric TiO_2 and the oxygen distribution through the roots and the column. Furthermore, the device behaves as a linear resistor between 8V to 1 V, where the current decreased in a linear way.

The electrical characteristic of the device Air500 at positively polarized top contact suggests the existence of a Schottky interface barrier at the TiO_2/Au.

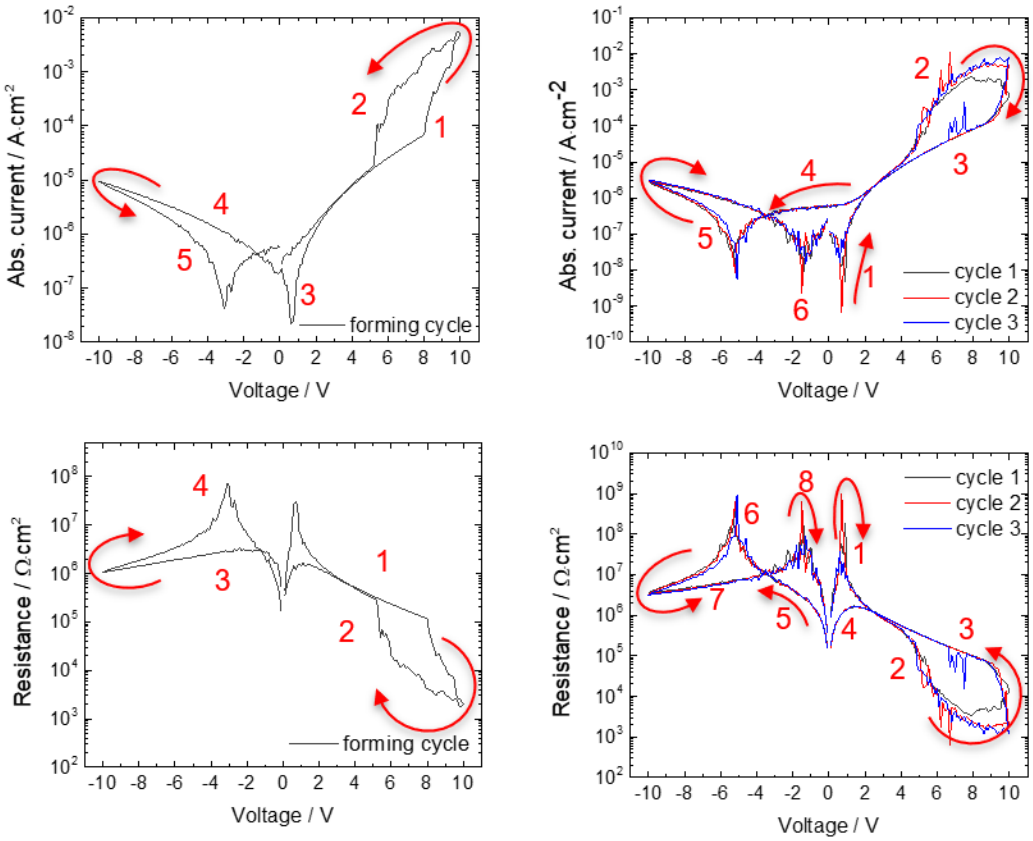


Figure 3.40.: Electrical characteriyation of air annealed device Air500. The current behavior during the cycling is suggest to a capacitive coupled diode behavior.

The measured I(V) characteristics were compared with characteristics from other *transient metal/transient metal oxide/noble metal* devices [57.][80.] where similar non/linear characters were observed. The asymmetric current voltage behaviors are probably caused by a formation of a rectifying Schottky junction on oxide/metal interfaces in case of as-anodized devices and air annealed devices respectively.

At positive polarization of the top electrode (Au) the only limiting electron transport feature is the Schottky-like barrier formed at TiO_2 interface. The Ti/TiO_2 interface is considered as an ohmic contact. This is consistent with the work function and electron affinities of the materials involved (for Au: 5,4 eV [61.], for Ti: ~4,1-4,3 eV [61.] and for TiO_2: ~4,4-5 eV [61.]).

In the nanocolumns the concentration of the oxygen vacancies are acting as electron donors, which concentration at the top of the columns is depending on the annealing set up or the Schottky barrier is higher due to the thicker depletion layer at the TiO_2/Au interface. This phenomenon was observed at other anodized transition metals as well. [57.] The ohmic or non-rectifying contact at the Ti/TiO_2 interface was written by *Michalas et. al.*.

Asymmetric I(V) characteristics are typical for interface-controlled transport, which can be dominated by a thermionic emission or by tunneling through the formed barrier at the interface. These two types of transport are easily distinguishable via temperature dependence of the I(V) characteristics furthermore for interface-controlled transport the most common thermally activated mechanism is the thermionic emission. [81.]

Temperature dependent I(V) curves were plotted as logI vs. logV and logI vs. $V^{1/2}$ for positively and negatively polarized top electrode (Figure 3.41., Figure 3.42.). The saturation current I_0 was evaluated from semi-logarithmic plots of the temperature dependent I(V) curves. These above written curves were obligatory to calculate Schottky barrier height.

The current in reverse direction can be calculated by equation

$$I_R = A^* \times T^2 \times e^{\frac{-q\left(\Phi_B - \sqrt{\frac{q}{4\varepsilon\pi d}} \times \sqrt{V_R}\right)}{kT}}, \qquad (21)$$

where I_R is the reverse current density, A* is the effective Richardson constant, Φ_B is the Schottky barrier height, ε is the permittivity of TiO_2, and d is the depletion layer. Based on this equation the *log*I ($V^{1/2}$) plots have linear dependence in ideal case. [57.][61.][62.]

For As-Anodized device the plots hardly can be called as a linear, however the current density is in a range of one order of magnitude for all temperatures. Based on this behavior the temperature dependency at As-Anodized sample is questionable at low potential.

Vac500 device shown linear tendency in reverse direction in plots *log*I ($V^{1/2}$), with increasing current density at higher temperatures. However, two ranges were observed, from Rt to 140°C and from 180°C to 230°C, where the current density of the curves in range from 180°C to 230°C were lower than at 65°C.

Air500 device shown linear tendency in reverse direction in plots *log*I ($V^{1/2}$), with increasing current density at higher temperatures.

The equation (21) rewritten into form:

$$ln\frac{I_R}{T^2} = lnA^* - \frac{1}{T} \times \frac{q}{k}\left(\Phi_B - \sqrt{\frac{q}{4\varepsilon\pi d}} \times \sqrt{V_R}\right), \qquad (22)$$

With plotted Richardson plots *lnI/T²(1/T)* for all three devices and with method from Bendova et al. the constant value of *lnA** independent on the reverse potential is defined, the values of the Schottky barrier height Φ_B and the depletion layer depth *d* was calculated respectively.[57.]

The currents in forward direction can be written as

$$ln\frac{I_F}{T^2} = lnA^* - \frac{1}{T} \times \frac{q}{k}\left(\Phi_B - V_F\right), \qquad (23)$$

and they were plotted as Richardson plots, *lnI/T²(1/T)* for all three devices. ([57.] and with above used method the value of *lnA**, the Schottky barrier height Φ_B and the depletion layer depth *d* was calculated. The results are summarized in Table 5. [57.][61.]

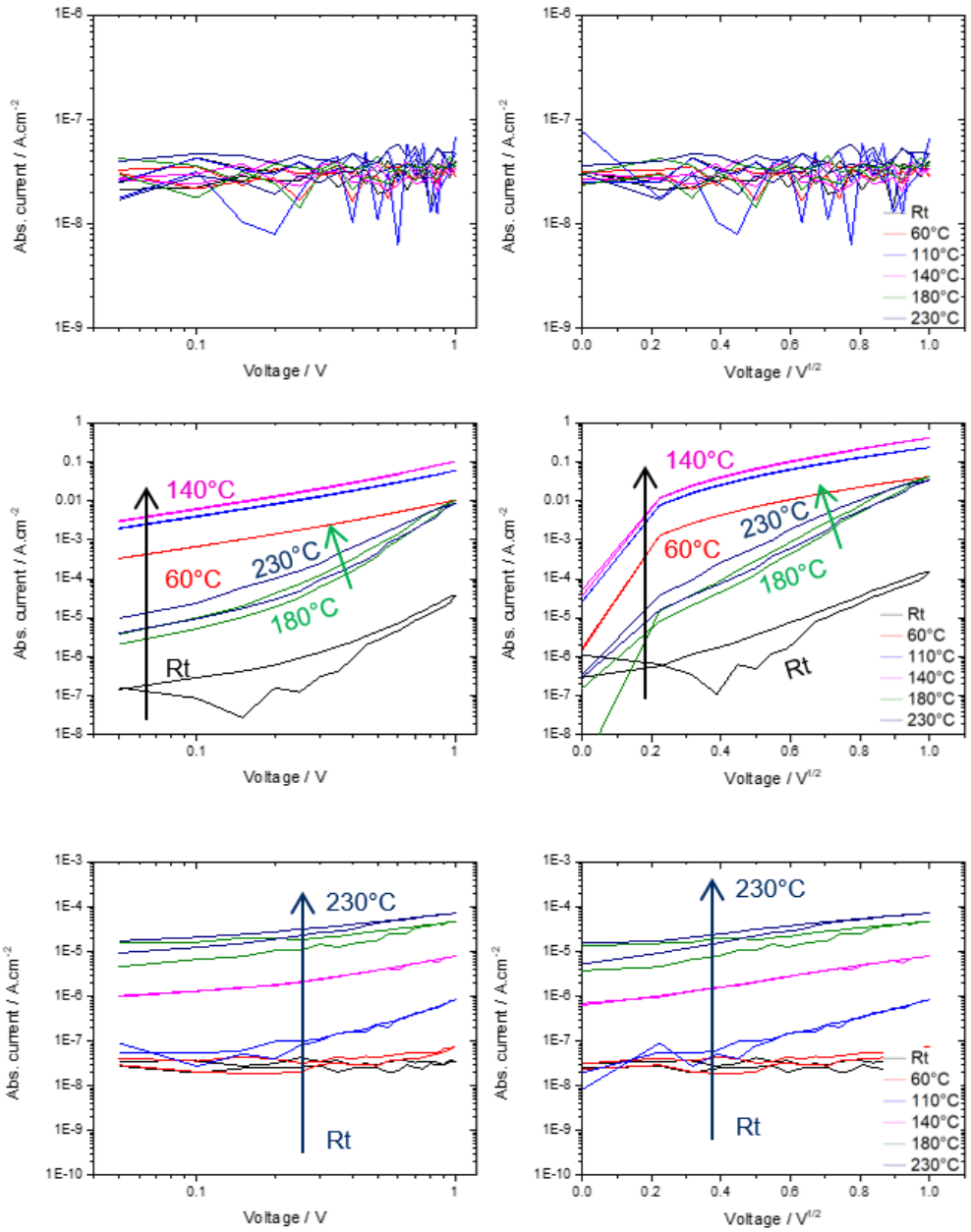


Figure 3.41.: Temperature dependent I(V) curves were plotted as logI vs. logV

and logI vs. $V^{1/2}$ for positively polarized top electrode

The Schottky barrier height Φ_B was calculated from the saturation current density I_0, which was earned by extrapolation of the current density at 0V red from the semi-logarithmic plots in forward direction, presented in Figure 3.43.

The Φ_B was calculated as

$$\Phi_B = \frac{kT}{q} ln \frac{A^* T^2}{I_0} \quad (24)$$

[57.][61.] and compared with values from previous calcualtions in Table 5.

The temperature dependent current voltage curves were plotted for positive and negatative polarization of Au electrode and the Schottky junction presence at the Ti/TiO_2

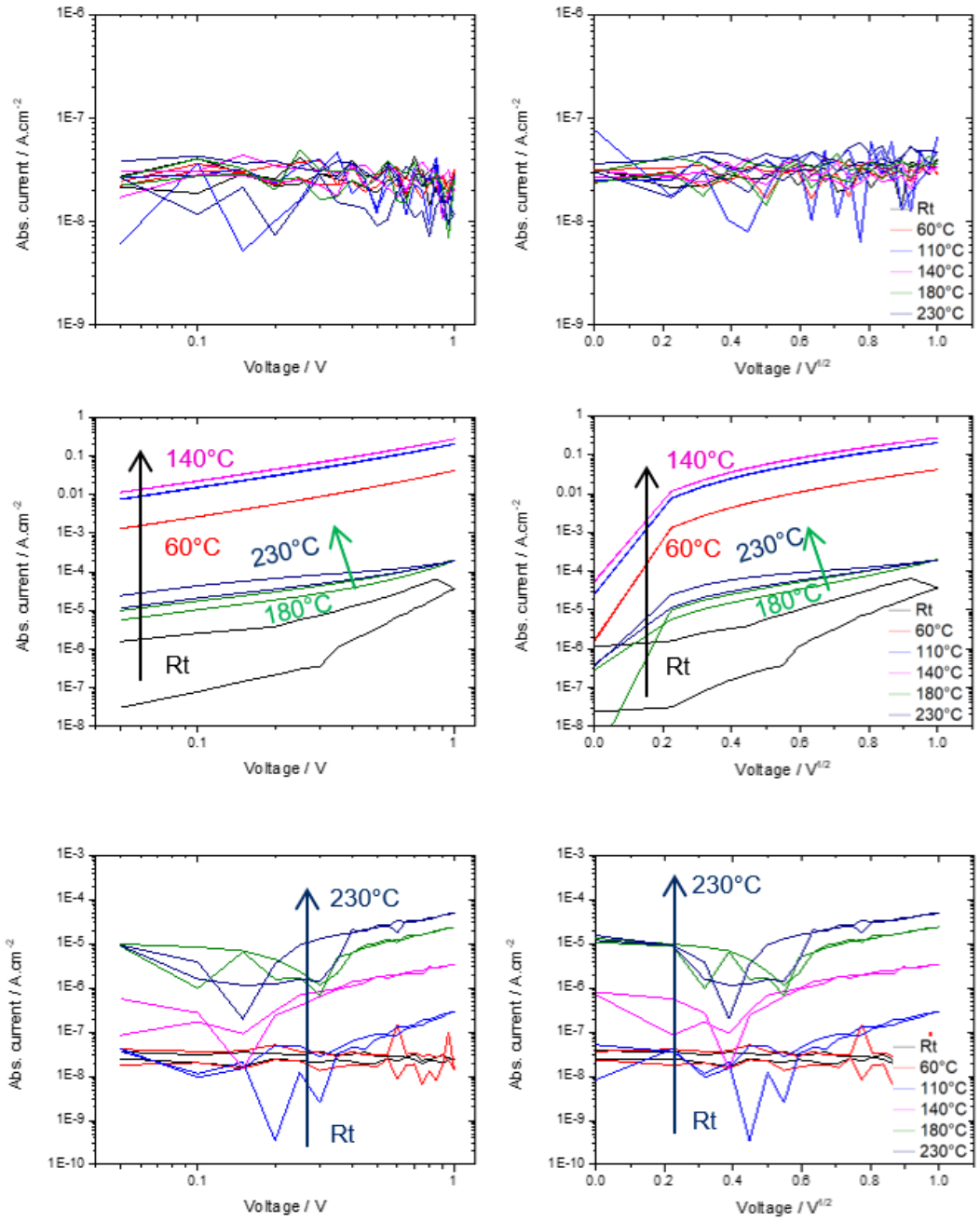


Figure 3.42.: Temperature dependent I(V) curves were plotted as logI vs. logV and logI vs. $V^{1/2}$ for positively and negatively polarized top electrode

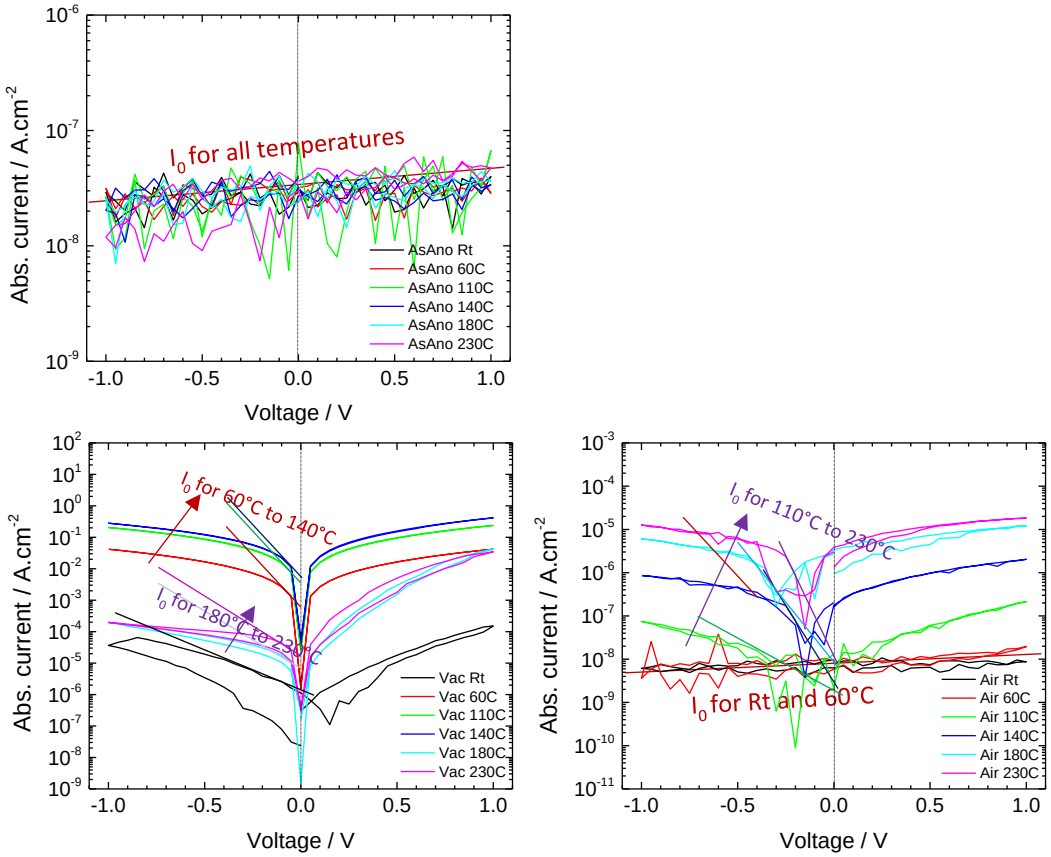


Figure 3.43.: Extrapolated current density in forward direction at as anodized, vacuum annealed and air annealed devices. The current density I_0 was red from the curves manually, therefore small inaccuracy in the results may appear.

Table 5.: Summarized Schottky barrier heights for as anodized, vakuum annealed and air annealed devices, respectively.

	Forward dierction (neg. top electrode)		**Reverse direction (pos. top electrode)**		**Forward direction I0 method**	**Reverse direction I0 method**
	ΦB [eV]	***d [nm]***	***ΦB [eV]***	***d [nm]***	***ΦB [eV]***	***ΦB [eV]***
As anodized	1,11	0,68	0,54	0,6	0,56	0,3
Vacuum annealed	-0,43	1,6	-4,91	3,3	-0,2	-0,32
Air annealed	-1,84	2,9	-4,72	2,4	-0,21	-0,4

Schottky barrier heights and depletion layer thicknesses summarized in Table 5. are corresponding with the first conclusions from the IV characterizations. The as-anodizded

device with a Schottky barrier height at BE and the nanocolumns are lower, than at the TE. The resistive switching at this device is real, the switching interface is between the oxide layer and the TE.

The vacuum annealed and the air annealed devices shown diode like behavior, which was confirmed by the calculations of the Schottky barrier height. The calculations were given negative values for Schottky barrier height at vacuum annealed and air annealed device, respectively. This rare phenomenon at the Ti/TiO_2 interface can be presented as an ohmic contact. Similar phenomenon at different material combinations was observed and published by [82.]

The calculations of Schottky barrier heights with I_0 method brought similar results as above written calculations. The device with as-anodized nancolumns shown Φ_B 0,56 eV (prev. calc. 1,11 eV) in forward direction and 0,3 eV (prev. calc. 0,54 eV) in reverse direction. The difference between the calculated SBH are negligible and they can be considered as realistic resuls.

The SBH for the vacuum annealed and air annealed devices are in negative range with both calculation methods. The tenfold difference between the values in reverse direction was probably caused by the differences between the calculation methods. The lower SBH with I_0 method can be closer to the reality.

4 CONCLUSION

Resistive switching in MOM devices is an actual topic with huge possibilities in many fields, as computer sciences, systems with artificial intelligence, analogue and digital electronics, etc.

In this work, the prepared nanostructures were analyzed from material and structural view with several high-tech techniques.

Fabrication of the highly self-ordered nanocolumn arrays in AAO template with different root structures, opened new possibilities and showed possible challenges from realization to characterization as well. The short nanocolumns with a void-full tooth like root structure are helped to understand their growing process, the differences between the voltage sweep rates on the root structures were also visible on the root structures.

Effect of the annealing properties were presented by three device groups - as anodized, vacuum annealed and air annealed devices, where the self-ordered AAO with the TiO_2 nanocolumns were prepared in identic way, only the annealing step was different. The nanocolumns remained amorphous in all three cases, however at the bottom of the roots under the Ti borderline a thin layer of nano-crystallites was detected.

The electrical characterization of the devices was provided on Keithley 4200 SMU, where a resistive switching behavior was detected at short (anodized at 40V) vacuum annealed device with electrochemically deposited gold TE and at as anodized device with magnetron sputtered gold TE, respectively. The device with short vacuum annealed columns had low endurance, therefore it was not included to the experiments dealing with the Schottky barrier height declaration.

The SBH at the Ti/TiO_2 interface was calculated with two methods for all three differently annealed devices. The as anodized device with resistive switching properties had SBH between 1,11 eV (forward direction) and 0,54 eV (reverse direction). The shigher SBH at interface TiO_2/Au and the switching direction from LRS to HRS suggests, the switching interface is between the column and the TE. The vacuum and air annealed devices shown only diode like behavior with negative SBH at the BE and column interface, what is considered as an ohmic contact.

The length of the nanocolumns requires higher potential (few volts) to show any resistive switching or diode like behavior, therefore their future area of use can be mainly in analogue techniques where a capacitive coupled diode circuits are required or at slower digital techniques where higher potentials (few Volts) can be used for writing and lower potentials for reading.

Table 6.: Overview about the results of the electrical characterization of three devices, differently annealed.

Anodizing potential	Sweep rate for re-anodization	Sweep rate for re-anodization	Annealing set up		
	0,2 $V \cdot s^{-1}$	2 $V \cdot s^{-1}$	As-Anodized	500°C/2h in Vacuum	500°C/2h in Air
40V	Resistive switching appeared: LRS to HRS difference is about 3 orders of magnitude. Switching interface: oxide/TE.	No sweep rate differencies at 40V.	Difficulties during gold sputtering into the AAO. The pores were too narrow and too long for magnetron sputtering.	Difficulties during gold sputtering into the AAO. The pores were too narrow and too long for magnetron sputtering.	Difficulties during gold sputtering into the AAO. The pores were too narrow and too long for magnetron sputtering.
40V re-anodized at 100V	Resistive switching appeared: LRS to HRS difference is about 3 orders of magnitude. Switching interface: oxide/TE. SBH was not calculated due to different TE deposition technique.	No RS behavior, only diode like behavior was measured. The resistance of the columns are increasing with the length.	Resistive switching appeared: LRS to HRS difference is about 3 orders of magnitude. Switching interface: oxide/TE. SBH at BE/oxide is about 1,11 to 0,54 eV.	No RS behavior, only diode like behavior was measured. The active interface is at the oxide/TE. The SBH at the BE/oxide is about -0,2 to -4,9 eV.	No RS behavior, only capacitive coupled diode like behavior was detected. The active interface is at the oxide/TE. The SBH at the BE/oxide is about -0,2 to -4,7 eV. The capacitive character is probably caused by the void zone in the BE.
40V re-anodized at 130V	Device damage during re-anodization.	No RS behavior, only diode like behavior was measured. The resistance of the columns are increasing with the length.	Device damage during re-anodization.	Device damage during re-anodization.	Device damage during re-anodization.

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LIST OF ACRONYMS

AAO	Anodic alumina oxide
BE	Bottom electrode
BTF	Barrier type film (barrier type anodic alumina)
CF	Conductive filament
EDX	Energy dispersive X-ray spectroscopy
EELS	Electron energy loss spectroscopy
HRS	High resistance state
HR-TEM	High resolution transmission electron microscope
LRS	Low resistance state
MIM	Metal Insulator Metal device
MOM	Metal Oxide Metal device
MSM	Metal Semiconductor Metal device
NVM	Non-volatile memory
PAA	Porous anodic alumina
PVD	Physical vapor deposition
RS	Resistive switching
SBH	Schottky Barrier Height
SEM	Scanning electron microscopy
STEM	Scanning transmission electron microscopy
TEM	Transmission electron microscopy

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