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SIGNAL INTEGRITY OPTIMIZATION TECHNIQUES FOR HIGH-SPEED CHIPS SIGNALING
METODY OPTIMALIZACE PRO ZAJIŠTĚNÍ INTEGRITY SIGNÁLŮ PRO VYSOKORYCHLOSTNÍ PŘENOS DAT MEZI ČIPY

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TEZE DISERTAČNÍ PRÁCE

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KLÍČOVÁ SLOVA

Vysokorychlostní komunikace, komunikace mezi čipy, přenosové vedení, ekvalizace, preemfáze, metody tvarování pulsů, integrita signálu, pulsně šířková modulace, diagram oka, přenosový kanál, digitální signál, Nyquistův kmitočet, diskontinuita signálu, signálový jitter.

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1 INTRODUCTION

Today's high-speed multi-core microprocessors and memory interfaces require ever-increasing interconnect bandwidth for modern applications such as computing and graphic systems, networking and other high-speed systems. Stringent requirements for reduced board space, miniature connectors, efficient printed circuit board (PCB) design and low susceptibility to noise are associated with serial communications links architecture. Many existing serial I/O standards operate at multi-Gbps speeds such as well known PCI Express (PCIe). Next generation of the standard PCIe Gen 3 is able to operate at 8 Gbps in a single lane. As data rates are increasing, their susceptibility to damage is more critical. It is caused by the nonideal aspects of transmission lines, such as crosstalks and losses as well as energy dissipation caused by reflections and radiation. All these issues can cause significant problems in signal integrity and timing. These impacts dominate at multi-Gb/s speeds where the unwanted signal distortion can cause that signal energy is spread over multiple bit positions, a phenomenon known as intersymbol interference (ISI) [1]. This leads to increase in the jitter that degrades the timing margin as well as a distortion in the signal levels is the main cause of voltage margin degradation of the inter-chip signaling link [3]. In such severe environments, sophisticated pulse-shaping techniques such as equalization or pre-emphasis (equalization at the transmitter is often called transmitter pre-emphasis to reflect the effect of the filter operation), need to be employed to increase the data rates [4]. Equalization is a circuit technique that reduces the ISI-induced timing jitter and voltage margin loss by compensating for nonideal aspects, in particular the loss of interconnects at high speed [5]. For instance, the significant frequency-dependent losses of transmission lines which can cause system degradation are effectively overcome by using pre-emphasis or equalization techniques, the maximum signaling rate is significantly extended [6], [7], [8].

The transmitter equalization filter is commonly realized as finite impulse response (FIR) filters [9], [10], [11]. Various types of equalizers are also commercially available [12], [13]. The purpose of this operation is to increase (decrease for de-emphasis [14]) amplitude for the first bit after a logic transition relative to successive bits. However, the conventional FIR pre-emphasis techniques for recent CMOS technology trends are mainly restricted by its supply voltage, which will decrease according to CMOS scaling [2]. A time-domain pre-emphasis method does not change the pulse amplitude as for conventional FIR pre-emphasis, but a timing resolution is used to signal pre-distortion [15], [16]. This method is able to better adapt to current requirements in CMOS technology trends where higher switching speeds and lower supply voltage dominate. Actual research is primarily focused on the analysis and development of effective transmitter pre-distortion method for PCB channels where ISI and crosstalk noise are dominant factors of losses. In the dissertation thesis a modified signaling scheme to minimize these factors is proposed. Current time-domain pre-distortion methods use conventional rectangular pulse. This causes that many undesirable harmonic high frequency components are contained in a pre-distorted signal at the transmitter output. Such a system is very susceptible to crosstalk noise.

2 STATE OF THE ART

In this chapter the state of the art in the field of equalization techniques developed for high speed interconnect inter-chip signalization is presented. Thus, the conventional equalization techniques available in the literature are presented..

2.1 TRANSMITTER EQUALIZATION

Finite impulse response (FIR) filter (discrete linear equalizer) is usually implemented at the transmitter side. The most common implementation involves the use of high-speed digital-to-analog converter (DAC). Such a FIR-DAC filter has a digital input and an analog output. In [1], the basic architecture of typical FIR filter is shown. The structure of FIR filter includes delay elements known as stages of a shift register. In this case, a flip-flop is used to delay the signal with one bit time, input samples passes through these delay elements and are multiplied by the filter tap coefficients. The tap outputs are summed to form the output [1], [16]. In this case, the filter can be seen as de-emphasis circuit because the maximum voltage amplitude is achieved for bit stream with the most high-frequency content when there are rapid transitions in the bit stream, either from '0' to '1' or vice versa. When continuous bits of the same value are transmitted the output is attenuated because low-frequency content is just contained in portions of the signal. It corresponds better with leading-edge digital silicon manufacturing processes where the maximum voltage swing continues to decrease significantly below 1V [1].

Methods described in the literature for equalization of various transmission channels such as coaxial cables, twisted pair cables and PCBs where the FIR-DAC implementation described above is used are given in [9], [10], [32], [33], [34], [35], [36]. The simplest implementation is achieved by using the 2-tap symbol-spaced FIR (SSF) filters. However, in this case loss compensation does not exceed 18 dB, e.g. [32] at 4 Gb/s (2PAM), 10 dB loss compensation and in [37] at 5 Gbps (2PAM) 18 dB loss compensation is achieved. More complex implementation in [9] where a 5-tap symbol-spaced equalizer is described can achieve 30 dB channel loss compensation at the Nyquist frequency, at 3.125 Gb/s (2PAM). In this case 5 manually tuned FIR taps are used.

From the literature introduced above it can be concluded that the simplest implementation of FIR filters with only 2-tap coefficients cannot provide more than ~20 dB of loss compensation. Further increase in loss compensation can be realized only by using more complex circuits where it is necessary to take into account more parameters that need to be tuned to match the equalizer to the channel [16].

Pulse-width modulated pre-emphasis (PWM) technique was successfully implemented and summarized in [16]. This paper describes time-domain based pre-emphasis method where pulse-width modulated scheme is used to the sophisticated pre-distortion of the input data signal. The PWM filter achieves 30 dB loss compensation to equalization of 25 m long coaxial cable. For PCB interconnect performance only FR4 backplane with simple very long single-ended trace (270 cm) is tested. However, 24 dB loss compensation is demonstrated. These values of loss compensation can be achieved with conventional pre-distortion FIR methods if more complex (multitap) filters are used. In the next chapter, the conventional PWM method is compared with proposed modified PWM-RC method which uses raised cosine (RC) signaling scheme. This provides more options to customize the filter to the transmission channel with the advantage of crosstalk reduction.

2.2 RECIEVER EQUALIZATION

Receiver equalization is often used together with transmitter pre-distortion because the information obtained at the channel output can be simply used to filter coefficients adaptation for the receiver filter as well as for transmitter filter to improve the effect of equalization. In this case, an adaptive equalization by using feedback loop can be created. The benefit of adaptive equalization is to adjust the current pre-emphasis or equalization level with respect to interconnect lengths or increase/decrease in data rates. On the other hand, additional complexity to the design and more power consumption are required. The receiver equalizers can be categorized into two main groups as continuous-time equalizers and discrete-time equalizers.

A continuous-time equalizer is based on the use of simple analog components to achieve the desired high-pass filter function. The simplest implementation is possible by using RC equalizer where the main sections of the equalizer are the termination, high-pass filter and dc power-limiting filter [1]. These types of equalizers are also designed with active components to perform the desired signal gain. More complex circuit modifications are possible by using higher-order high-pass filters. Two types of practical implementation as second-order active equalizers and equalizers using RC-degenerated stages are further discussed.

In [9] the receiver includes a second order derivative analog equalizer and implementation of multitap filter at the transmitter side is performed. The proposed equalization system is able to 30 dB loss compensation at 3.125 Gbps. The receiver equalizer consists of three paths, DC, first-order derivative and second-order derivative [9]. The proposed concept includes several stages of variable gain amplifiers on each path. Thus, the circuit complexity and latencies through the three paths are significantly increasing. In [38] a high-speed CMOS adaptive cable equalizer is described. The filter has two separate paths for low-frequency and high-frequency signals. The tunable source degeneration capacitors are used to control the high-frequency boosting. The additional degeneration resistor is more complex circuit solution used to adapt low-frequency gain. Both elements are included in the impedance Z_2 which represents a larger impedance network. The impedance Z_1 is used as load resistor. By cascading multiple stages of such RC-degenerated differential pairs, in [38] 30 dB channel loss compensation was achieved in 0.18μm CMOS, at a speed of 3 Gbps [16]. In this case five stages were used. Each stage has a Z_2 impedance that can be switched and this allows you to precisely adjust the equalizer gain to the channel transfer function. In this case high channel loss compensation is achieved at the receiver side but both described implementations use more complex circuit solution.

A discrete-time receive-side equalizer architecture is the decision feedback equalizer (DFE). The concept is illustrated in [1]. In a DFE, decisions of previously detected symbols are used to remove ISI in the current symbol. The advantage of this technique is that DFE does not boost noise or crosstalk to achieve signal equalization as in the case of transmitter pre-emphasis. In situations when the transmitter pre-distortion circuit is used it is necessary to take into account an additional high-frequency noise in the signal. By using DFE equalization technique, the high-frequency noise induced in the signal can be effectively reduced. Especially for real PCBs channels of high-speed communication systems where the crosstalk at higher frequencies is dominated degradation factor, it can be an effective solution to improve the signal quality at the system output [34], [36].

However, the main limitations of the DFE technique are sensitivities to error propagation because for proper functionality it is necessary to assume that the past symbol decisions are correct [1]. Incorrect value decision affects future decisions due to the feedback based decisions. In [34] it is shown that for practical implementations a 4-tap DFE can be used. A further limitation is that the DFE architecture is able only to compensate post-cursors ISI. Furthermore, at very high bit rates it can be a problem in a sufficiently feedback loop response for the first post cursor tap. Loop unrolling techniques can be used to mitigate this [36], [16], [1].

2.3 DISSERTATION OBJECTIVES

Signal integrity, thanks to continuous development and improvement in the field of high-speed digital design, has become a critical issue. Thus, the timing and the quality of signal to ensure reliable high-speed data transmission is still current theme. There is a still area for improvement of conventional signaling techniques to overcome transmission channel with higher order transfer function with respect to current requirements for low power chip signaling. The main goals of dissertation can be divided to the four parts.

- Modeling of the real signal integrity phenomena by using own designed computational models using the latest information in the field of high-speed digital design.
- Detailed analysis of the time-domain equalization techniques and research of the new approaches to optimize signal emphasizing for better adjustability to the transmission channels with higher order transfer function.
- Extend of conventional time-domain equalization technique to the second order realization, practical implementations and the study of performance of proposed technique during equalization of higher order transmission channels.
- Detailed analysis of the impact and influences of additional channel discontinuities on the proposed signaling method together with practical verification of achieved results during the development of advance signal integrity models.

3 TIME-DOMAIN PRE-DISTORTION TECHNIQUES

In this chapter, for the first time the PWM-RC (raised cosine) pre-distortion method is proposed to the equalization of high-speed PCBs channels. Innovative PWM method is proposed in [16] and is applied to the coaxial cable loss equalization and simple single PCB trace equalization. It provides an alternative to FIR pre-emphasis which is still commonly used in high-speed interconnect systems. The proposed time-domain pre-distortion method in [16] has the advantage for modern low-voltage CMOS devices where the maximum voltage swing is pushed markedly below 1.0 V and the implementation of the pre-distortion methods based on pulse amplitude shaping can be a problem. The first part of the chapter shows both FIR and PWM schemes, all presented simulations have been created in MathCAD and Agilent Advanced Design Studio (ADS). In the next section both conventional PWM pre-distortion methods and proposed PWM-RC are analytically compared. It is shown that PWM-RC method is able to better compensate higher-order transmission channel than conventional PWM scheme. The PWM pre-emphasis provides higher maximum loss compensation (24 dB) than the commonly used 2-tap SSF filter (18 dB), because its transfer function is able to adapt very well to the copper channel, see simulation results in Agilent ADS studio [42]. However, the crosstalk susceptibility of conventional PWM can cause additional high-frequency content in equalized data stream. Thus, the loss compensation can be significantly reduced. The proposed PWM-RC method reduces ISI, see section 3.2. Eye diagram analysis and additional high-frequency noise are analyzed in sections 3.3 and 3.4.

3.1 PULSE-WIDTH MODULATION SCHEME

In Fig. 3.1, the output voltage waveforms for both 2-tap FIR signaling and the PWM signaling are shown. Transmitter output is normalized to +/- 1V. Transmission channel model has a monotonically decreasing transfer function. It corresponds approximately with PCB loss model for single trace. The current channel losses are adjusted using the typical bandwidth parameter BW_{3dB}.

Actual channel losses BW_{3dB} = 0.35 GHz corresponds with the 70 cm long PCB trace. A similar result is shown for 25 m long coaxial cable in [16]. The optimum duty-cycle settings are strongly dependent on the channel characteristics, see Fig. 3.1. In this case the optimal coefficients are f = 0.62 and dc = 56 % for FIR pre-distortion and PWM pre-distortion, respectively. The PWM pulse shape is similar to Manchester code for duty-cycle (dc) parameter setting to 50 %. However, the Manchester code has fixed amplitude at 50 % without a tunable duty-cycle [16]. A duty-cycle of 100 % corresponds to transmission of a normal polar NRZ data signaling without pre-distortion. In [35] the symmetrical impulse response for the channel where dielectric losses dominated is shown. The measured results and advanced simulation model shows that this channel has nonsymmetrical pulse response see Fig. 3.1.

The coefficients for time domain simulations are rewritten according to [16] as $c_1 = f$, $c_2 = f$ 1 with $f \in \{0.5...1\}$, resulting in one coefficient f that can be used to control the pre-distortion level. Function $p_{fir}(t)$ can be simply formulated as

$$p_{fir}(t) = \begin{Bmatrix} 0 & t < 0 \\ f & 0 \le t < T_b \\ f-1 & T_b \le t < 2 \cdot T_b \\ 0 & 2 \cdot T_b \le t \end{Bmatrix}, \tag{3.1}$$

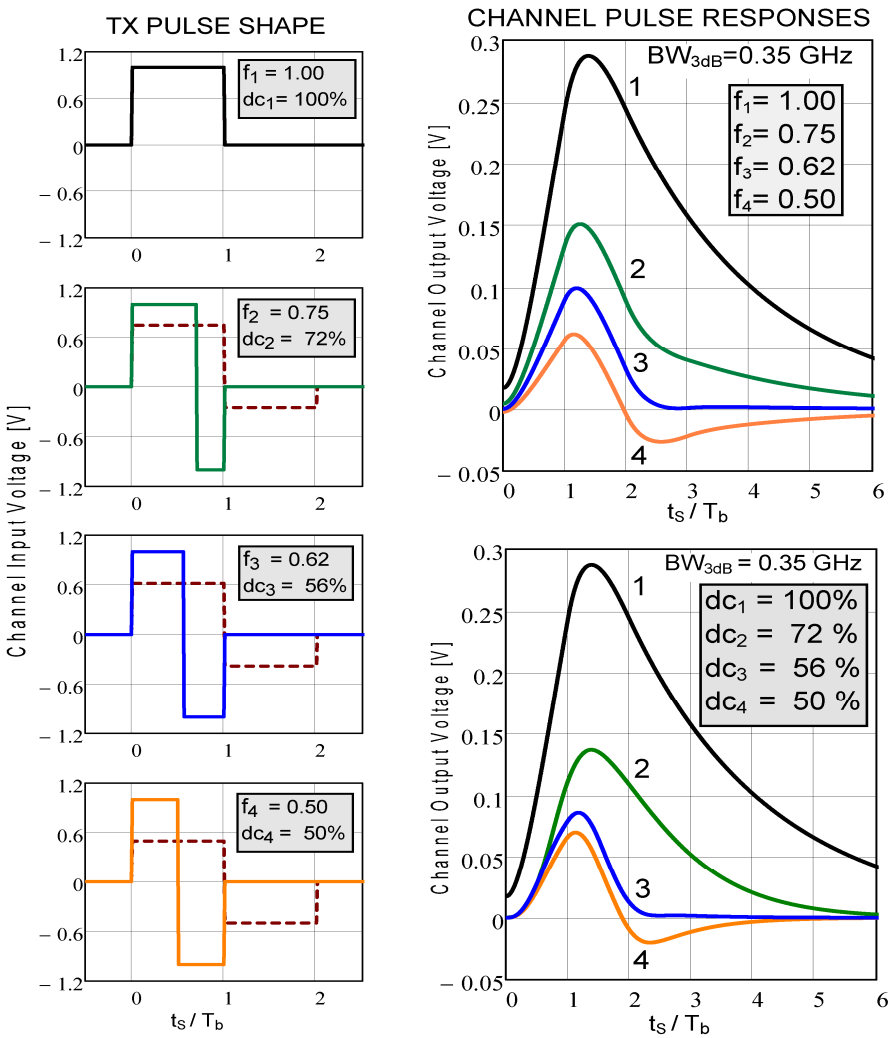
where f and f 1denote the values of the first and the second FIR taps, respectively, and T_b represent the symbol period (T_b = 200 ps).

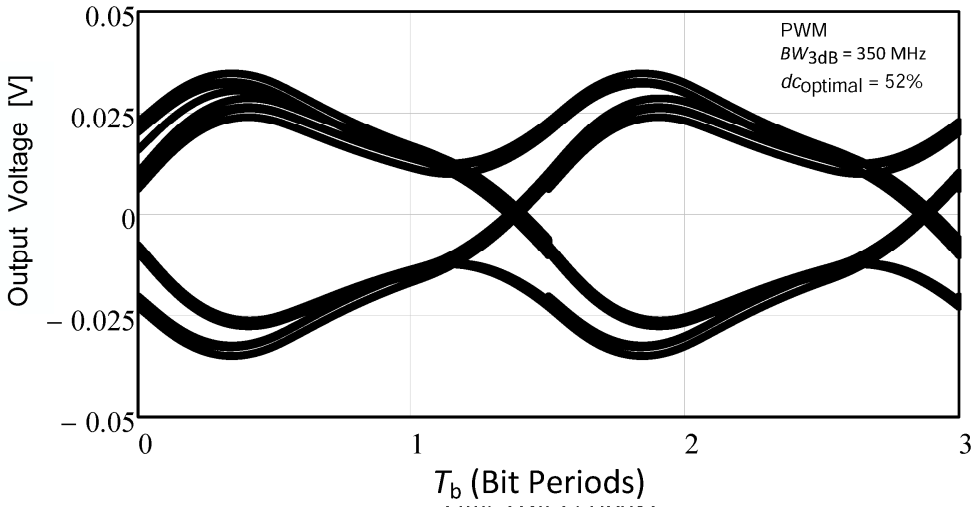
The PWM pulse $p_{pwm}(t)$ is defined as follows, see Fig. 3.1

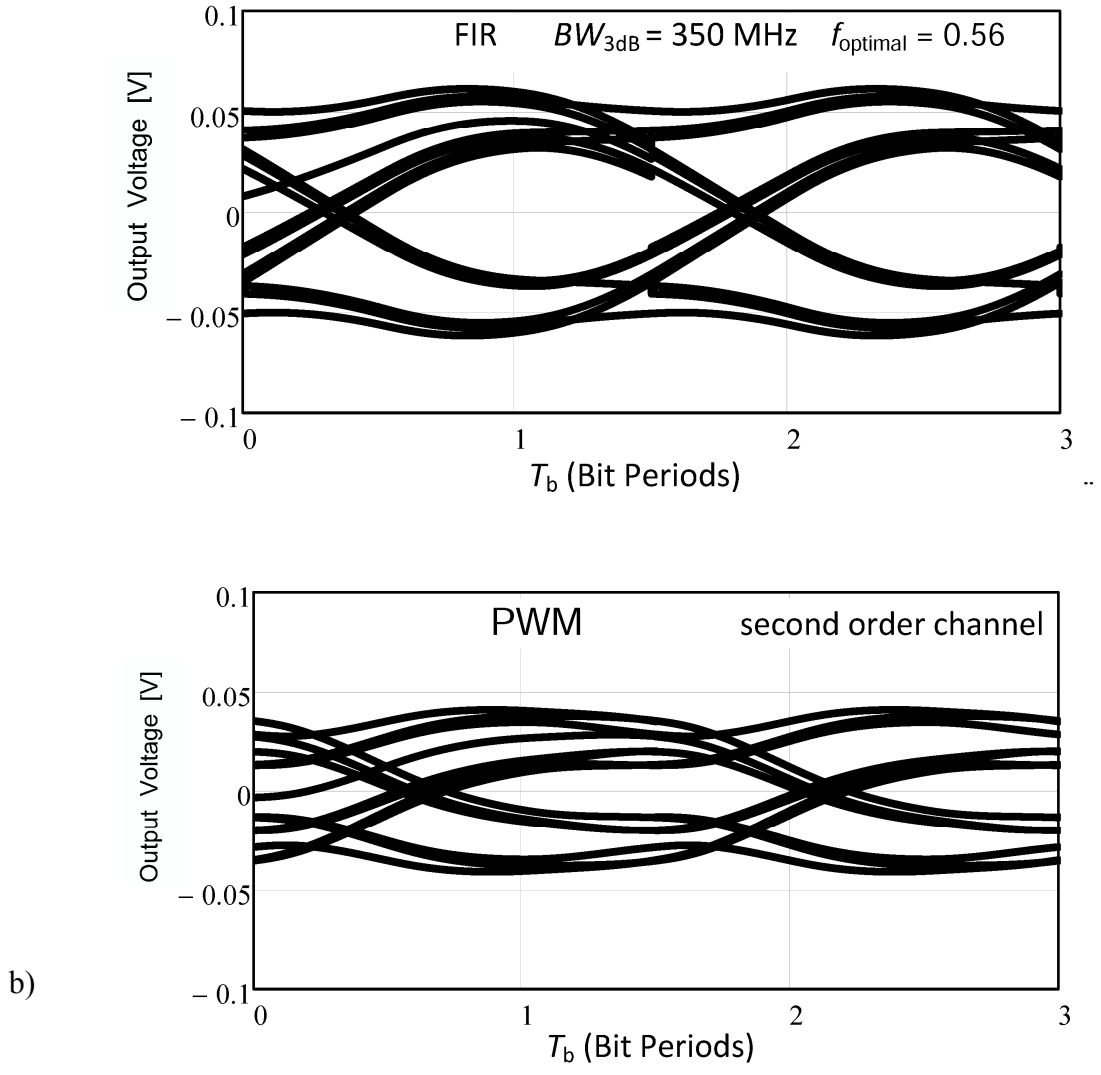
$$p_{pwm}(t) = \begin{Bmatrix} 0 & t < 0 \\ 1 & 0 \le t < dc \cdot T_b \\ -1 & dc \cdot T_b \le t < T_b \\ 0 & T_b \le t \end{Bmatrix}, \tag{3.2}$$

where dc denotes the duty-cycle ($0.5 < dc < 1$ fits best to PCB backplanes) and T_b again represents the symbol period (T_b = 200 ps).

a)


TX PULSE SHAPE
f1 = 1.00
dc1= 100%
f2 = 0.75
dc2 = 72%
f3 = 0.62
dc3 = 56%
f4 = 0.50
dc4 = 50%
Channel Input Voltage [V]
ts / Tb
CHANNEL PULSE RESPONSES
BW3dB=0.35 GHz
f1= 1.00
f2= 0.75
f3= 0.62
f4= 0.50
BW3dB = 0.35 GHz
dc1 = 100%
dc2 = 72 %
dc3 = 56 %
dc4 = 50 %
Channel Output Voltage [V]
ts / Tb


PWM
BW3dB = 350 MHz
dcoptimal = 52%
Output Voltage [V]
Tb (Bit Periods)



b)

Fig. 3.1: Eye diagram outputs**:** a) TX pulse shapes (T_b = 200 ps) of FIR filter (dashed line) and PWM filter (solid line) and simulated channel pulse responses for transmission line bandwidth BW_{3dB} = 0.35 GHz, b) output eye diagrams for optimal coefficients setting and second order channel response for PWM.

From eye diagrams presented in Fig. 3.1b is it possible to do following conclusions. PWM method better compensate channel losses for first order channel model. Despite the overall reduction in the signal amplitude a significant jitter and ISI reduction in PWM response is visible. As a result of improvements in these parameters eye opening is greater than in the case of the FIR filter. The problem in signal integrity can occur when the channel path is affected by other disturbing elements such as vias, additional aggressor lines. Thus, signal reflection and a steeper drop in signal level at higher frequencies cause the significant degradation of leading edges shaping. In this case higher order channel modeling must be applied to the modeling of these additional signal degradations. If transfer function for second order channel defined and analyzed in section 4.4 is used the eye opening is significantly reduced, see last eye diagram in Fig. 3.1b. In this case pre-emphasis techniques successfully used for first order channel response fail. However, as will be shown below, it is possible to introduce into the shaping signal additional parameter to more sophisticated shaping. It allows to significantly decrease jitter and ISI effect of transmission channel in output signal. Thus, the data signal that was previously undetectable for receiver due to the significant BER growth, is detected with better BER parameters.

The time-domain pre-distortion method described above has the advantage of only one coefficient settings to achieve optimal pre-emphasis level. Thus it can be very simplified implementation process of adaptive duty-cycle settings for control algorithms which are widely used for receiver equalization. A sign-sign block least mean squares (LMS) algorithm can be used as shown in [35]. From Fig. 3.1 it is clearly seen that replacing FIR pre-distortion with PWM pre-distortion, when amplitude resolution requirements are replaced with timing resolution requirements, can be beneficial for future low voltage CMOS technologies where stringent noise margins can reduce the usable voltage amplitude for pre-distortion level settings. It is obvious that optimal pulse shaping (coefficient setting) for analyzed channel is accompanied by a reduction of signal amplitude. It should be noted that the minimum transmitted signal swing clearly depends on the receiver sensitivity and channel frequency response. This is shown in [18] where reduction in receiver sensitivity from 100 mV to 25 mV changed the minimum required transmitter signal swing from 600 mV to 200 mV while the same BER is maintained.

3.2 PWM-RC PRE-DISTORTION TECHNIQUE

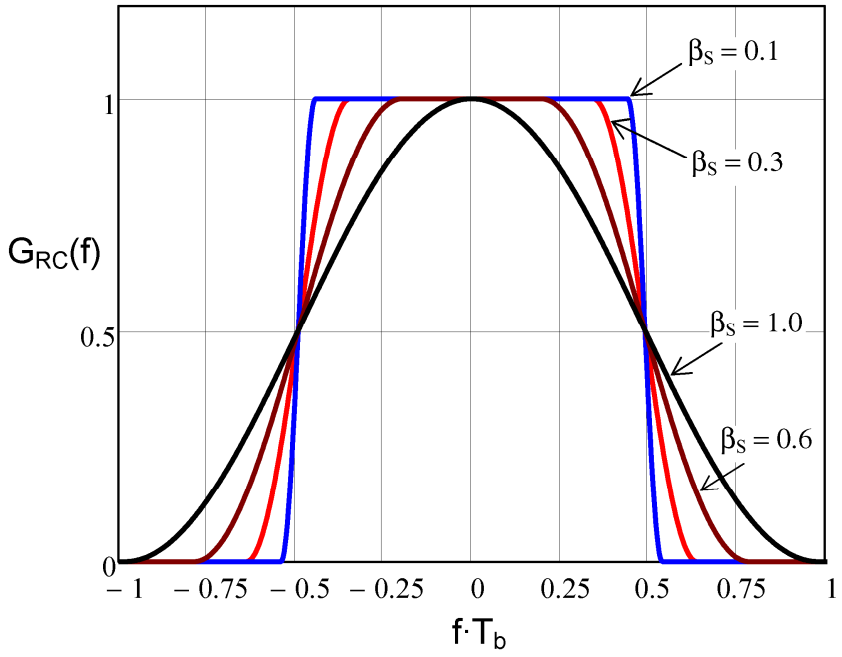
The conventional PWM scheme based on rectangular pulse shaping has many harmonic high-frequency components [16]. It can cause problems in practical implementation of this method in real communication systems, e.g. PCI Express based ones. A method proposed in this work uses a raised cosine pulse scheme to reduce crosstalk noise. The combination of PWM pre-distortion technique and appropriate pulse shaping method can provide an effective reduction of high-frequency components of the pulses. This preserves the beneficial properties of time-domain pre-distortion technique and consequently the crosstalk susceptibility as a main disadvantage of PWM scheme can be reduced. The raised cosine signaling is the process when the waveform of transmitted pulses is changed in order to achieve better signal adaptation to the band-limited channel. The raised-cosine filtering is widely used in digital modulation techniques to effectively suppress ISI. In the dissertation the PWM-RC scheme is introduced for the first time. In the frequency domain, a function is defined in MathCAD formulation as

$$G_{RC}(f,\beta_S)=\left\{\begin{array}{lll} 1 & if & \left|f\cdot T_b\right|<\frac{1-\beta_S}{2} \\ \frac{1}{2}\cdot\left\{1-sin\left[\frac{\pi}{\beta_S}\left(\left|f\cdot T_b\right|-\frac{1}{2}\right)\right]\right\} & if & \frac{1-\beta_S}{2}\le\left|f\cdot T_b\right|\le\frac{1+\beta_S}{2} \\ 0 & if & \left|f\cdot T_b\right|\ge\frac{1+\beta_S}{2} \end{array}\right\} \tag{3.3}$$

The raised cosine pulse transform function is shown in Fig. 3.2a. The parameter β_S (pulse roll-off parameter) is varied from 0.1 to 1.0. It controls the smoothness and the bandwidth, see β_S variation in Fig. 3.2a. The frequency on the x axis is normalized according to the current bit period T_b to easily identify bandwidth variations. For roll-off parameter values close to zero a rectangular shape in the frequency domain is obtained. Extremes are $\beta_S = 0$ and $\beta_S = 1$. In the first case for rectangular shape ($\beta_S = 0$), a significant ripples can cause that neighboring bits will interfere with the current bit. This effect becomes more pronounced for low values of the β_S parameter. It is clearly seen in the time-domain pulse analysis in Fig. 3.2b where the impulse response (inverse Fourier transform) is shown. The second case ($\beta_S = 1$) shows double bandwidth occupation but the impulse response shows more ripple reduction. The impulse response is defined as

$$h(t,\beta_S)=\operatorname{sinc}\left(\frac{\pi\cdot t}{T_b}\right)\cdot\frac{\cos\left(\frac{\pi\cdot t\cdot\beta_S}{T_b}\right)}{1-\left(\frac{4\cdot\beta_S\cdot t}{T_b}\right)^2} \tag{3.4}$$

a)



b)

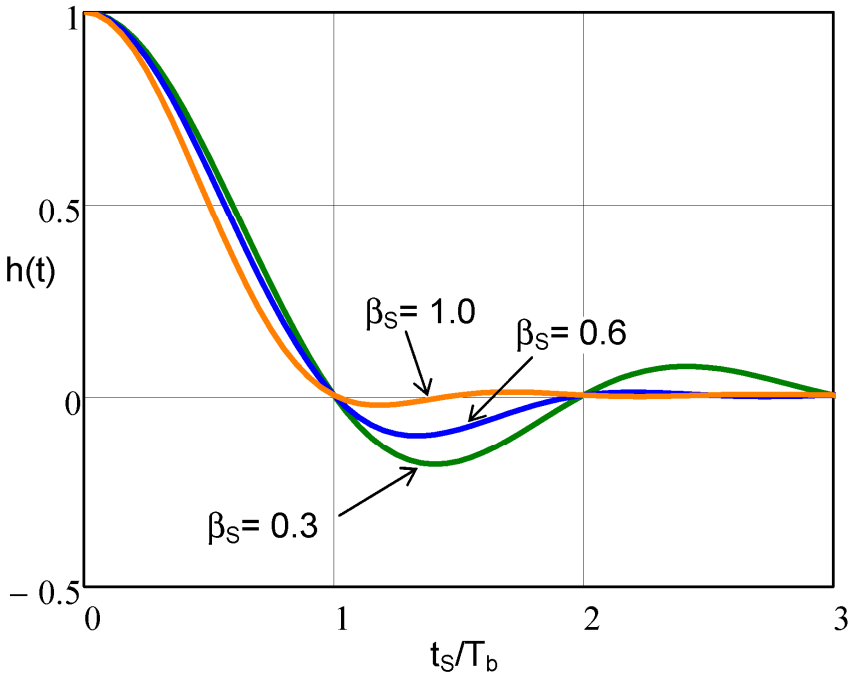


Fig. 3.2: Raised cosine pulse shaping: a) spectral analysis of raised cosine function, b) raised cosine impulse response.

The proposed PWM-RC scheme which is described below still used only one coefficient *dc* to achieve the required value (amount) of pre-emphasis, compare (3.2) and (3.5). Experimental pulse shaping results normalized to unity peak realized in MathCAD according to (3.5) is shown in Fig. 3.3. For the proposed PWM-RC method the pulse shaping in the time-domain is defined as

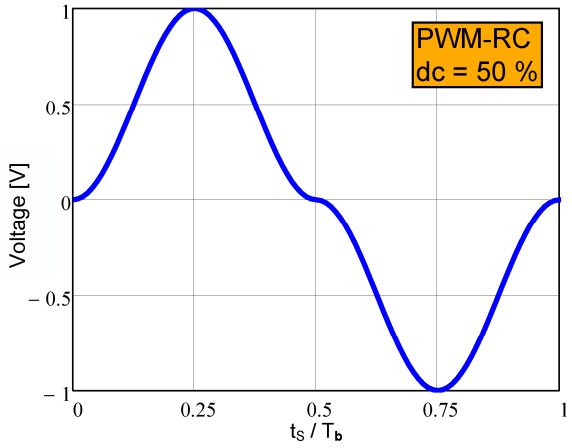
$$s_{RC}(t) = s_1(t) - s_2(t) \tag{3.5}$$

where

$$s_1(t) = \begin{cases} \frac{1}{2 \cdot dc \cdot T_b} \cdot \left(1 - cos \frac{2 \cdot \pi \cdot t}{dc \cdot T_b}\right) & if \quad 0 \le t \le dc \cdot T_b \\ 0 & otherwise \end{cases} \tag{3.6}$$

$$s_2(t) = \begin{cases} \frac{1}{2 \cdot (1-dc) \cdot T_b} \cdot \left(1 - cos \frac{2 \cdot \pi \cdot (t - T_b)}{(1-dc) \cdot T_b}\right) & if \quad dc \cdot T_b \le t \le \cdot T_b \\ 0 & otherwise \end{cases} \tag{3.7}$$

a)



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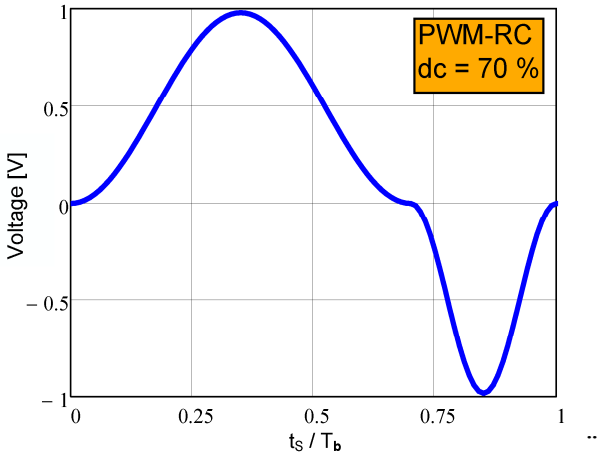


c)

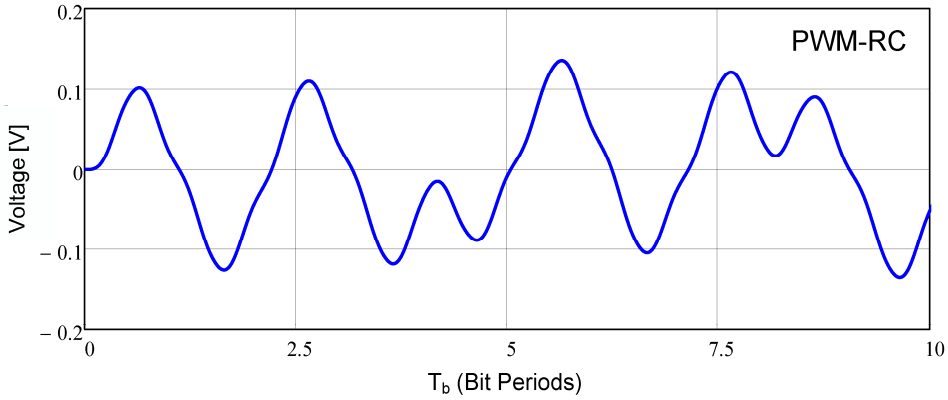


Fig. 3.3: Time-domain analysis: a) PWM-RC pulse shaping - strong pre-emphasis, b) PWM-RC pulse shaping -weak pre-emphasis, c) band-limited channel output, PWM-RC scheme enabled.

3.3 FREQUENCY SPECTRUM ANALYSIS

The spectrum of PWM pulse is more boosted at higher frequencies above Nyquist frequency (0.5 on the x axis) approximately for *d* values from 65 % or less. It can be important factor for higher performance to compensate more lossy channels. The main disadvantage of the PWM method proposed in [16] is that the output pre-distorted signal has many harmonic high frequency components, especially if low-frequency pattern is transmitted. This situation is critical with increasing level (amount) of pre-emphasis. Furthermore, it is necessary to take into consideration that for practical implementations optimal duty cycle coefficients for more lossy channel are just located about strong pre-emphasis level between 50 % and 60 %. In Fig. 4.4b the frequency spectrum analysis for both conventional PWM and proposed PWM-RC pre-distortion methods is shown. In this case a strong pre-emphasis level (dc = 50%) is chosen. It is clearly demonstrated that for proposed PWM-RC pulse the high-frequency harmonic components are more attenuated. It can be an important factor to suppress high-frequency harmonic content in a conventional PWM scheme and also a potential crosstalk noise. Both signal pulses have T_b = 200 ps.

The PWM pulse $p_{pwm}(t)$ definition is used to calculate the spectrum of the PWM filter by taking the Fourier transform, similarly in [16] as

$$P_{pwm}(\omega) = \int_{-\infty}^{+\infty} p_{pwm}(t) \cdot e^{-j\omega t} dt = \int_{-T_s/2}^{(d-0.5)\cdot T_s} e^{-j\omega t} dt - \int_{(d-0.5)\cdot T_s}^{T_s} e^{-j\omega t} dt \,. \tag{3.8}$$

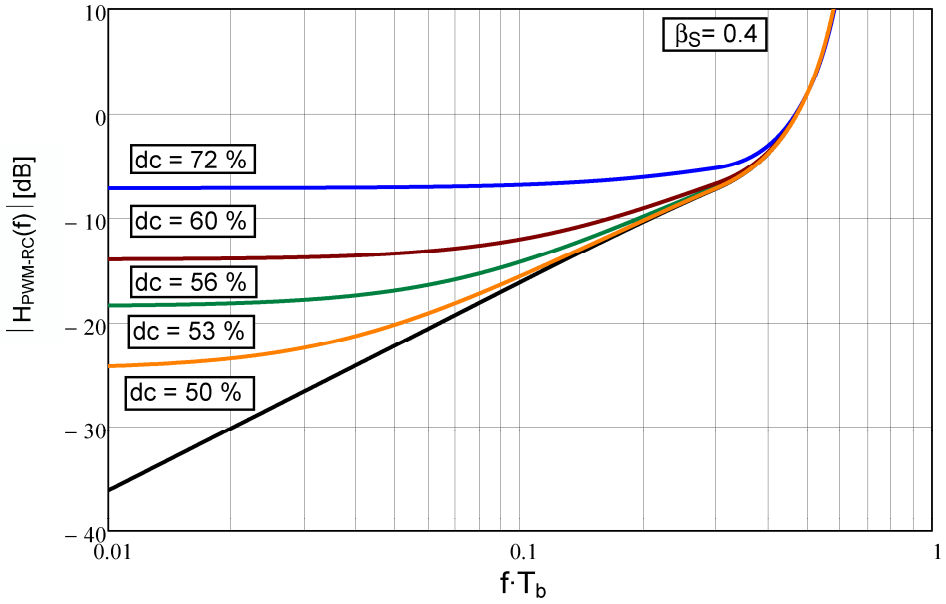
Now for proposed PWM-RC pre-emphasis the frequency domain transfer functions can be calculated according to (3.5) by taking (3.6) and (3.7) into account. The frequency transfer function response for PWM-RC filter can be calculated as follows

$$H_{PWM-RC}(\omega) = \frac{P_{pwm}(\omega)}{G_{RC}(\omega)} \tag{3.9}$$

In Fig. 3.3a the PWM-RC filter transfer function for various duty cycle coefficients settings is shown. In this case, the pulse roll-off parameter β_S is set to 0.4. The proposed PWM-RC scheme is capable of higher loss compensation around Nyquist frequency (0.5 on the x axis). For example, the gain 10 dB of PWM-RC equalizer corresponds with value 0.6 on the x axis, see Fig. 3.3a. The

conventional PWM filter shows the same gain value but for the value 0.8 on the x axis. The proposed method allows not only to set the optimal pre-emphasis level by changing the duty cycle but the β_S parameter can be used to adjust the optimal equalization characteristic according to current channel losses. It is obvious that the Nyquist frequency varies according to the actual data transmission rate. For lower data rates the β_S parameter can be set to a higher value. In this case high frequency noise and crosstalk, which can degrade performance in real systems, are effectively reduced because high frequency boost is tempered. For higher data rates it is possible to achieve higher channel loss compensation because the amount of equalization around the Nyquist frequency can be effectively adjusted depending on where current high slopes in channel frequency response occur.

a)



b)

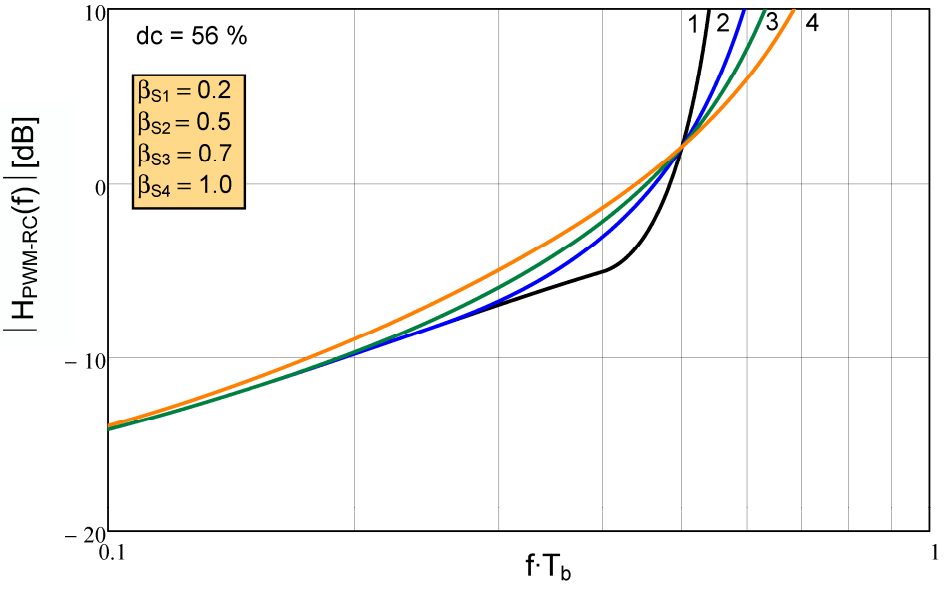


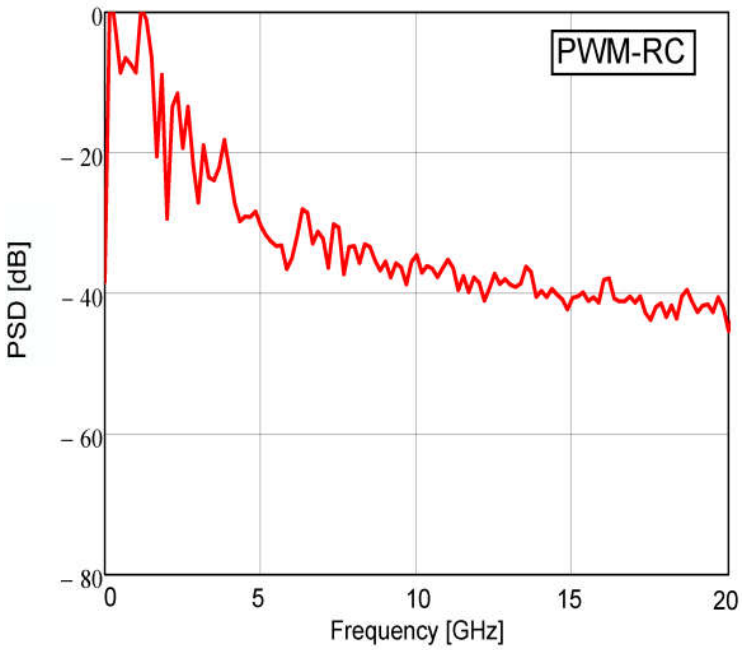
Fig. 3.3: PWM-RC frequency domain analysis: a) Calculated magnitude of PWM-RC filter transfer function (β_S = 0.4) b) high-frequency compensation settings for different values of β_S parameter.

The main advantage of the proposed PWM-RC pre-distortion method lies in its adjustable variability. Comparing the conventional PWM pre-emphasis and FIR pre-emphasis transfer functions is shown in [16]. In this case the proposed PWM-RC method retains the same behavior for low-frequencies as the FIR filter and conventional PWM filter. The PWM scheme due to the time-varying has high-order transfer function and so effective gain of the PWM filter increases to infinity [16]**.** It can cause also additional high-frequency noise in output pre-distorted signal even if weak pre-emphasis is applied. The PWM-RC pre-emphasis technique is capable to find optimal settings for both low-frequency and high-frequency signal content and additional high frequency content can be minimized due to the adjustability at higher frequency compensation, see Fig. 3.3b.

3.4 SIGNAL SPECTRUM ANALYSIS

The main disadvantage of conventional pre-emphasis methods as previously described above is a strong susceptibility to crosstalk [15], [16]. In [16] by using a simple Fourier series calculation it is shown that the output spectrum of conventional filter exhibits more high frequency components if low-frequency (LF) pattern (transmitting many 1s in succession) is transmitted. It can cause complications if channel which has been equalized is predisposed to crosstalk formation. In Fig. 3.4 and Fig. 3.5 the frequency spectrum analysis at the band-limited channel output for both PWM methods is shown. In the first case the strong pre-emphasis setting is selected. The real random high-speed 5 Gbps data stream is formed. The proposed PWM-RC method significantly reduces high frequency harmonic components.

a)



b)

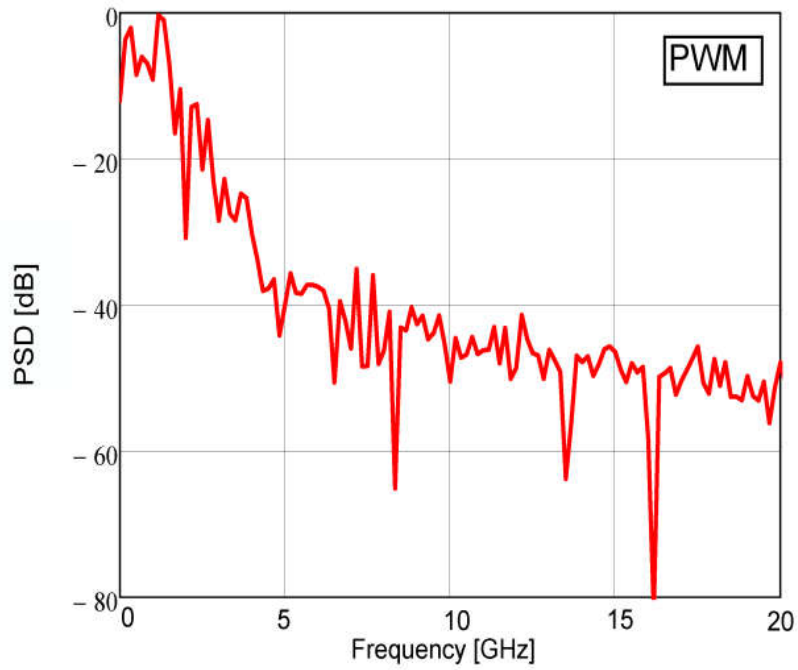
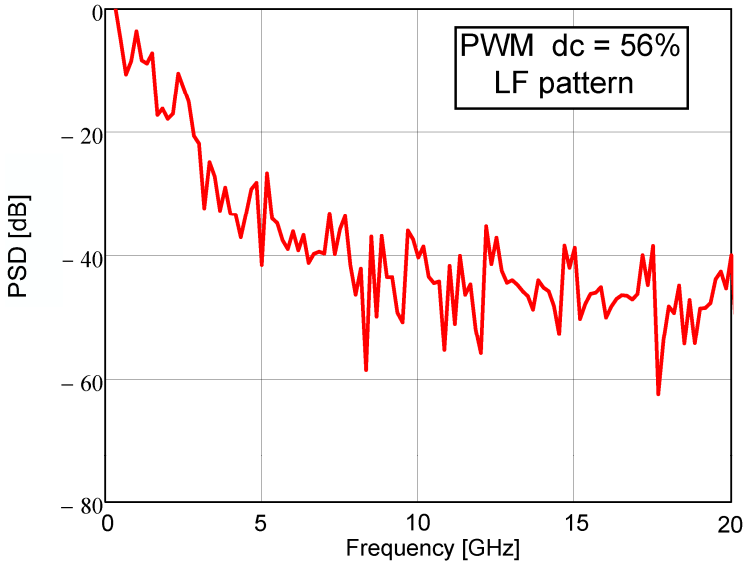


Fig. 3.4: Channel output frequency spectrum analysis if random data pattern is transmitted at 5 Gbps (BW_{3dB} = 150 MHz, strong pre-emphasis enabled *dc* = 50 %): a) PWM-RC scheme b) PWM scheme.

In the second case the frequency spectrum analysis is focused on the problem described above. The optimal pre-emphasis level is enabled. Now, the LF pattern is transmitted over the band-limited channel. We can see again the significant reduction in high-frequency components. It can be concluded that the proposed PWM-RC scheme is able to sufficiently compensate the additional high-frequency components for lower switching frequency. This behavior is close to conventional FIR filter where the filter exhibits less power for lower switching frequency. For the HF pattern the difference between FIR and PWM scheme is only in phase (time-shift) [16]. However, in Fig. 3.5 it is clearly seen additional high frequency harmonic content compensation if proposed PWM-RC scheme is used.

a)



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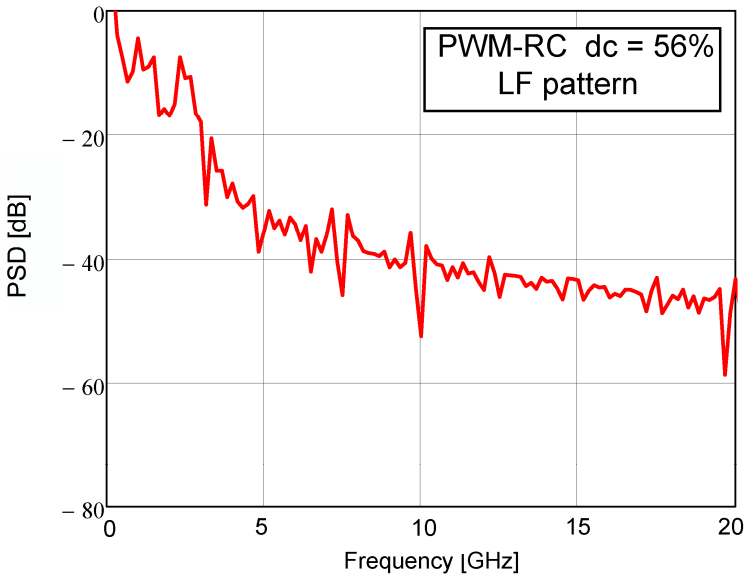


Fig. 3.5: Channel output frequency spectrum analysis if LF data pattern is transmitted at 5 Gbps (BW_{3dB} = 350 MHz, optimal pre-emphasis enabled): a) PWM-RC scheme b) PWM scheme.

3.5 OPTIMIZATION OF RAISED-COSINE PULSE

Based on the results discussed in section 3.4 and the results presented in [41], [42] a modified pulse is proposed. Thus, more variants of signal conditioning are applicable to improve signal integrity through the lossy channels. As can be shown in Fig. 3.1a pulses at the output of the transmission channel are spread over several symbol periods with exponential character.

The invention lies in adaptation of this function to the pulse shaping filter which uses time-domain and amplitude pre-emphasis. Thus, a novel pulse shaping is achieved. The assumptions are based on the similar functionality as in the case of equalizers used in high-speed communication signaling where equalizer transfer function is ideally inverse to transmission channel response. Thus, the conventional raised-cosine pulse shaping is replaced. As will be shown below, this causes better pulse adaptation to pass through the lossy transmission channel. Together with optimized adaptive pulse shaping a better performance is achieved compared to the conventional pulse. The modified pulse is defined in time-domain as

$$s_{\exp}(t) = A_{OPT}\,\mathrm{sinc}\left(\frac{\pi t}{T_b}\right)\left[\frac{4\beta_x t\pi z_1 + 2\beta_x^2 z_2 - \beta_x^2}{4\pi^2 t^2 + \beta_x^2}\right] \tag{3.10}$$

where

$$z_1(t) = \sin\left(\pi\alpha_x \frac{t}{T_b}\right) \quad \text{and} \quad z_2(t) = \cos\left(\pi\alpha_x \frac{t}{T_b}\right) \tag{3.11}$$

The key pulse parameter which establishes an inverse exponential function is β_x. The modification of the proposed pulse shaping lies in two parameters. The first parameter A_{OPT} is adaptively changed together with parameter β_x which is defined as

$$\beta_x = \frac{\ln 2}{\alpha_x B_x} \tag{3.12}$$

where B_x variable is set similarly according to analysis described above in section 3.2 where pulse-width raised cosine pre-emphasis is described. The maximum value $B_x = 1/(2T_b)$ but optimal value will be lower, $B_{x\text{opt}} = 1/T_{\text{bopt}}$. The variable α_x is represented as in the case of raised cosine pulse roll-off factor.

3.6 SIMULATION RESULTS

In Fig. 3.6 all the analyzed pulses are shown. It is obvious that the magnitudes of the two largest side lobes of the pulses based on the flipped-exponential function are smaller than the magnitudes of the two largest side lobes of the conventional raised-cosine pulse. If we compare both pulses based on the flipped-exponential function, we can see additional better performance for optimized exponential pulse where magnitudes of two largest side lobes have still decreasing tendency. Moreover, notice the difference in pulse shaping of optimized exponential pulse where steeper transition is evident. This reduces pulse width and minimizes the pulse spreading due to the channel ISI effect.

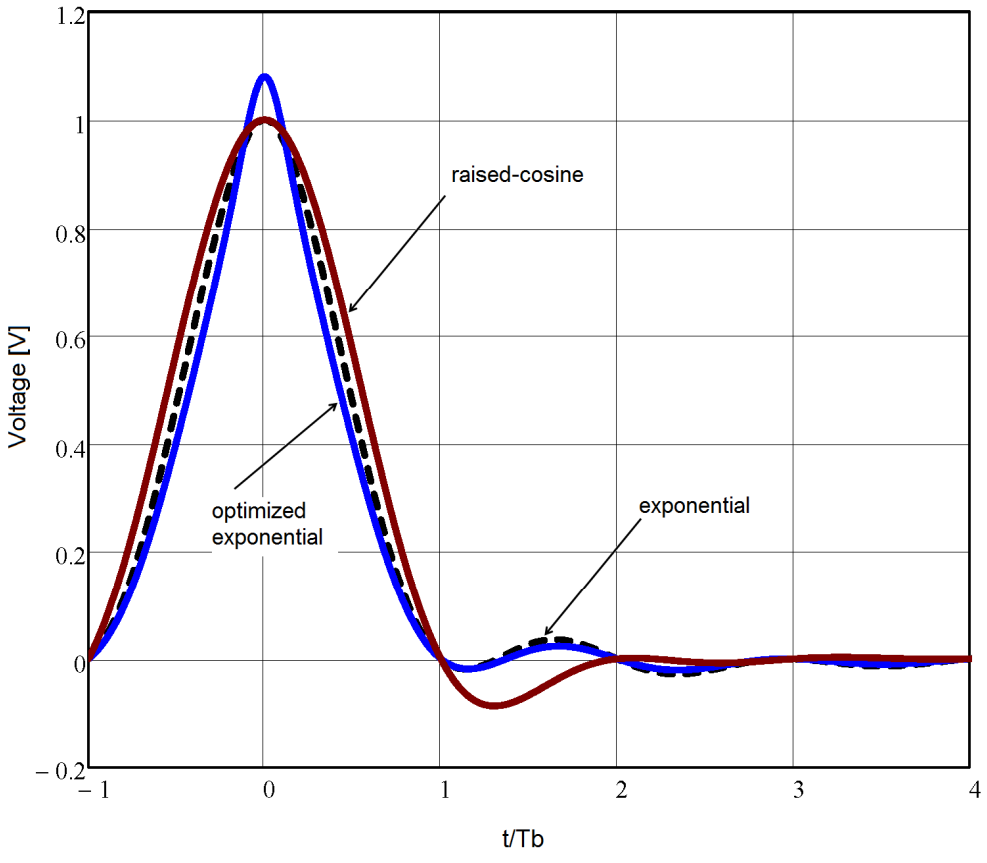


Fig. 3.6: Impulse responses of all compared pulses.

The parameter β_x can be adjusted by changing two variables. Both of the parameters are swept linearly. However the response of β_x is different for each of them. Increasing value of the first variable α_x causes an exponential decreasing of β_x. Increasing value of the second variable T_b shows linear increasing of β_x. This situation is clearly shown in Fig. 3.7.

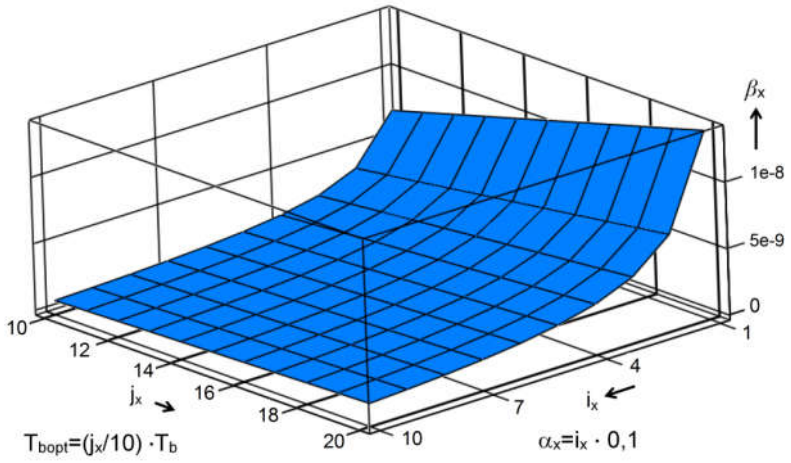


Fig. 3.7: Dependence of β_x when variables α_x and T_{bopt} are linearly swept.

For optimal setting of both parameters, it is necessary to analyze their impact on output signal. In Fig. 3.8 it is shown the impulse response and output eye diagram of proposed pulse during the α_x variation.

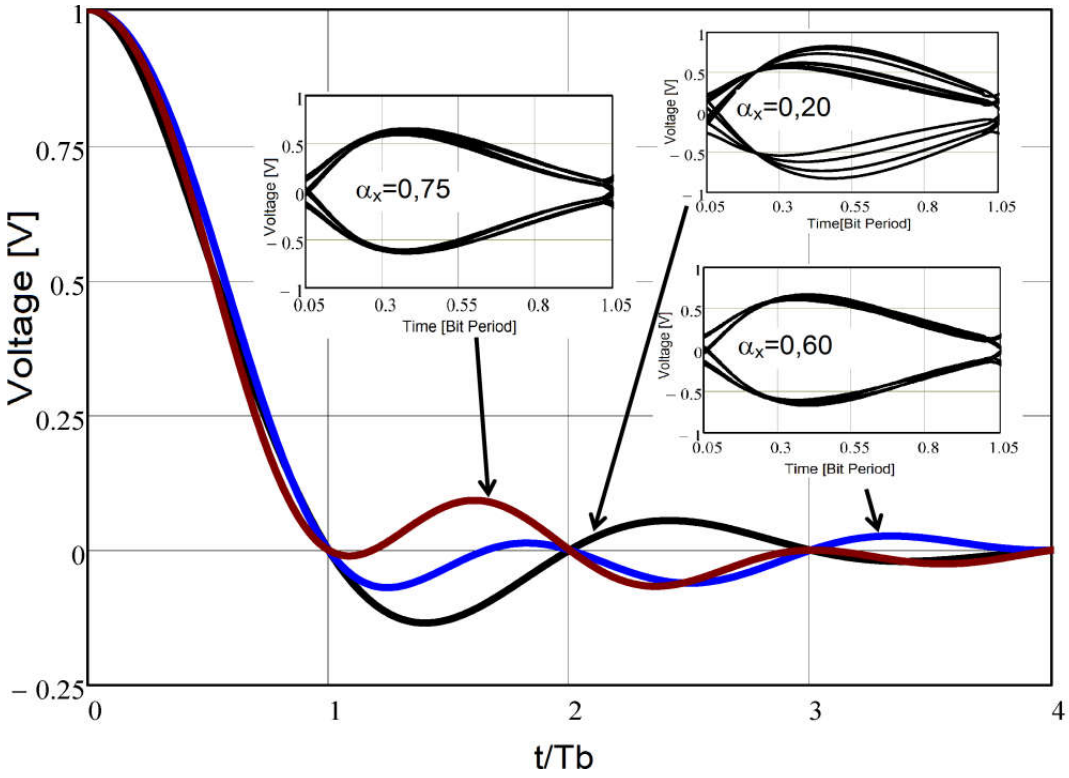


Fig. 3.8: Impulse response and eye diagram performance for various α_x.

It is obvious that appropriate α_x setting can improve jitter and eye opening. In this case transmission channel with small losses was used. Optimal α_x value lies approximately in the middle of range ($\alpha_x = 0.60$). Two possible extremes of α_x are 0 and 1 but in this case eye diagram shows strong ISI. Very low value of α_x can cause significant ISI between symbols and additional signal jitter as well higher α_x values. The second variable T_b shows additional jitter during variation. The situation is clearly shown in Fig. 3.9. As in the previous case, an optimal eye opening is strongly dependent on accurate setting of variables. Both variables complement each other due to the different response of β_x parameter on variation of each of them, see Fig. 3.9. The optimal setting process for β_x parameter includes two main steps. Firstly, the optimal value of α_x variable is found with a set of maximum value of B_x. The next step involves adjusting of variables T_b to achieve jitter reduction.

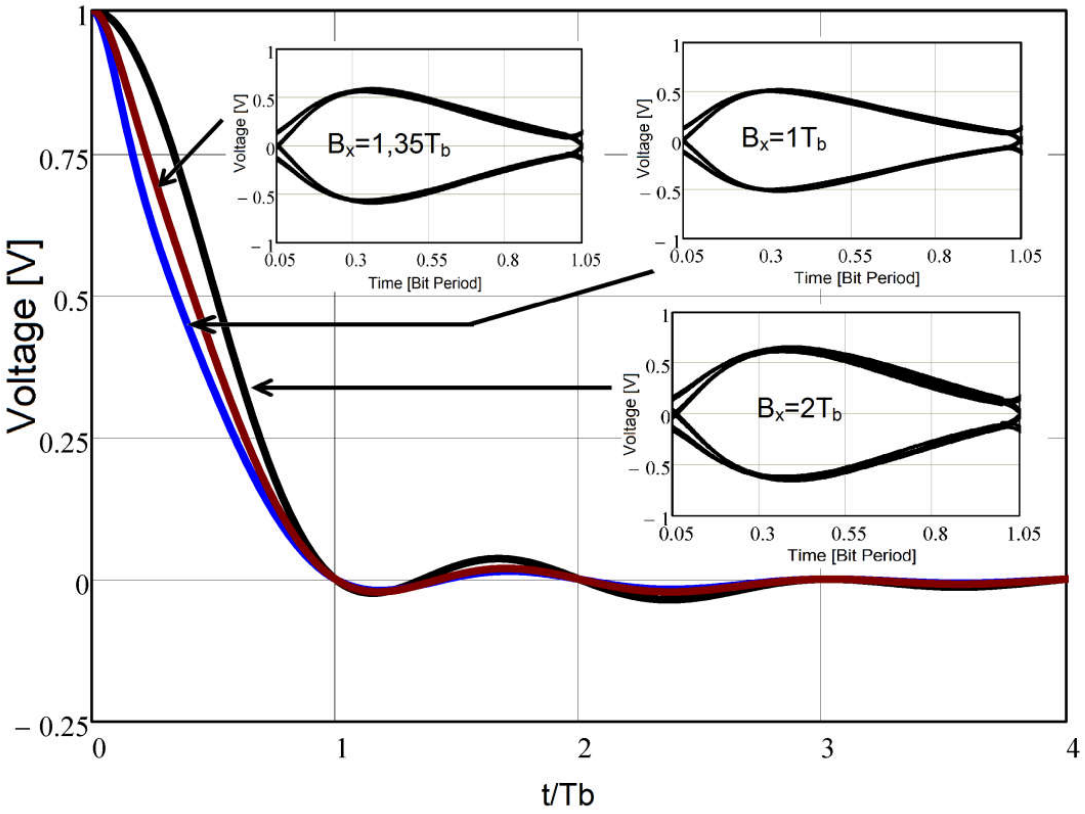


Fig. 3.9: Impulse response and eye diagram performance for various T_b.

4 EXTENSION OF PWM-RC TECHNIQUE FOR SECOND ORDER CHANNELS

In previous chapter it was shown great potential of PWM equalization technique to improve signal quality at the output of channel with high losses. But the first order channel must be replaced by more complex transfer function because of more disturbing factors which can occur in advanced multi chip communications systems. Other effects as crosstalk predisposition, via stubs needed for multilayer PCB's can cause that transfer channel function has character of a higher order functions. Thus, the effect of PWM modulation for the first order channel can be easily suppressed and in some extreme situation may be insufficient for proper equalization of channel losses. In this chapter the concept of the first order equalization to higher order equalization will be extended.

This is the innovative core of the dissertation and shows the great potential of PWM modulation for higher order equalization.

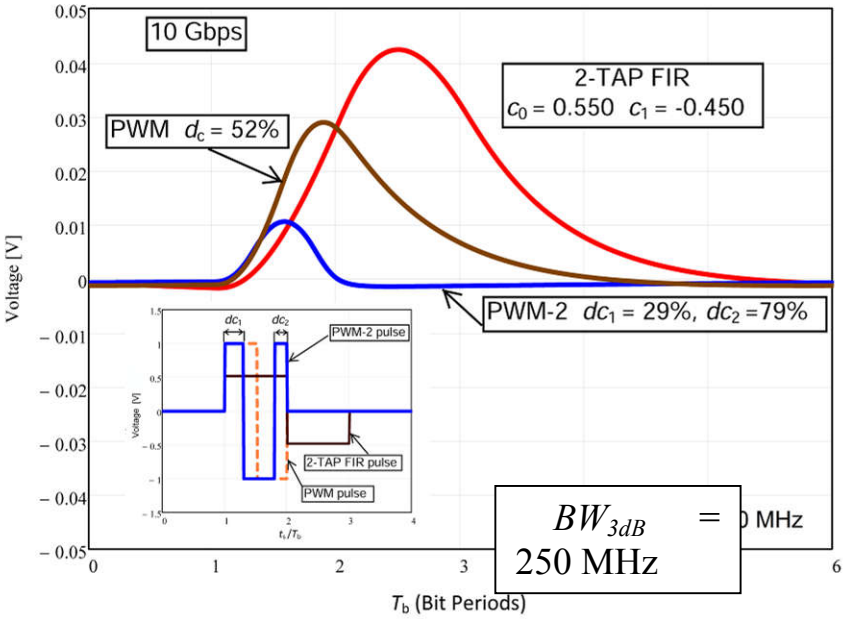
4.1 SECOND ORDER PULSE-WIDTH MODULATION SCHEME

The coefficients for time domain simulations are defined as dc_1 with $dc_1 \in \{0...0.5\}$ and dc_2 with $dc_2 \in \{0.5...1\}$. In this case it is not possible to use one coefficient as above because optimal results of signal shaping require different coefficients setting. Function $p_{pwm\text{-}2}(t)$ in the time domain can be simply formulated as

$$p_{pwm-2}(t) = \begin{cases} 0 & t < 0 \\ 1 & 0 \le t < dc_1 \cdot T_b \\ -1 & dc_1 \cdot T_b < t \le \frac{1}{2} \cdot T_b \\ -1 & \frac{1}{2} \cdot Tb < t \le dc_2 \cdot T_b \\ 1 & dc_2 \cdot T_b < t \le T_b \\ 0 & t > T_b \end{cases}, \tag{4.1}$$

Optimal coefficient setting for the second order pulse-width modulated scheme (PWM-2) is strictly dependent on overall channel impulse response. Due to the more variability in PWM-2 pulse shaping the better adaption to different types of transmission channels may be achieved. As can be seen in Fig. 4.1 the optimal setting of both duty cycle coefficients can result in significant intersymbol interferences reduction. This effect can be achieved for transmission channels with higher losses in relation to the considered transmission rate, see example of transmission channel with significant reduced bandwidth parameter on BW_{3dB} = 250 MHz, where the optimal duty cycle coefficients are dc_1 = 79 % and dc_2 = 29 %. Significant jitter reduction for PWM-2 signalling is obvious, compare all eye diagrams in Fig. 4.1b. However, the significant amplitude reduction in the case of PWM-2 is obvious. It can be a problem if the noise margin is higher than the residual signal amplitude.

a)



b)

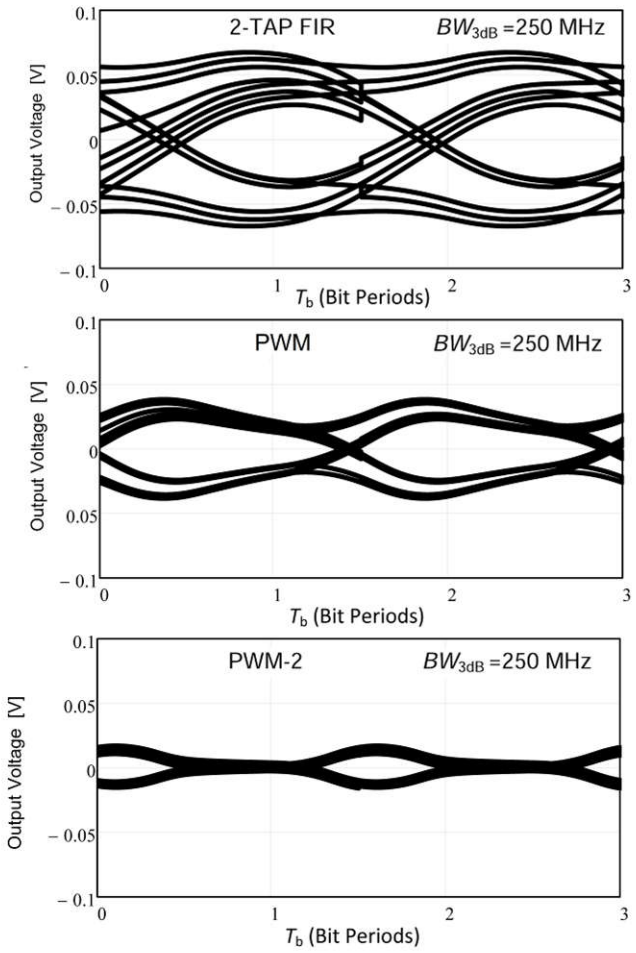
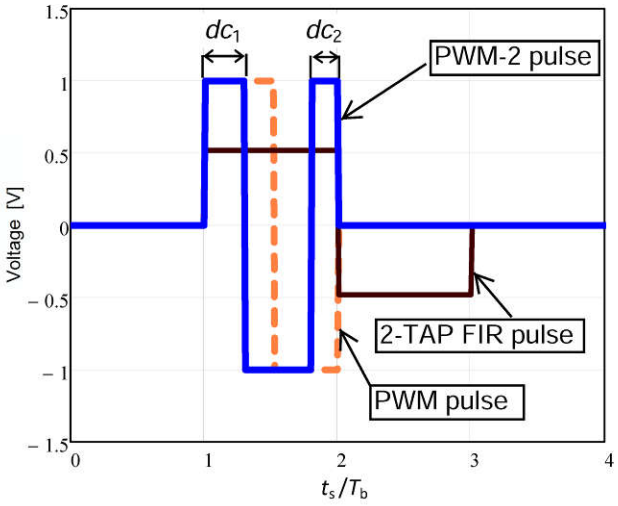
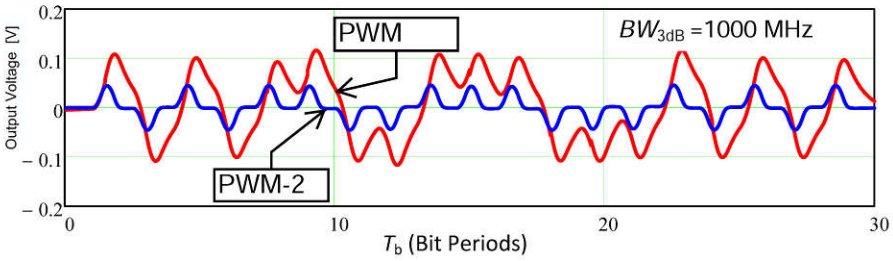


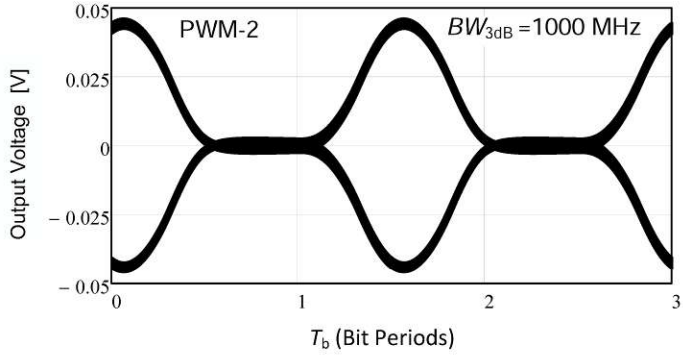
Fig. 4.1: Time-domain analysis: a) impulse responses for FIR, PWM and PWM-2 pulse shaping, b) eye diagrams to evaluate signalling performance after passing through the channel with significant bandwidth restriction.

a)





b)



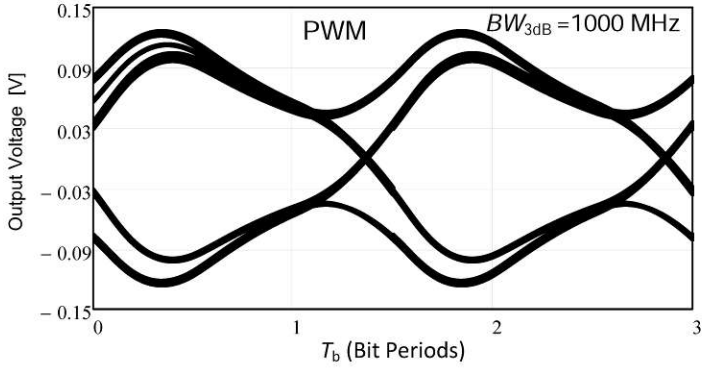


Fig. 4.2: Time-domain analysis: a) PWM-2 pulse shaping with channel output bit stream demonstration, b) the relevant eye diagrams for both PWM and PWM-2 signalling technique.

4.2 FREQUENCY DOMAIN BEHAVIOR

For meaningful comparisons previously presented signalling techniques with newly proposed signalling method the PSD is calculated. The voltage scheme is normalized again to +/-1 V. The spectrum $P_{\text{pwm-2}}(f)$ of the PWM-2 pulse is calculated through Fourier transform of $p_{pwm-2}(t)$ as

$$P_{\text{pwm-2}}(\omega) = \int_{-\infty}^{\infty} p_{pwm-2}(t)\cdot e^{-\text{j}\omega t}dt = \int_{-\frac{T_b}{2}}^{-dc_1\cdot T_b} e^{-\text{j}\omega t}dt - \int_{-dc_1\cdot T_b}^{(dc_2-0.5)\cdot T_b} e^{-\text{j}\omega t}dt + \int_{(dc_2-0.5)\cdot T_b}^{\frac{T_b}{2}} e^{-\text{j}\omega t}dt. \tag{4.2}$$

After simplification:

$$\mathbf{P}_{\text{pwm-2}}(\text{j}\omega) = \frac{2\cdot e^{-\text{j}\omega\cdot(dc_2-0.5)\cdot T_b} + e^{\text{j}\omega\cdot T_b} - 2\cdot e^{\text{j}\omega\cdot dc_1\cdot T_b} - e^{-\text{j}\omega\cdot 0.5\cdot T_b}}{\text{j}\omega} \tag{4.3}$$

Now we can calculate the power spectral density PSD_{pwm} for the PWM-2 filter:

$$PSD(\omega) = \frac{|P(\omega)|^2}{T_b}\sum_{k=-\infty}^{k=\infty} R(k)\cdot e^{\text{j}\omega k T_b} \tag{4.4}$$

$$\begin{aligned}
\text{PSD}(\omega) &= \frac{\left|-2\text{j}\cdot e^{-\text{j}\omega\cdot(dc_2-0.5)\cdot T_b} - \text{j}\cdot e^{\text{j}\omega\cdot T_b} + 2\text{j}\cdot e^{\text{j}\omega\cdot dc_1\cdot T_b} + \text{j}\cdot e^{-\text{j}\omega\cdot 0.5\cdot T_b}\right|^2}{\omega^2\cdot T_b} = \\
&= \frac{\left|-2\cdot e^{-\text{j}\omega\cdot(dc_2-0.5)\cdot T_b} - e^{\text{j}\omega\cdot T_b} + 2\cdot e^{\text{j}\omega\cdot dc_1\cdot T_b} + e^{-\text{j}\omega\cdot 0.5\cdot T_b}\right|^2}{\omega^2\cdot T_b} = \\
&= \frac{1}{\omega^2 T_b}\left\{\begin{array}{l}\left[2\cos\omega dc_1 T_b - 2\cos\left(\omega\left(dc_2-0.5\right)T_b\right) + \cos\omega 0.5T_b - \cos\omega T_b\right]^2 + \\ +\left[2\sin\omega dc_1 T_b + 2\sin\left(\omega\left(dc_2-0.5\right)T_b\right) - \sin\omega 0.5T_b - \sin\omega T_b\right]^2\end{array}\right\}
\end{aligned} \tag{4.5}$$

where $P(\omega)$ is the Fourier transform of $p(t)$ (in this case it is $p_{pwm-2}(t)$ and $R(k)$ is the autocorrelation function for a polar NRZ signaling ($R(k)$ is the same for PWM as for polar NRZ) and is completely calculated in [16].

If (4.5) is taken into the account for calculation of $\text{PSD}_{\text{pwm-2}}$ following graphical outputs in Fig. 4.3 are obtained. Note that the normalization for bit periods on x-axis and y-axis is for better understanding of the performance of the new proposed pulse. The *dc* coefficients are set for equalization of transmission channel with higher losses. The spectrum of PWM-2 pulse is even more boosted at higher frequencies than conventional PWM pulse above Nyquist frequency (0.5 on the x axis). It can be important factor for higher performance to compensate more lossy channels. The main disadvantage of the PWM method proposed in [16] is that the output pre-

distorted signal has many harmonic high frequency components. In the case of PWM-2 pulse it can be expected also significant high frequency content but due to the ability to higher loss compensation the final signal level where equalization will be done is lower than for the conventional PWM filter. Thus, a stronger low pass effect of the transmission channel will be expected. Finally, this effect may contribute to the higher loss compensation of PWM -2 filter with possibility of sustainable eye opening.

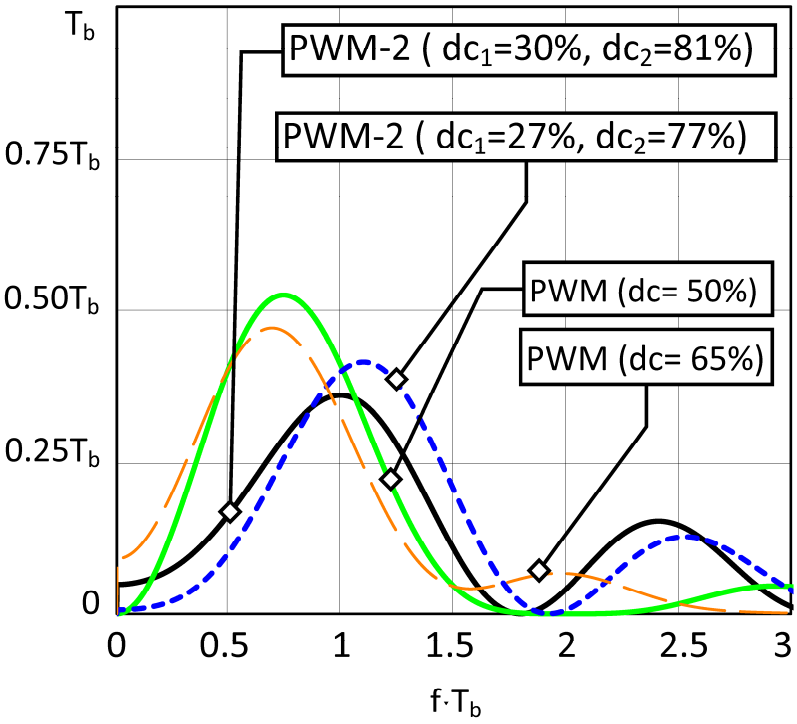


Fig. 4.3: PSD calculation for PWM-2 pulse

4.3 TRANSFER FUNCTION ANALYSIS

The transfer function for new presented PWM-2 filter can be calculated similarly as in the case of PWM filter [16]. For relevant comparison of both types of filters the spectrum of normal polar NRZ pulse of width T_b and height 1 is used for normalization of both functions and the final expression is defined as (5.13) below.

$$H_{PWM-2}(\omega) = \frac{P_{pwm-2}(\omega)}{P_{NRZ}(\omega)} \tag{4.6}$$

The equation for transfer function can be rewritten as :

$$\mathbf{H}_{\text{PWM-2}}(\mathrm{j}\omega) = \frac{\mathbf{P}_{\text{pwm-2}}(\mathrm{j}\omega)}{\mathbf{P}_{\text{NRZ}}(\mathrm{j}\omega)} = \frac{2\cdot e^{-\mathrm{j}\omega\cdot(dc_2-0.5)\cdot T_b} + e^{\mathrm{j}\omega\cdot T_b} - 2\cdot e^{\mathrm{j}\omega\cdot dc_1\cdot T_b} - e^{-\mathrm{j}\omega\cdot 0.5\cdot T_b}}{e^{\mathrm{j}\omega\cdot 0.5\cdot T_b} - e^{-\mathrm{j}\omega\cdot 0.5\cdot T_b}} \tag{4.7}$$

Taking the modulus yields:

$$\left|H_{PWM-2}(\omega)\right| = \frac{\sqrt{\left[2\cos\omega\left(dc_2-0.5\right)T_b+\cos\omega T_b-2\cos\omega dc_1 T_b-\cos\omega 0.5T_b\right]^2+}}{2\cdot\left|\sin\omega 0.5T_b\right|} \quad (4.8)$$

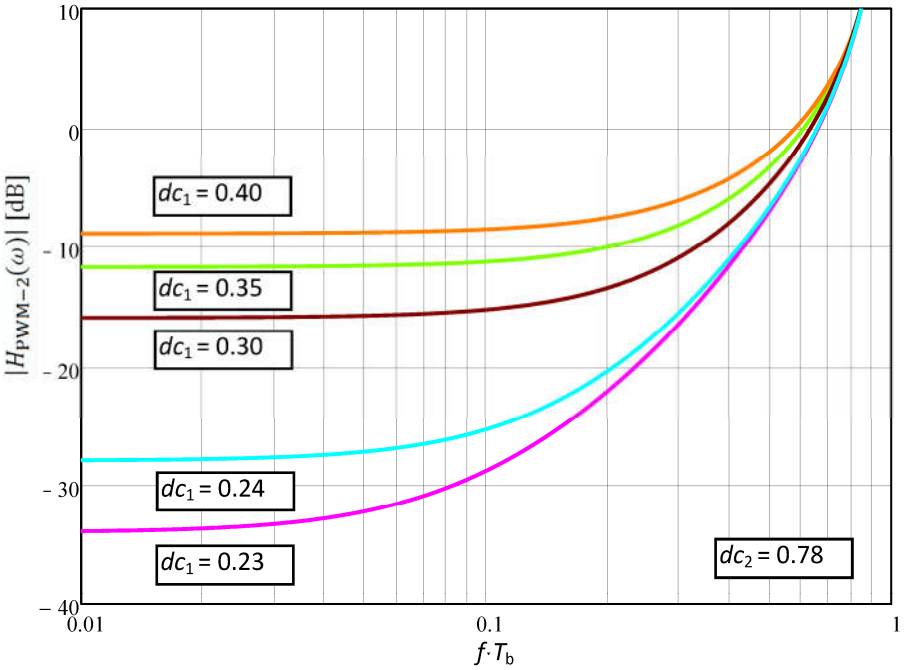


Fig. 4.4: Calculated magnitude of PWM-2 filter transfer. Note that f_N is at 0.5 on the x-axis.

This function is illustrated in Fig. 4.4 for several values of dc_1. The second coefficient dc_2 is set to the value which corresponds with the necessity to higher intersymbol interference compensation. A precondition therefore is that the pulse response of the channel is formed by long tail which does affect more bit periods. One of the evaluated parameters is above discussed low-frequency compensation, compare Tab. 4.1 and Tab 4.2. It is obvious that PWM-2 filter achieve worse performance during compensation of less lossy channels. On the other hand the ability to achieve better loss compensation results for more channels with significant bandwidth restriction is better almost by 26%.

Tab. 4.1: PWM filter loss compensation

Channel BW_{3dB} [MHz]	*dc [%]*	LF compensation [dB]
2000	61	13
1000	57	17
500	54	22
250	52	27
The maximum theoretical compensation is 36 dB, *dc* = 50 %		

Tab. 4.2: PWM-2 filter loss compensation

Channel BW_{3dB} [MHz]	dc_1 [%]	dc_2 [%]	LF compensation [dB]
2000	36	83	9
1000	29	79	16
500	23	79	28
250	23	78	34
The maximum theoretical compensation is 54 dB, dc_1 = 22 %, dc_2 = 78 %			

4.4 EQUALIZED CHANNEL TRANSFER FUNCTION

Last section of the chapter 4 is focused on the practical using of proposed PWM-2 scheme for equalization of second order channel transfer function. If it is considered that during practical implementation and testing low cost coaxial cable will be used we need to simulate appropriate channel pulse response which corresponds with long tail asymmetrical pulse.

The second order system (impulse) response can be similarly, as in the case of the first order function, defined by using of two bandwidth coefficients BW_1 and BW_2 as

$$h_{2nd}(t) = \frac{1}{\frac{1}{2\pi \cdot BW_2} - \frac{1}{2\pi \cdot BW_1}} \left(e^{-2\pi t \cdot BW_2} - e^{-2\pi t \cdot BW_1} \right) \tag{4.9}$$

where the ratio between the both coefficients determine the final pulse shaping.

Thus, pulse with long tail which represents transmission channel prone to intersymbol interferences can be effectively modeled, see pulse shaping variation with different BW coefficients settings in Fig. 4.5. Note that the pulse response with more symmetry is typical for PCB channels with strong RMS roughness effect. On the other hand more asymmetry pulse shaping is typical for channels where skin-effect loss is dominated factor.

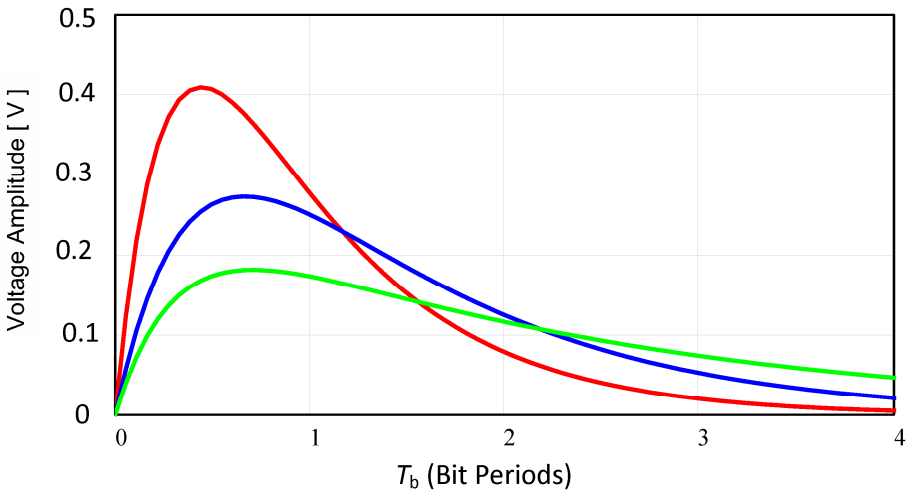
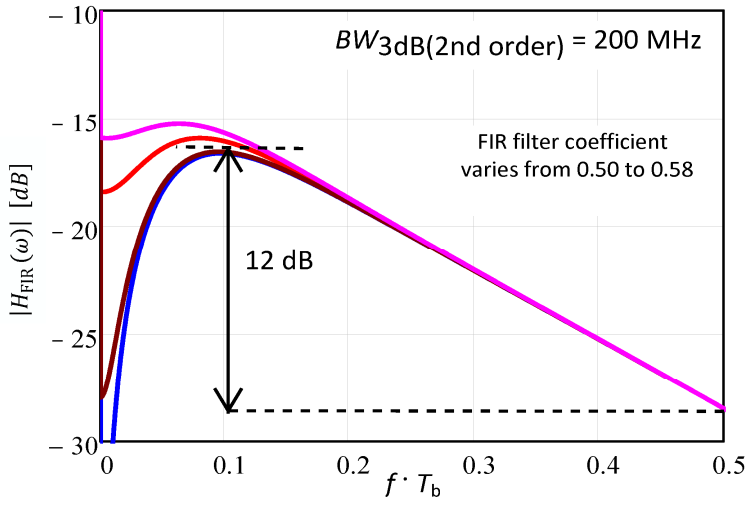


Fig. 4.5: Second order pulse responses.

Finally, the equalized channel transfer function can be calculated for FIR filter and both PWM and PWM-2 filters. As can be analyzed in section 3.1 a theoretical first-order channel with significant bandwidth restriction is sufficiently equalized by using of all three equalization techniques. However, a real cable or PCB trace, especially with additional signal discontinuities, does not have a first order transfer function. From analysis depicted in chapter 4 is obvious that the higher order transfer functions, typically for multilayer boards where vias occurs, still can be equalized with PWM and PWM-RC pre-emphasis with better results than by using of conventional 2-Tap FIR filter. In this case the channel losses exceed more than 35 dB. This is the limitation of conventional PWM scheme where was achieved a maximum loss compensation about 30 dB [16]. Now it can be clearly determined the flatness in the frequency interval [0, f_N]. The channel response for FIR filter is only flat to within 12 dB. It is obvious that FIR filter is not reliable to equalize such high losses. The channel response for PWM filter shows flatness only 7 dB. In the case of the new proposed signaling scheme PWM-2 the flatness is achieved with less than 3 dB differences between low frequency signal level and high frequency signal level. It can be clearly seen from Fig. 4.6c that the PWM-2 filter is able to "almost eliminate" or better said equalize higher channel losses. Thus, the bandwidth where the signal reduction is 3 dB is extended over the all analyzed range of filtration from 0 to f_N. Note that the better equalization is achieved on the lower signal level. Thus, the decisive factor for effective using of the PWM-2 equalization lies also in the current receiver sensitivity and in the current noise content which occurs during the equalization.

a)



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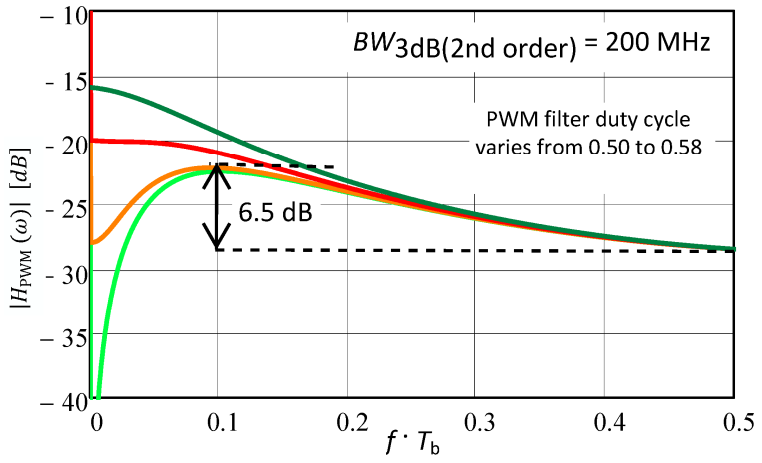


c)

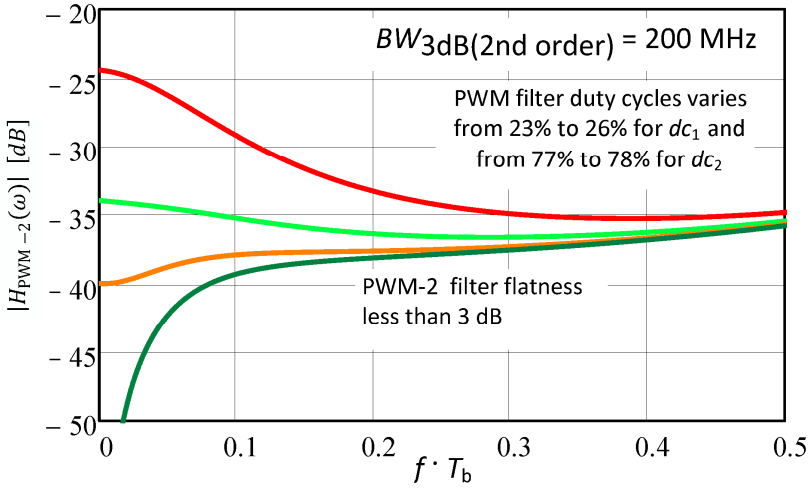


Fig. 4.6: Equalized transfer function, second order channel used: a) FIR filer, b) PWM filter, c) PWM-2 filter.

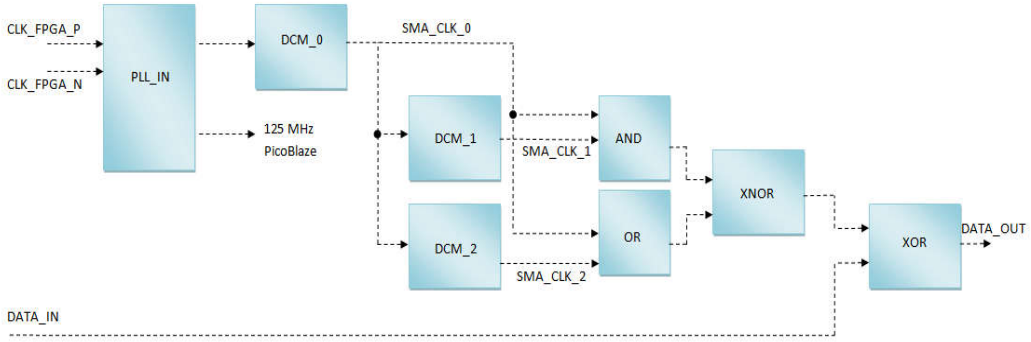
5 IMPLEMENTATION OF BOTH PWM AND PWM-2 SIGNALING TECHNIQUES

In this chapter practical implementations of both PWM and PWM-2 pulse-width techniques are demonstrated. Due to the maximal transmission speed restriction of the digital signal with regard to the currently available development kit the effect of equalization is realized for 300 Mbps and 450 Mbps.

5.1 SIGNAL GENERATION CIRCUITS

FPGA implementation was used for general realization of signalling PWM techniques. In Fig. 5.1a the principle of FPGA implementations is illustrated. Development board with XUPV5 circuit Virtex-5 (XC5VLX110T) was configured. DCM (digital clock manager) represents an electronic component available on FPGAs (notably produced by Xilinx producer). Mainly used for manipulating with clock signals inside the FPGA and to avoid clock skew which would introduce errors in the circuit? Main functions of DCM are multiplying or dividing an incoming clock from external source to the FPGA, for example from a Digital Frequency Synthesizer. Thus, SMA_CLK_0 clock is adjusted in two steps to generate SMA_CLK_1 clock and SMA_CLK_2 clock. For the first order PWM signalling only SMA_CLK_1 clock is needed. For the second order PWM-2 signalling an additional SMA_CLK_2 clock is added. Finally input data stream DATA_IN is merged through XOR with both PWM clocks.

a)



b)

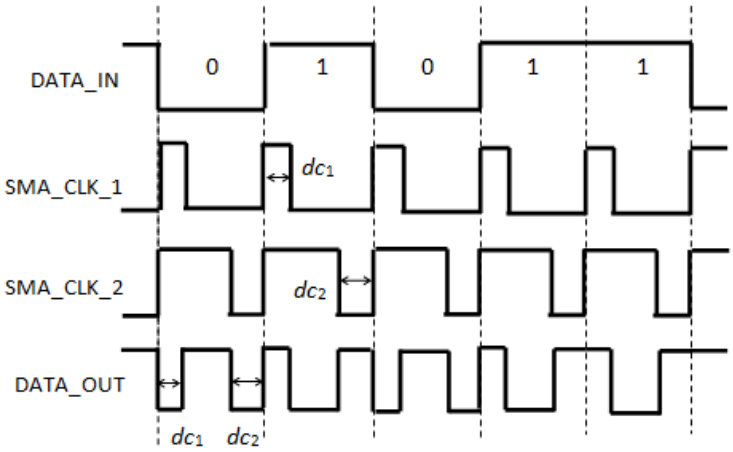


Fig. 5.1: Principle of PWM-2 equalization technique: a) signalling circuit concept for FPGA implementations, b) signal diagram.

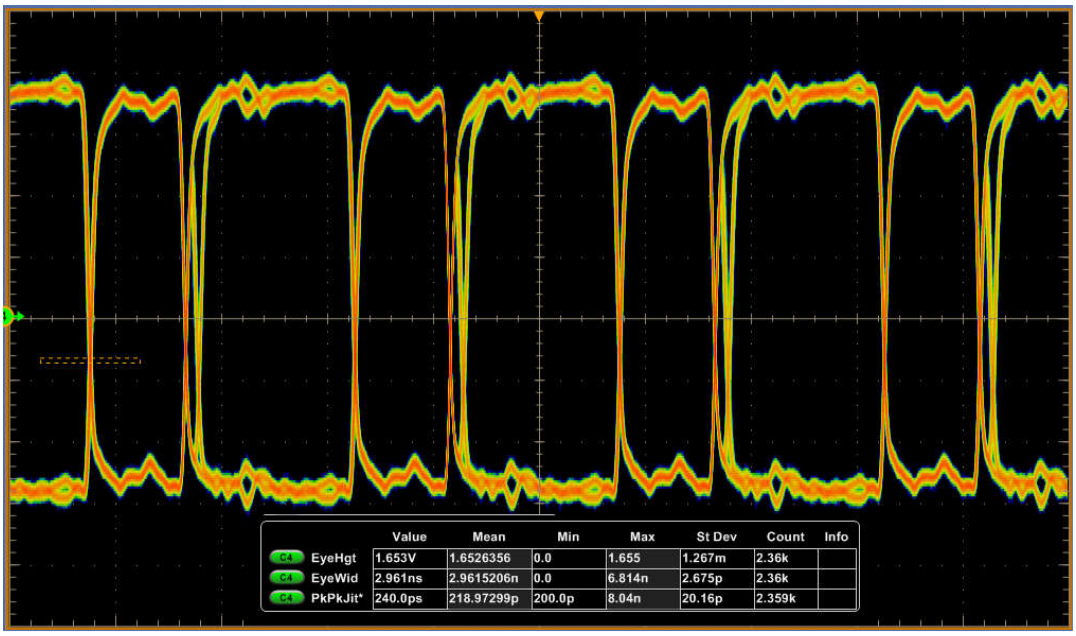
5.2 PERFORMANCE OF EQUALIZATION

In the first case the performance of both PWM and PWM-2 equalization methods for lower transmission rate 200 Mbps are compared. In this case it can be expected lower high frequency content attenuation which mainly defines sharp signal transitions, especially during long sequences of alternating symbols ...1010101... generated by transmitter. After comparing of both eye diagrams for PWM and PWM-2 data streams it can be found that due to the better possibility to set appropriate pulse shaping in PWM-2 configuration higher eye opening is achieved. Note that the jitter and noise parameters are worst for PWM-2 signalling, see Tab. 5.1.

In the second case the transmission rate was increased by more than 50 %. It is necessary to keep in mind that transmission channel completely closes eye diagram for conventional NRZ signalling. It is obvious that Nyquist frequency for higher transmission rates is situated in an area where channel losses reach almost 30 dB. A comparison of the performance of both signalling techniques shows better results for PWM-2 pulse. Note that the eye height, eye width, jitters and noise parameters are completely better than in the case of PWM pulse, see Tab. 5.1 and 5.2. If both input pulses for PWM techniques are compared (only PCB trace from transmitter affects the data signal) it can be seen that the basic parameters like the eye height and jitter are very similar. However, it is obvious that PWM-2 signal has signal amplitude reduction from initial 1.800 V to 1.497 V (16.83 % reduction) and PWM signal has signal amplitude reduction from initial 1.800 V to 1.520 V (15.56 % reduction). On the other hand comparison of both outputs eye diagrams brings better performance (+6,4 %) in eye height for PWM-2 signal. This confirms the correctness

or reasoning that PWM-2 filter adjust signal shaping similarly as raised cosine approximation applied on PWM signal and thus signal goes through the channel with the same parameters with lower losses.

a)



b)

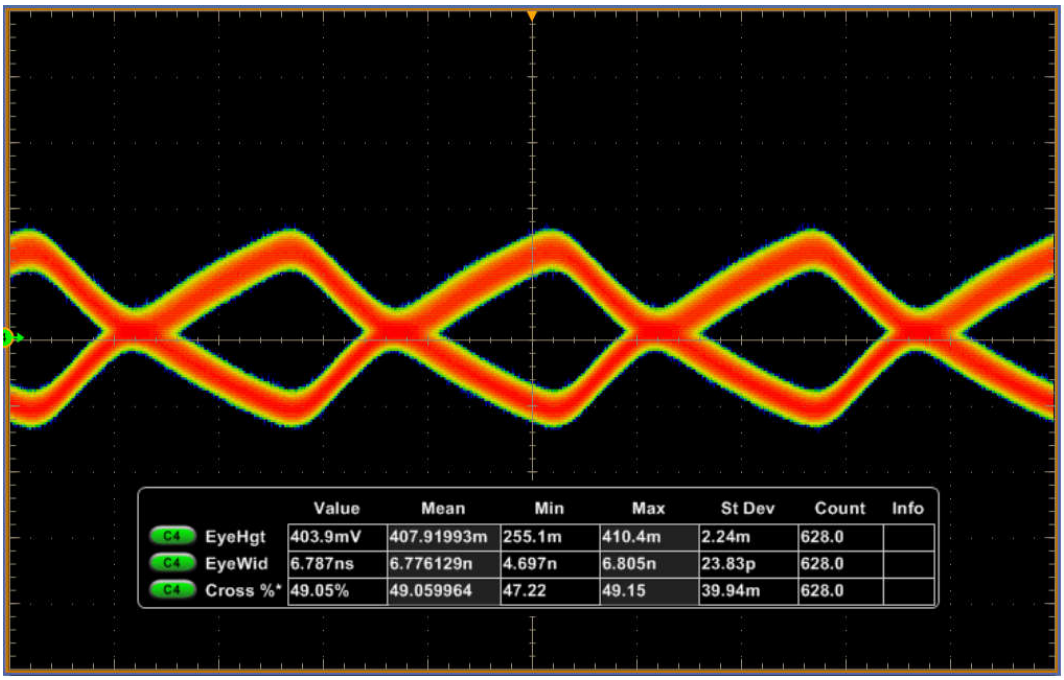
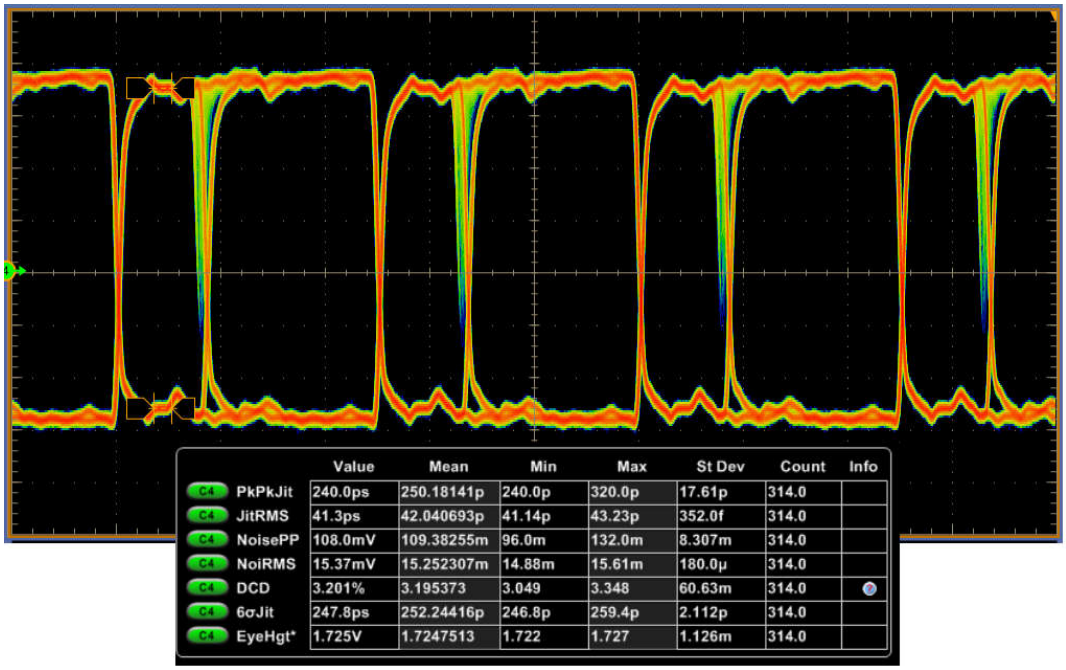


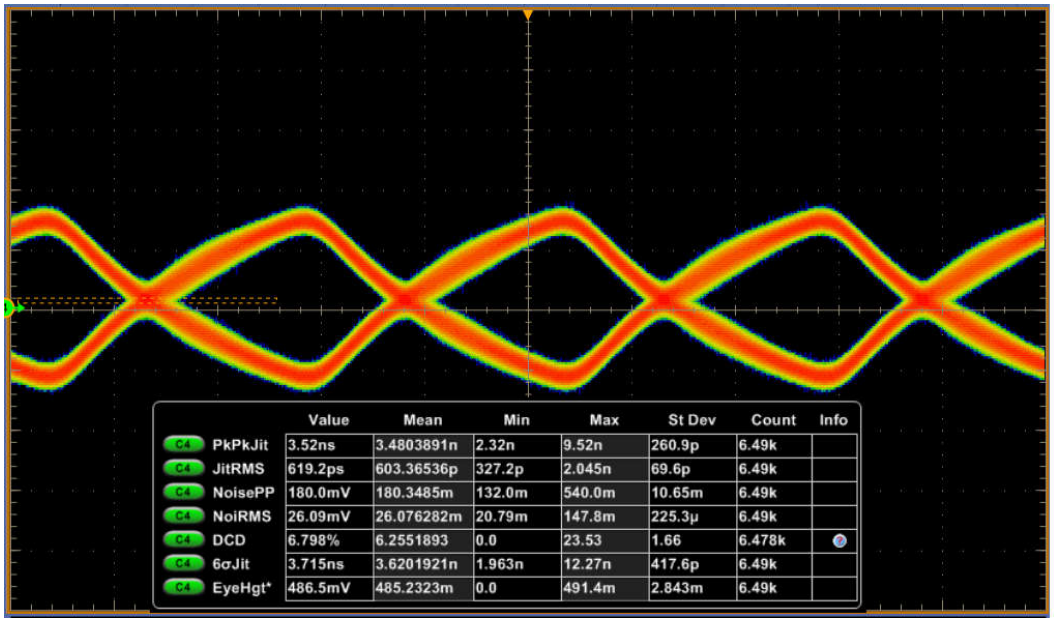
Fig. 5.2: Eye diagrams for PWM signalling (200 Mbps): a) input signal, b) channel output signal.

a)



	Value	Mean	Min	Max	St Dev	Count	Info
PkPkJit	240.0ps	250.18141p	240.0p	320.0p	17.61p	314.0	
JitRMS	41.3ps	42.040693p	41.14p	43.23p	352.0f	314.0	
NoisePP	108.0mV	109.38255m	96.0m	132.0m	8.307m	314.0	
NoiRMS	15.37mV	15.252307m	14.88m	15.61m	180.0µ	314.0	
DCD	3.201%	3.195373	3.049	3.348	60.63m	314.0	
6σJit	247.8ps	252.24416p	246.8p	259.4p	2.112p	314.0	
EyeHgt*	1.725V	1.7247513	1.722	1.727	1.126m	314.0	

b)



	Value	Mean	Min	Max	St Dev	Count	Info
PkPkJit	3.52ns	3.4803891n	2.32n	9.52n	260.9p	6.49k	
JitRMS	619.2ps	603.36536p	327.2p	2.045n	69.6p	6.49k	
NoisePP	180.0mV	180.3485m	132.0m	540.0m	10.65m	6.49k	
NoiRMS	26.09mV	26.076282m	20.79m	147.8m	225.3µ	6.49k	
DCD	6.798%	6.2551893	0.0	23.53	1.66	6.478k	
6σJit	3.715ns	3.6201921n	1.963n	12.27n	417.6p	6.49k	
EyeHgt*	486.5mV	485.2323m	0.0	491.4m	2.843m	6.49k	

Fig. 5.3: Eye diagrams for PWM-2 signalling (200 Mbps): a) input signal, b) channel output signal.

In Tab. 5.1 is clearly demonstrated that during the lower transmission rates, where can be expected less channel low pass effect, the performance of PWM-2 techniques is not better in all parameters. Especially higher jitter and noise content due to the more transitions in the PWM-2 signal is obvious. After increasing of transmission rate the low pass effect of transmission channel was increased significantly. Subsequently it can be seen that PWM-2 signaling is better adjusted for the higher channel losses.

Tab. 5.1: Performance of analyzed equalization techniques - 200 Mbps

	dc = 64 %	dc_1 = 28 %, dc_2 = 90 %	
200 Mbps	PWM	PWM-2	PWM-2 Performance
Eye width [ps]	6787	7892	+ 16.3 %
Eye height [mV]	403.9	486.5	+ 20.6 %
Jitter RMS [ps]	580	619.2	- 6.8 %
Noise RMS [mV]	25.2	26.9	- 6.7 %

Tab. 5.2: Performance of analyzed equalization techniques - 450 Mbps

	dc= 53 %	dc_1= 29 %, dc_2= 76 %	dc= 50 %		
450 Mbps	PWM	PWM-2	PWM	3-TAP FIR	PWM-2 Performance
Eye width [ps]	1385	1530	1182	1848	+10.5 %
Eye height [mV]	68.12	72.46	42.76	57.75	+ 6.4 %
Jitter RMS [ps]	139.1	115.1	173.3	62.31	+17.3 %
NoiseRMS [mV]	8.63	7.94	13.84	11.24	+8 %

6 Research Challenges and Conclusion

In this chapter doctoral thesis is summarized. The main goals of the doctoral thesis are divided into the following points:

- Development of perspective adaptive pre-emphasis techniques that are feasible to implement in modern high-speed CMOS processes according to new trends in low power consumption design.
- Optimalization of the first order time-domain equalization techniques to achieve higher crosstalk immunity to achieve higher loss compensation in real PCB high-speed communication channels.
- Equalization of higher-order transmission channel with more complex transfer functions. Development of complex models of transmission channels which reflect the signal integrity issues that occur during high speed interconnection signaling. Extension of the new proposed scheme of PWM-RC equalization technique to the second order realization.

- Implementation of developed pre-emphasis algorithms to one complex MathCAD model for effective pre-design simulations of equalization techniques performance applicable in practice during high-speed interconnection design.
- Experimental implementations of proposed solutions and optimization of models based on the practical findings.

The first chapters of the doctoral thesis are focused on signal integrity problems which can occur during high-speed data transfer. A several models of high speed transmission channels have been analyzed. Based on the practice measurement on the development board from Texas Instruments the real channel characteristics for a few types of high speed transmission lines were obtain. It is obvious that PCB copper channels suffer from attenuation and dispersion effects which may ultimately reduce the quality of a transmitted signal. Especially for low cost PCB transmission lines is typically use of inexpensive materials for dielectric and low quality fabrication of micro strip lines. Thus, the channel losses can achieve fairly soon tens of decibels at frequencies which correspond with Nyquist frequencies for data rates from gigabits to tens of gigabits. It is evident that there is a very small border between sufficient signal quality at the channel output and the maximum achievable bit rate. Seemingly sufficient transmission channel e.g. for 5 Gbps rate may be unusable for higher transmission rate e.g. 30 % higher transmission rate. It is important to realize that this is not just about overcoming the exponentially growing losses but additional signal discontinuities effects can occur at higher frequencies. Thus, the data signal must overcome far more lossy environments with additional signal integrity issues such as additional reflections or resonant frequency notches.

Other part of the doctoral thesis deals with perspective time-domain pre-emphasis technique usable as an adequate substitute of conventional equalization technique which are not compatible with current requirements for low power CMOS design. Thus, the timing resolution instead of an amplitude resolution is used. The beginning of the work is greatly inspired by the results achieved in [16]. However, the conventional time-domain equalization technique due to the exhibition of more high frequency noise content in data signal can be in practice less powerful than expected results from theoretical simulations. These assumptions were verified during the practical implementations where strong pre-emphasized conventional PWM pulse was tested. It was found that additional loss compensation is not possible because eye diagram opening was significantly reduced by the own noise produced by PWM filter. The additional content of many high-frequency harmonic components which is strongly dependent on low-frequency content in the data signal can cause problems with implementation in high-speed channels with crosstalk susceptibility. Thus, in the main part of the Chapter 3, the novel PWM-RC scheme is proposed, original own contributions are listed in [42], [43]. In comparison with the conventional PWM method, the frequency-domain analysis shows better performance of proposed method for equalization of transmission channels where the attenuation is not monotonically increasing. Additional variability due to the possibility of edge pulse shaping allows achieving higher frequency loss compensation. These key findings can play a critical role for optimal pre-emphasis setting to achieve better eye opening at the channel output. For example, the weak pre-emphasis can be sufficient to low-frequency content compensation but the compensation for high-frequency content is not still sufficient. The solution for the conventional PWM method is to increase the amount of pre-emphasis and it also boosts high-frequency noise. Furthermore, a better signal to noise ratio (SNR) is required. Using an advanced model of higher-order PCB channel based on measured results with differential transmission line implemented in Agilent ADS studio, successful transmission of a 2-PAM 5 Gbps data signal is demonstrated for PWM-RC scheme. The proposed equalization method triples the frequency at which the eye closes completely from 0.8 GHz to 2.5 GHz. In the case of conventional PWM filter the reduction in the loss variation allows only shifting the

frequency at which the eye closes completely from 0.8 GHz to 1.8 GHz. From the practical implementations realized in Chapter 5 it can be concluded that the PWM pre-emphasis is capable to compensate almost 30 dB of channel loss at f_N =200 MHz. It is obvious that pulse edge shaping may ultimately improve jitter parameters of output signal after passing through a lossy channel. It was confirmed during practical measurement was confirmed that the major effect on the overall eye diagram opening has just final pulse shaping on the channel output. Thus, the jitter parameter can be significantly reduced and better eye opening can be achieved with lower overall signal amplitude. Note that it was also found that raised cosine pulse and exponential pulse have tendency to increase BER during increasing of sampling error. Thus, the modified exponential edge pulse shaping was proposed and demonstrated. It is necessary to have in mind the fact that the overall performance of pulse-width modulation technique is strongly dependent on quality of synchronization of PWM clock signal with data signal. Especially, during the increasing of data rates, the synchronization problem can cause additional sampling error, which can be significantly reduced to a certain extent just by using optimized pulse edge shaping, see eye diagram outputs and results in section 3.6. The own publication focused on the pulse shaping optimalization and higher order channel functions are listed in [41], [42] and [43].

In Chapter 4 the novel pulse second order shaping was firstly introduced for high-speed chip-to-chip interconnects. The proposed signalling scheme is based on the results published in the connection with the search for the optimum edge pulse shaping. As can be listed in Fig. 4.2a using the second order PWM-2 scheme it is possible to achieve the channel output signaling which just corresponds with the proposed PWM-RC scheme. Especially during the fast signal transitions the effect of raised cosine shaping allows to achieve better results during the higher order channel compensation. In [46] is published similar idea which was coming out of author's original ideas published two years before in the works [41], [42]. In this paper it seems that some practical measurements were performed not quite right. The output simulation models of eye diagrams are not correspond with PWM shaping. The testing Xilinx kit listed in the work is not able to produce such high data transmission rates with pulse width modulated scheme. The outputs from the practical measurements show unreliable eye diagrams with additionally drawn axes. It confirms the fact mentioned in the previous sentence. In fact, the true measured results from implementation of PWM-2 scheme and detailed information from the performance analysis in the time-domain and frequency domain are listed only in this doctoral thesis. The presented results in Chapter 5 clearly show the parameters of the analyzed transmission channel and the presented eye diagrams show clearly the parameters of the analyzed signal. Also Fig. 5.3 clearly demonstrates that the proposed PWM-2 scheme was truly implemented. As can be seen from the performance comparison of PWM techniques listed in Tab. 5.1 and Tab. 5.2 the proposed PWM-2 scheme is able to achieve better eye opening at the Nyquist frequency of the transmitted pulse which corresponds with current channel losses about 35 dB. It is obvious that conventional PWM scheme does not achieve higher loss compensation than 30 dB and during the compensation of the 35 dB channel losses the eye diagram shows worse result than in the case of PWM-2 filter. In Tab. 5.2 is clearly demonstrated that additional strong pre-emphasis is not able to improve the eye opening and additional noise content is generated. The PWM-2 scheme shows additional potential in future testing because the maximum *dc* coefficients settings are not achieved, especially dc_2 coefficient set to only 76% has a reserve for compensation of pulses with longer tails. According to realized simulation, the maximum limit of loss compensation should be around more than 40 dB.

The original contributions of the doctoral thesis are

- The discovery that by applying modified PWM-RC scheme to wireline equalization the maximal achievable loss compensation during the channel equalization can be improved by an average of 2 dB.
- The discovery that PWM-RC scheme can be optimized by using additional edge pulse shaping with achievable better endurance to the sampling errors.
- Advanced simulation scheme which shows better performance of eye opening if pulses based on raised cosine shaping are produced at the channel output.
- Implementation of previous findings into the new proposed second order PWM-2 signaling scheme with detail analysis of second order PWM-2 scheme in time domain and frequency domain.
- Practical experimental implementations of proposed PWM-2 scheme together with PWM scheme which confirms the discovery realized in the third point and realized simulations.
- 35 db channel loss compensation achieved by using higher order transmission channel

Recommendations for future work

- Practical implementations of PWM-2 pulse scheme on higher transmission rates together with higher order channel loss compensation.
- Possibility to extend PWM pre-emphasis to the systems which use multilevel signaling scheme.
- Other simulation work on the proposed higher order transmission channel which reflects possible signal integrity issues.

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Postgraduate studies at the Department of Radio Electronics, Study Programme: Electrical, Electronic, Communication and Control Technology
Topic of dissertation thesis: Signal integrity optimization techniques for high-speed inter-chip signalling.

2007 - 2009 Master's degree (MSc) - inženýr (Ing-), FEEC BUT Brno
Electrical engineering, telecommunications and computer technologies Department of Radio Electronics, Study Programme: Electrical, Electronic, Communication and Control Technology
Topic of master's thesis: digitally controlled active second order electrical filters

2004 - 2007 Bachelors's degree (BSc) - bakalář (Bc.), FEEC BUT Brno
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Topic of bachelor's thesis: Digitally television planimeter

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ABSTRACT

The doctoral thesis deals with signal integrity problems in modern chip circuits. Based on the simulation and practical experiments an optimized second order pre-emphasis signaling technique is proposed. High bandwidth efficiency of signal pre-emphasis together with a minimum voltage swing during signal emphasizing and still lower power dissipation are the main features respected in the proposal. The performed analysis clearly shows that proposed pulse shaping method due to the spectral efficiency can increase the transmission bandwidth of low cost wire channels. The performance of proposed signaling technique is demonstrated on various type channels with higher order transfer function. Additional channel impairments which can occur during transmission channel design are discussed too.

ABSTRAKT

Tato disertační práce je obsahově zaměřená na problematiku integrity signálů v moderních čipových obvodech. Na základě provedených simulací a praktických experimentů byl proveden návrh equalizační techniky druhého řádu pro efektivnější vysokorychlostní komunikaci. Předložený návrh respektuje současné požadavky na vyvíjené signalizační techniky, které zahrnují efektivnější využití šířky pásma přenosového kanálu a energetickou úsporu. Provedené analýzy podrobně ukazují možnost zvýšení přenosové rychlosti při přenosu signálu skrz nízkonákladové přenosové kanály s využitím navržené signální metody. Výkonnost navrhované signalizační techniky je demonstrována na různých typech přenosových kanálů s přenosovou funkcí vyššího řádu. Diskutovány jsou rovněž možnosti omezení rušivých vlivů na přenosové kanály během návrhu.